

The documentation and process conversion measures necessary to comply with this revision shall be completed by 1 January 2004.

INCH-POUND

MIL-PRF-19500/596F
 1 October 2003
 SUPERSEDING
 MIL-PRF-19500/596E
 14 August 2002

PERFORMANCE SPECIFICATION

SEMICONDUCTOR DEVICE, REPETITIVE AVALANCHE, FIELD EFFECT,
 TRANSISTOR, N-CHANNEL, SILICON,
 TYPES 2N7218, 2N7219, 2N7221, 2N7222, 2N7218U, 2N7219U,
 2N7221U, 2N7222U, JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a N-channel, enhancement mode, MOSFET, power transistor intended for use in high density power switching applications. Four levels of product assurance are provided for each device type as specified in MIL-PRF-19500, with avalanche energy maximum ratings (E_{AR} and E_{AS}) and maximum avalanche current I_{AR} . Two levels of product assurance are provided for die (element evaluation).

1.2 Physical dimensions. See figure 1 (TO-254AA), figure 2 for JANHC and JANKC (die) dimensions, and figure 3 for surface mount (TO-267AB).

* 1.3 Maximum ratings ($T_C = +25^\circ\text{C}$, unless otherwise specified).

Type	$V_{(BR)DSS}$ min $V_{GS} = 0\text{ V}$ $I_D = 1.0\text{ mA}$ dc	P_T (1) $T_C = +25^\circ\text{C}$	P_T $T_A = +25^\circ\text{C}$	V_{GS}	I_{D1} (2) (3) $T_C = +25^\circ\text{C}$	I_{D2} (2) $T_C = +100^\circ\text{C}$	I_S	I_{DM} (4)	T_{op} and T_{STG}
	<u>V dc</u>	<u>W</u>	<u>W</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A (pk)</u>	<u>°C</u>
2N7218, 2N7218U	100	125	4	± 20	28	20	28	112	-55 to +150
2N7219, 2N7219U	200	125	4	± 20	18	11	18	72	-55 to +150
2N7221, 2N7221U	400	125	4	± 20	10	6	10	40	-55 to +150
2N7222, 2N7222U	500	125	4	± 20	8	5	8	32	-55 to +150

See footnotes next page.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43216-5000, by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

* 1.3 Maximum ratings - continued.

Type	I _{AR}	E _{AS}	E _{AR}	V _(ISO) at 100,000 feet	R _{θJC} max	r _{DS(on)} max (5) V _{GS} = 10 V dc I _D = I _{D2}	
						T _J = +25°C	T _J = +150°C
	<u>A</u>	<u>mj</u>	<u>mj</u>		<u>°C/W</u>	<u>Ω</u>	<u>Ω</u>
2N7218, 2N7218U	28	250	12.5		1.0	0.077	0.154
2N7219, 2N7219U	18	450	12.5		1.0	0.18	0.387
2N7221, 2N7221U	10	650	12.5	400	1.0	0.55	1.32
2N7222, 2N7222U	8	700	12.5	500	1.0	0.85	2.04

- (1) Derate linearly 1.0 W/°C for T_C > +25°C;
- (2) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal wires and may be limited by pin diameter:

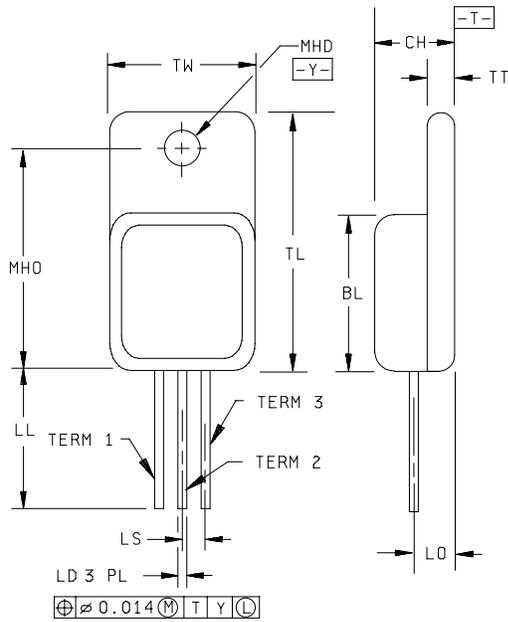
$$I_D = \sqrt{\frac{T_J \text{ max} - T_C}{(R_{\theta JC}) \times (R_{DS(ON)} \text{ at } T_{Jmax})}}$$

- (3) See figure 4, maximum drain current graph.
- (4) I_{DM} = 4 x I_{D1} as calculated in note 2.
- (5) Pulsed (see 4.5.1).

1.4 Primary electrical characteristics. T_C = +25°C (unless otherwise specified).

Type	Min V _{(BR)DSS} V _{GS} = 0 I _D = -1.0 mA dc	V _{GS(th)1} V _{DS} ≥ V _{GS} I _D = -0.25 mA dc		Max I _{DSS1} V _{GS} = 0 V V _{DS} = 80 percent of rated V _{DS}	Max r _{DS(on)1} (1) I _D = I _{D2} V _{GS} = 10 V
	<u>V dc</u>	<u>V dc</u>		<u>μA dc</u>	<u>Ohms</u>
		<u>Min</u>	<u>Max</u>		
2N7218, 2N7218U	100	2.0	4.0	25	0.077
2N7219, 2N7219U	200	2.0	4.0	25	0.18
2N7221, 2N7221U	300	2.0	4.0	25	0.55
2N7222, 2N7222U	400	2.0	4.0	25	0.85

- (1) Pulsed (see 4.5.1).

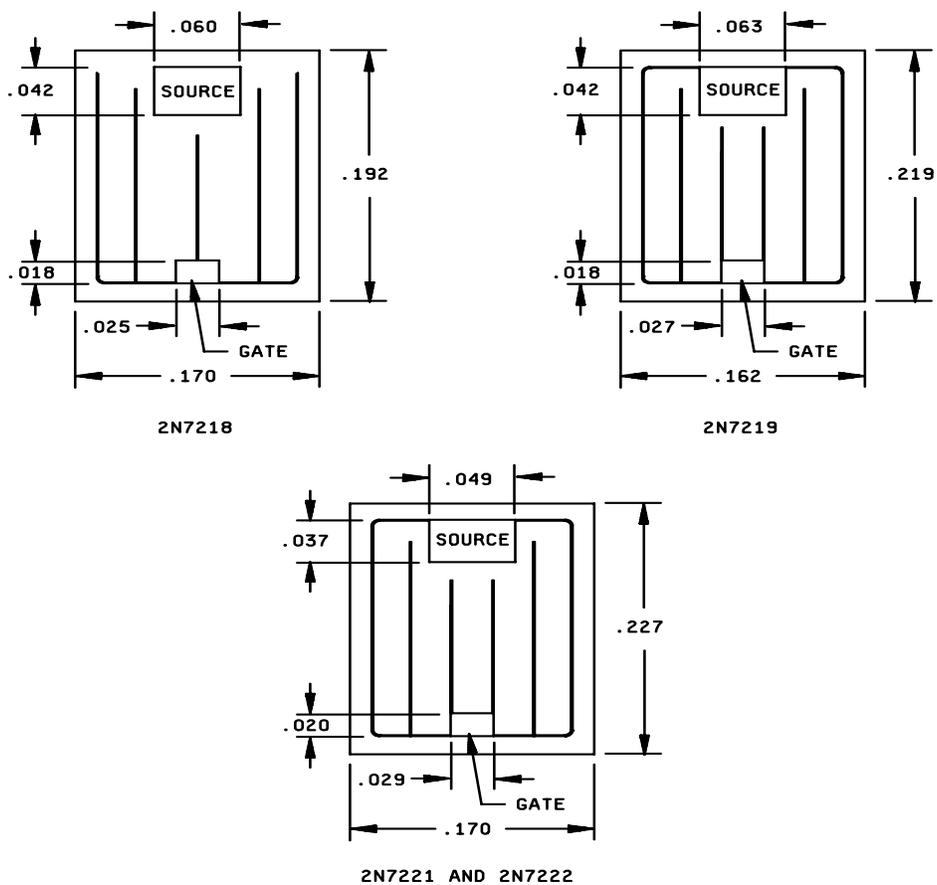


Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.535	.545	13.59	13.84	
CH	.249	.260	6.32	6.60	
LD	.035	.045	0.89	1.14	
LL	.510	.570	12.95	14.48	
LO	.150 BSC		3.81 BSC		
LS	.150 BSC		3.81 BSC		
MHD	.139	.149	3.53	3.78	
MHO	.665	.685	16.89	17.40	
TL	.790	.800	20.07	20.32	3, 4
TT	.040	.050	1.02	1.27	
TW	.535	.545	13.59	13.84	3, 4
Term 1	Drain				
Term 2	Source				
Term 3	Gate				

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Glass meniscus included in dimension TL and TW.
4. All terminals are isolated from case.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.

* FIGURE 1. Physical dimensions for TO-254AA (2N7218, 2N7219, 2N7221 and 2N7222).

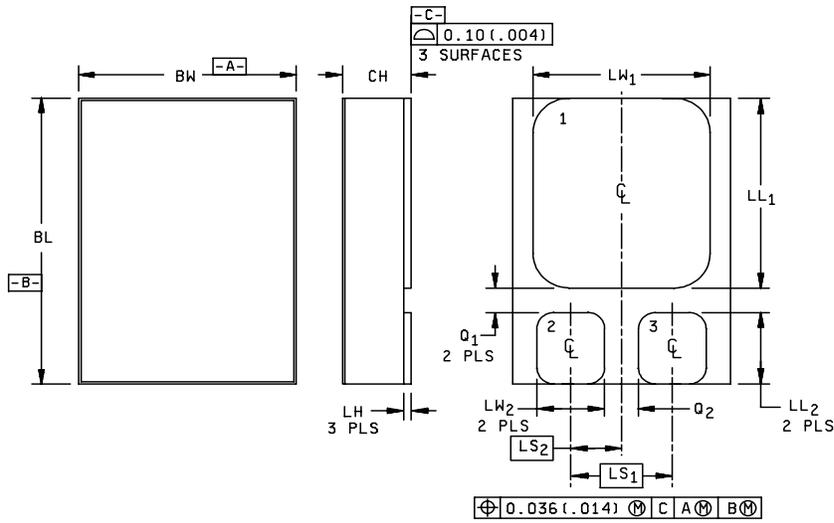


Inches	mm	Inches	mm	Inches	mm
.018	0.46	.037	0.94	.162	4.11
.020	0.51	.042	1.07	.170	4.32
.025	0.64	.049	1.24	.192	4.88
.027	0.69	.060	1.52	.219	5.56
.029	0.74	.063	1.60	.227	5.77

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Unless otherwise specified, tolerance is ± 0.005 inch (0.13 mm).
4. The physical characteristics of the die thickness are .0187 inch (0.475 mm). The back metals are chromium, nickel, and silver. The top metal is aluminum and the back contact is the drain.
5. See 6.4 for ordering information.
6. Dimensions are in accordance with ASME Y14.5M.

* FIGURE 2. JANHc and JANKC (A-version) die dimensions.



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.620	.630	15.75	16.00
BW	.445	.455	11.30	11.56
CH		.142		3.60
LH	.010	.020	0.26	0.50
LL ₁	.410	.420	10.41	10.67
LL ₂	.152	.162	3.86	4.11
LS ₁	.210 BSC		5.33 BSC	
LS ₂	.105 BSC		2.67 BSC	
LW ₁	.370	.380	9.40	9.65
LW ₂	.135	.145	3.43	3.68
Q ₁	.030		0.76	
Q ₂	.035		0.89	
Term 1	Drain			
Term 2	Gate			
Term 3	Source			

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for information only.
3. The lid shall be electrically isolated from the drain, gate and source.
4. Dimensioning and tolerancing shall be in accordance with ASME Y14.5M.

* FIGURE 3. Dimensions and configuration of surface mount package outline (TO-267AB), 2N7218U, 2N7219U, 2N7221U and 2N7222U.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

STANDARD

DEPARTMENT OF DEFENSE

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from the Document Automation and Production Services (DAPS), Building 4D (DPM-DODSSP), 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

* 3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figures 1 (TO-254AA), 2 (die), and 3 (TO-267AB, surface mount) herein. Methods used for electrical isolation of the terminal feedthroughs shall employ materials that contain a minimum of 90 percent AL_2O_3 (ceramic). Examples of such construction techniques are metallized ceramic eyelets or ceramic walled packages.

* 3.4.1 Lead formation, material, and finish. Lead material shall be Kovar or Alloy 52; a copper core or plated core is permitted. Lead finish shall be solderable in accordance with MIL-STD-750, MIL-PRF-19500 and herein. Where a choice of finish is desired, it shall be specified in the acquisition document (see 6.2). When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with screen 14 of MIL-PRF-19500 and 100 percent dc testing in accordance with table I, subgroup 2 herein.

3.4.2 Internal construction. Multiple chip construction shall not be permitted.

3.5 Electrostatic discharge protection. The devices covered by this specification require electrostatic protection.

3.5.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. The following handling procedures shall be followed:

- a. Devices shall be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent, if practical.
- g. Care shall be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source. $R \leq 100 \text{ k}\Omega$, whenever bias voltage is to be applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

* 3.7 Electrical test requirements. The electrical test requirements shall be table I, as specified herein

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500, except at the option of the manufacturer, the country of origin and/or the manufacturers identification may be omitted from the body of the transistor.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500, and as specified herein. Alternate flow is allowed for qualification inspection in accordance with MIL-PRF-19500.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the associated specification that did not request the performance of table II tests, the tests specified in table II herein shall be performed by the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANS, JANTX, and JANTXV levels). Screening shall be in accordance with table IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTX and JANTXV level
(3)	Gate stress test (see 4.3.2)	Gate stress test (see 4.3.2)
(3)	Method 3470 of MIL-STD-750. (see 4.3.3)	Method 3470 of MIL-STD-750. (see 4.3.3)
(3) 3c	Method 3161 of MIL-STD-750 (see 4.3.4)	Method 3161 of MIL-STD-750 (see 4.3.4)
9	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , subgroup 2 of table I herein;	Subgroup 2 of table I herein
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(on)1}$, $V_{GS(th)1}$ Subgroup 2 of table I herein. $\Delta I_{GSSF1} = +20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = -20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or ± 100 percent of initial value, whichever is greater.	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(on)1}$, $V_{GS(th)1}$ Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A or $T_A = +175^\circ\text{C}$ and $t = 48$ hours
13	Subgroup 2 and 3 of table I herein. $\Delta I_{GSSF1} = +20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = -20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value. $\Delta V_{GS(th)1} = \pm 20$ percent of initial value.	Subgroup 2 of table I herein. $\Delta I_{GSSF1} = +20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = -20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value. $\Delta V_{GS(th)1} = \pm 20$ percent of initial value.

- (1) At the end of the test program, I_{GSSF1} , I_{GSSR1} , and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1} , I_{GSSR1} , I_{DSS1} , and $V_{GS(th)1}$ shall be invoked.
- (3) Shall be performed anytime before screen 9.

* 4.3.1 Screening (JANHNC and JANKC). Screening of die shall be in accordance with MIL-PRF-19500 appendix H. As a minimum die, shall be 100 percent probed in accordance with table I, subgroup 2 except test current shall not exceed 20 amperes.

* 4.3.2 Gate stress test. Apply $V_{GS} = 30$ V minimum for $t = 250$ μ s minimum.

* 4.3.3 Single pulse avalanche energy (E_{AS}).

- a. Peak current (I_{AS}) I_{D1} .
- b. Peak gate voltage (V_{GS}) 10 V.
- c. Gate to source resistor (R_{GS})..... $25 \leq R_{GS} \leq 200 \Omega$.
- d. Initial case temperature..... $+25^{\circ}\text{C}$ $+10^{\circ}\text{C}$, -5°C .
- e. Inductance:..... $\left[\frac{2E_{AS}}{(I_{D1})^2} \right] \left[\frac{V_{BR} - V_{DD}}{V_{BR}} \right]$ mH minimum.
- f. Number of pulses to be applied 1 pulse minimum.
- g. Supply voltage (V_{DD}) 50 V, 25 V for 100 V devices.

* 4.3.4 Thermal impedance ($Z_{\theta JC}$ measurements). The $Z_{\theta JC}$ measurements shall be performed in accordance with method 3161 of MIL-STD-750. The maximum limit (not to exceed the table I, subgroup 2 limit or figure 5 thermal impedance curve) for $Z_{\theta JC}$ in screening (table IV of MIL-PRF-19500) shall be derived by each vendor by means of statistical process control. When the process has exhibited control and capability, the capability data shall be used to establish the fixed screening limit. In addition to screening, once a fixed limit has been established, monitor all future sealing lots using a random five piece sample from each lot to be plotted on the applicable X bar R chart. If a lot exhibits an out of control condition, the entire lot shall be removed from the line and held for engineering evaluation and disposition. This procedure may be used in lieu of an in-line monitor. The following parameter measurements shall apply:

- a. Measuring current (I_M) 10 mA.
- b. Drain heating current (I_H)..... 3.3 A minimum (2.5 A minimum for surface mount devices).
- c. Heating time (t_H) 100 ms minimum (25 ms minimum for surface mount devices).
- d. Drain-source heating voltage (V_H)..... 25 V minimum (20 V minimum for surface mount devices).
- e. Measurement time delay (t_{MD}) 30 to 60 μ s maximum.
- f. Sample window time (t_{SW}) 10 μ s maximum.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

* 4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein. Electrical measurements (end-points) shall be in accordance with the inspections of table I, subgroup 2 herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VIa (JANS) and table VIb (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and herein. Electrical measurements (end-points) shall be in accordance with the inspections of table I, subgroup 2 herein. See 4.3.4, (c = 0, n = 22 for 4.3.4).

4.4.2.1 Group B inspection, table VIa (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B3	1051	Test condition G.
B3	2037	Test condition A. All internal bond wires for each device shall be pulled separately.
B4	1042	Test condition D; the heating cycle shall be 1 minute minimum, 2,000 cycles. No heat sink nor forced air cooling on the device shall be permitted during the cycle.
B5	1042	Accelerated steady-state operation life; test condition A, $V_{DS} = \text{rated}$ $T_A = +175^\circ\text{C}$, $t = 120$ hours minimum. Read and record $V_{(BR)DSS}$ (pre and post at $1 \text{ mA} = I_D$. Read and record I_{DSS} (pre and post). Deltas for $V_{(BR)DSS}$ shall not exceed 10 percent and I_{DSS} shall not exceed $25 \mu\text{A}$. Accelerated steady-state gate stress; condition B, $V_{GS} = \text{rated}$, $T_A = +175^\circ\text{C}$, $t = 24$ hours.
B5	2037	Bond strength; test condition A.
B6	3161	See 4.5.2.

* 4.4.2.2 Group B inspection, table VIb (JAN, JANTX and JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G.
B3	1042	Test condition D, 2,000 cycles minimum. The heating cycle shall be 1 minute minimum.
B5	3161	See 4.5.2.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with the inspections of table I, subgroup 2 herein. See 4.3.4, ($c = 0$, $n = 22$ for 4.3.4).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	1056	Test condition B.
C2	2036	Tension: Test condition A; weight = 10 lbs, $t = 10$ s (not applicable to "U" suffix version).
C5	3161	See 4.5.2.
C6	1042	Test condition D, 6,000 cycles minimum. The heating cycle shall be 1 minute minimum.

4.5 Methods of inspection. Methods of inspection shall be as specified in appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurements shall be as specified in MIL-STD-750.

4.5.2 Thermal resistance. Thermal resistance measurements shall be performed in accordance with method 3161 of MIL-STD-750. The maximum limit of $R_{\theta JC(max)}$ shall be $1.0^{\circ}C/W$. The following parameter measurements shall apply:

- a. Measuring current (I_M) 10 mA.
- b. Drain heating current (I_H) 3.3 A minimum (2.5 A minimum for surface mount devices).
- c. Heating time (t_H) Steady-state (see method 3161 of MIL-STD-750 for definition).
- d. Drain-source heating voltage (V_H) 25 V minimum (20 V minimum for surface mount devices).
- e. Measurement time delay (t_{MD}) 30 to 60 μs maximum.
- f. Sample window time (t_{SW}) 10 μs maximum.

* TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3161	See 4.3.4	$Z_{\theta JC}$		0.9	$^{\circ}C/W$
Breakdown voltage, drain to source 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U	3407	Bias condition C, $V_{GS} = 0V$, $I_D = 1$ mA dc	$V_{(BR)DSS}$	100 200 400 500		V dc V dc V dc V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = .25$ mA	$V_{GS(th)1}$	2.0	4.0	V dc
Gate current	3411	Bias condition C, $V_{GS} = 20$ V dc, $V_{DS} = 0$ V dc	I_{GSSF1}		100	nA dc
Gate current	3411	Bias condition C, $V_{GS} = -20$ V dc, $V_{DS} = 0$ V dc	I_{GSSR1}		-100	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0$ V dc, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS1}		25	μA dc
Static drain to source on-state resistance 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U	3421	$V_{GS} = 10$ V dc, condition A, pulsed (see 4.5.1), $I_D =$ rated I_{D2} (see 1.3)	$r_{DS(on)1}$		0.077 0.18 0.55 0.85	Ω Ω Ω Ω
Static drain to source on-state resistance 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U	3421	$V_{GS} = -10$ V dc, condition A, pulsed (see 4.5.1), $I_D =$ rated I_{D1} (see 1.3)	$r_{DS(on)2}$		0.125 0.25 0.70 0.95	Ω Ω Ω Ω

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 2</u> - Continued						
Forward voltage (source drain diode)	4011	$V_{GS} = 0 \text{ V dc}$, $I_D = \text{rated } I_{D1}$, pulsed (see 4.5.1)	V_{SD}		1.5	V
<u>Subgroup 3</u>						
High temperature operation:		$T_C = T_J = +125^\circ\text{C}$				
Gate current	3411	Bias condition C, $V_{GS} = 20 \text{ V dc}$, $V_{DS} = 0 \text{ V dc}$,	I_{GSSF2}		200	nA dc
Gate current	3411	Bias condition C, $V_{GS} = -20 \text{ V dc}$, $V_{DS} = 0 \text{ V dc}$,	I_{GSSR2}		-200	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0 \text{ V dc}$, $V_{DS} = 100 \text{ percent of rated } V_{DS}$	I_{DSS2}		1.0	mA dc
Drain current	3413	Bias condition C, $V_{GS} = 0 \text{ V dc}$, $V_{DS} = 80 \text{ percent of rated } V_{DS}$	I_{DSS3}		0.25	mA dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 0.25 \text{ mA}$	$V_{GS(th)2}$	1.0		V dc
Static drain to source on-state resistance 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U	3421	$V_{GS} = 10 \text{ V dc}$, pulsed (see 4.5.1), $I_D = \text{rated } I_{D2}$ (see 1.3)	$r_{DS(on)3}$		0.24 0.48 1.44 2.04	Ω Ω Ω Ω
Low temperature operation:		$T_C = T_J = -55^\circ\text{C}$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 0.25 \text{ mA}$	$V_{GS(th)3}$		5.0	V dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 4</u>						
Switching time test	3472	$I_D = \text{rated } I_{D2}$ (see 1.3), $V_{GS} = -10$ V dc, gate drive impedance = 9.1 Ω , $V_{DD} = 50$ percent of $V_{BR(DSS)}$				
Turn-on delay time 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U			$t_{d(on)}$		21 20 25 21	ns ns ns ns
Rise time 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U			t_r		105 105 92 73	ns ns ns ns
Turn-off delay time 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U			$t_{d(off)}$		64 58 79 72	ns ns ns ns
Fall time 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U			t_f		65 67 58 51	ns ns ns ns
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See figure 6; $t_p = 10$ ms, $V_{DS} = 80$ percent of rated $V_{BR(DSS)}$, $V_{DS} = 200$ V maximum				
Electrical measurements		See table I, subgroup 2				
<u>Subgroup 6</u>						
Not applicable						

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 7</u>						
Gate charge	3471	Condition B				
On-state gate charge 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U			$Q_{g(on)}$		59 60 65 68.5	nC nC nC nC
Gate to source charge 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U			Q_{gs}		16 14.6 14.0 12.5	nC nC nC nC
Gate to drain charge 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U			Q_{gd}		30.7 37.6 40.5 42.4	nC nC nC nC
Reverse recovery time 2N7218, 2N7218U 2N7219, 2N7219U 2N7221, 2N7221U 2N7222, 2N7222U	3473	$di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq 30 \text{ V}$, $I_D = I_{D1}$, (see 1.3)	t_{rr}		400 500 600 700	ns ns ns ns

1/ For sampling plan, see MIL-PRF-19500.

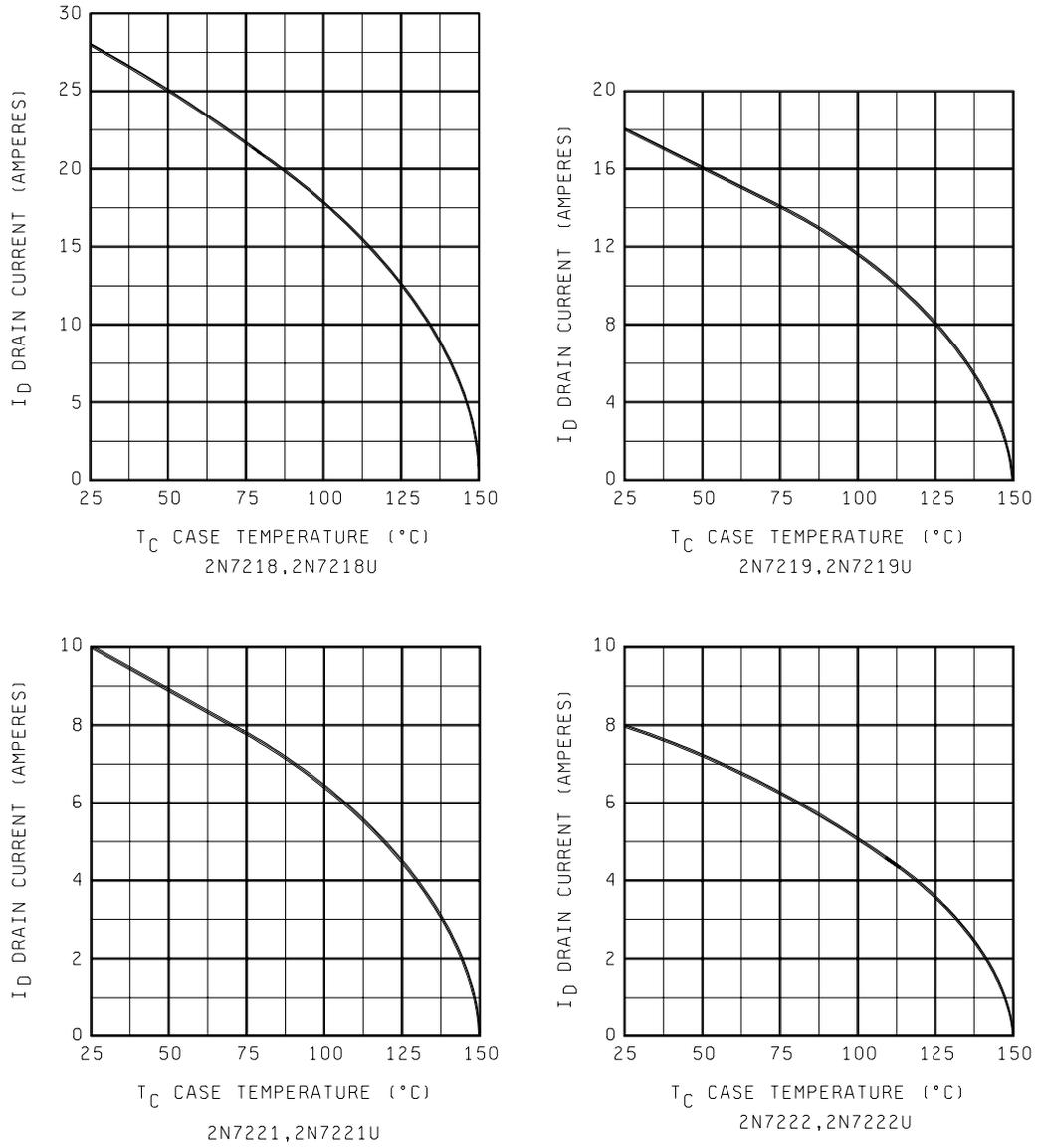
2/ This test is required for the following end-point measurement only (not intended for screen 9, 11, or 13): JANS, table VIa of MIL-PRF-19500, group B, subgroups 3 and 4; JAN, JANTX, and JANTXV, table VIb of MIL-PRF-19500, group B, subgroups 2 and 3; and table VII of MIL-PRF-19500, group C, subgroup 6, and table IX of MIL-PRF-19500, group E, subgroup 1.

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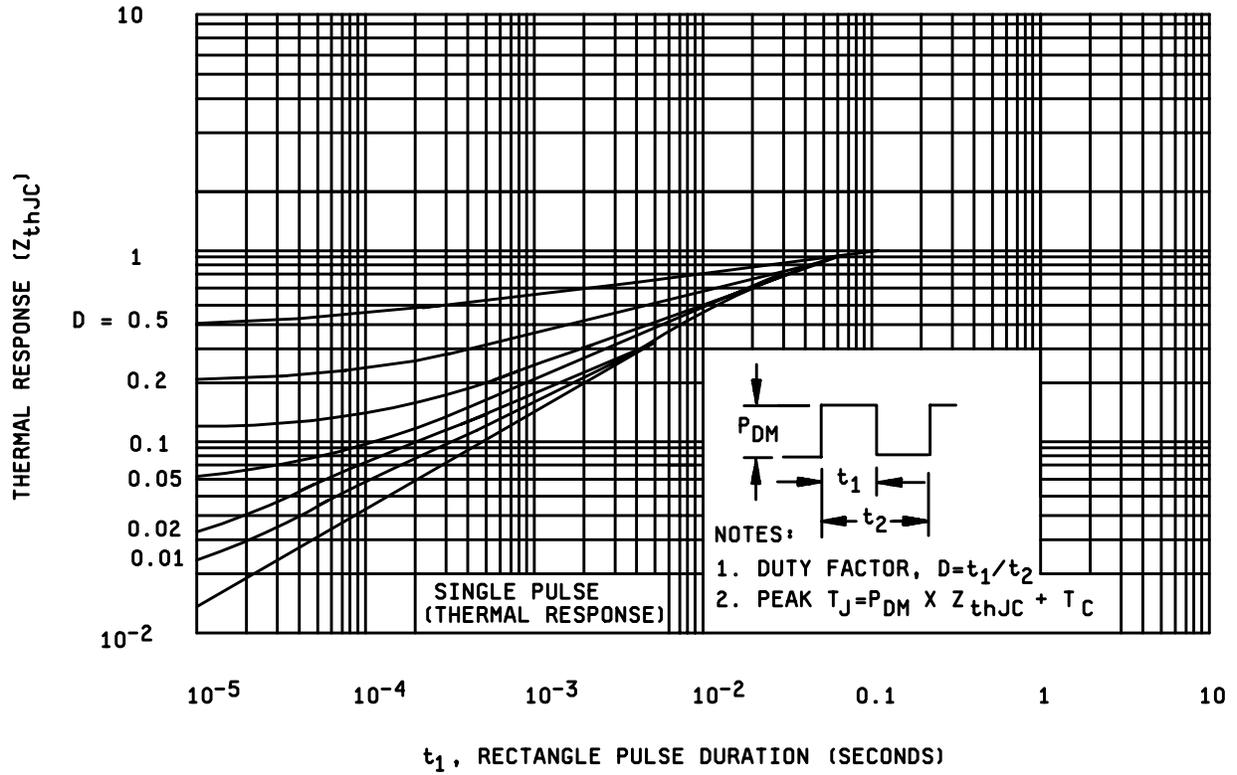
* TABLE II. Group E inspection (all quality levels except JANHC and JANKC) for qualification or requalification only.

Inspection	MIL-STD-750		Sampling plan
	Method	Conditions	
<u>Subgroup 1</u>			
Temperature cycling	1051	-55 to 150°C, 500 cycles	45 devices c = 0
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2	
<u>Subgroup 2 1/</u>			
Steady-state reverse bias	1042	Condition A, 1,000 hours	45 devices c = 0
Electrical measurements		See table I, subgroup 2	
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
<u>Subgroup 3</u>			
DPA	2102		3 devices c = 0
<u>Subgroup 4</u>			
Thermal impedance curves		Each supplier shall submit their (typical) design thermal impedance curves. In addition, test conditions and $Z_{\theta JX}$ limit shall be provided to the qualifying activity in the qualification report	sample size N/A
<u>Subgroup 5 2/</u>			
Barometric pressure test 2N7221, 2N7221U 2N7222, 2N7222U	1001	Condition C, $V_{(ISO)} = V_{DS}$ $V_{DS} = 400$ V dc $V_{DS} = 500$ V dc	5 devices c = 0
<u>Subgroup 6</u>			
ESD	1020		3 devices
<u>Subgroup 7</u>			
Soldering heat	2031	1 cycle	45 devices c = 0
<u>Subgroup 8</u>			
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476		45 devices c = 0

See footnotes at end of table.

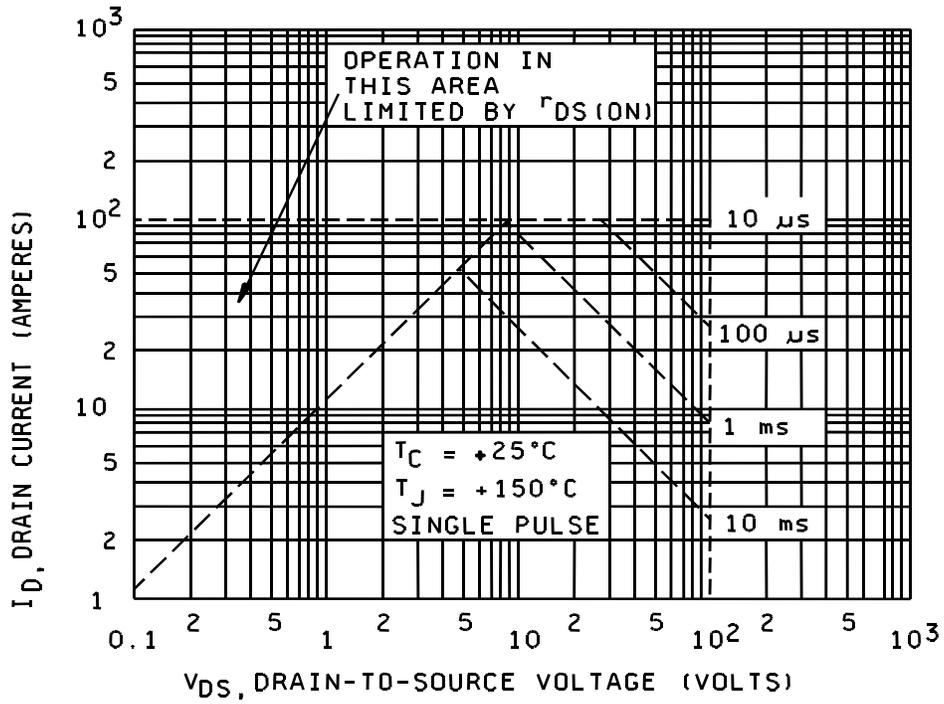


* FIGURE 4. Maximum drain current vs case temperature graphs.



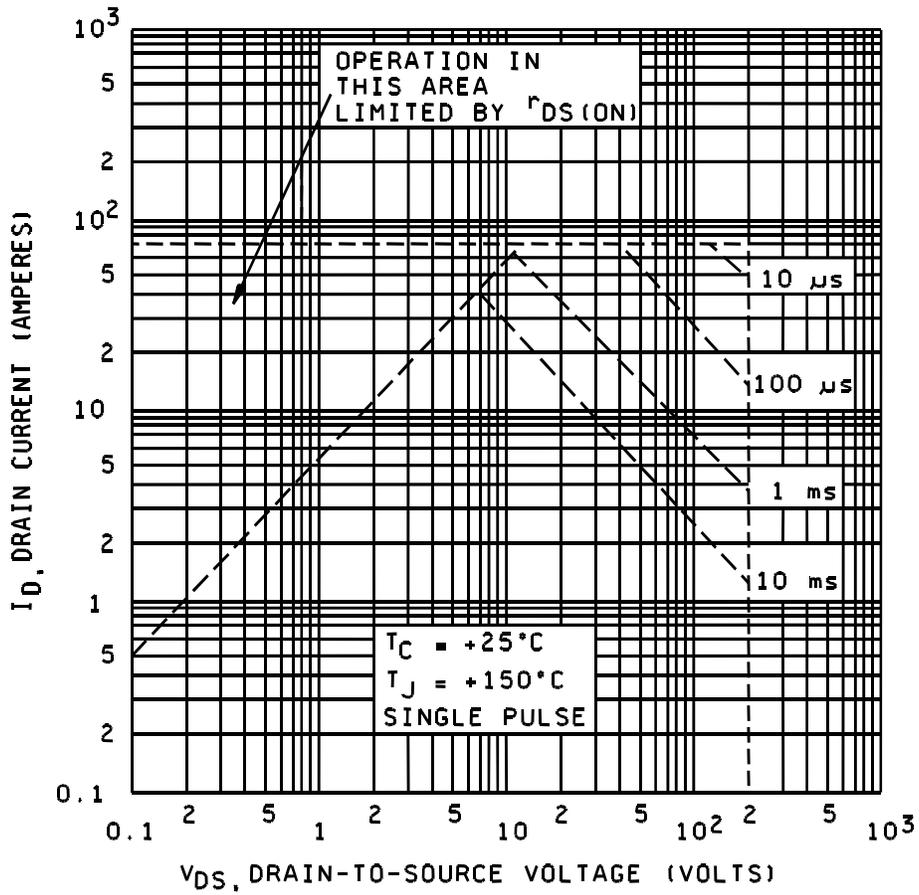
* FIGURE 5. Thermal response.

2N7218, 2N7218U



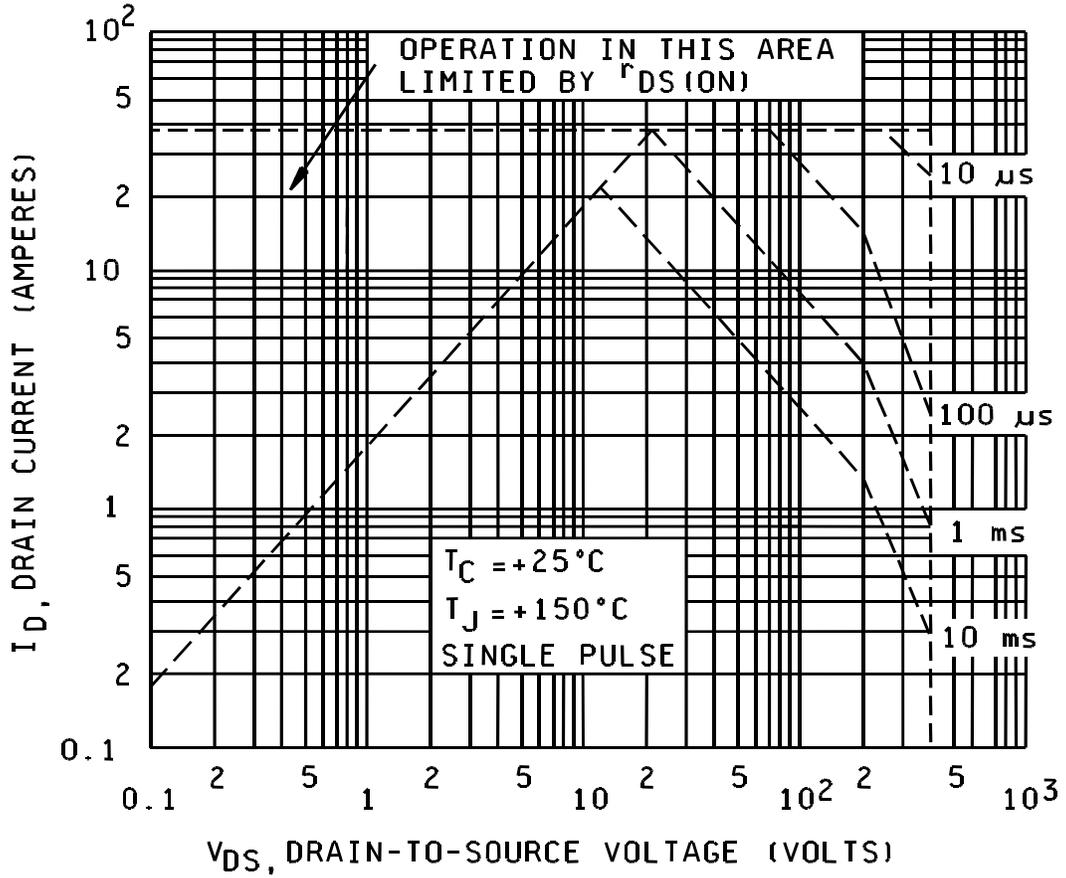
* FIGURE 6. Safe operating area.

2N7219, 2N7219U

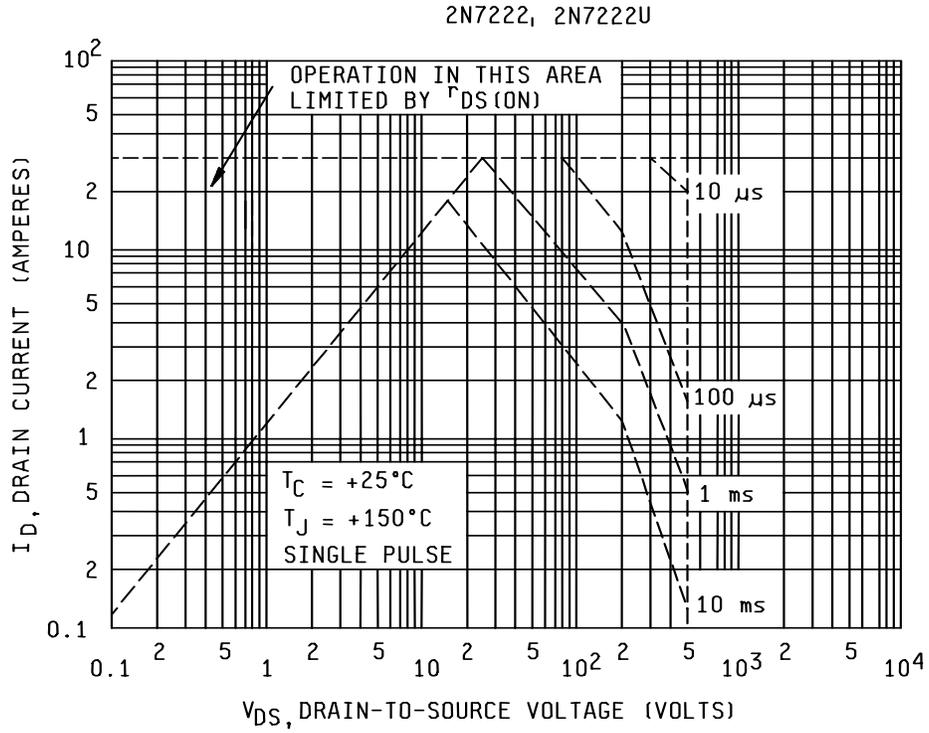


* FIGURE 6. Safe operating area - Continued.

2N7221, 2N7221U



* FIGURE 6. Safe operating area - Continued.



* FIGURE 6. Safe operating area - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Points' packaging activity within the Military Department or Defense Agency, or within the Military Departments' System Command. Packaging data retrieval is available from the managing Military Departments' or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents must specify the following:

- a. Title, number, and date of this specification.
- b. Issue of DODISS to be cited in the solicitation and, if required, the specific issue of individual documents referenced (see 2.2.1).
- c. Lead finish (see 3.4.1).
- d. Type designation and product assurance level. For die acquisition, specify the JANHC or JANKC letter version (see figure 2 and 6.4).
- e. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers' List (QML) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43216-5000.

6.4 Suppliers of JANHC and JANKC die. The qualified die suppliers with the applicable letter version (example JANHCA2N7218) will be identified on the QML.

JANC ordering information		
Military PIN	Manufacturer	
	59993	59993
2N7218	JANHCA2N7218	JANKCA2N7218
2N7219	JANHCA2N7219	JANKCA2N7219
2N7221	JANHCA2N7221	JANKCA2N7221
2N7222	JANHCA2N7222	JANKCA2N7222

6.5 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable as a substitute for the military PIN.

Military PIN	Manufacturer's CAGE	Manufacturer's and user's PIN
2N7218	59993	IRFM 140
2N7219	59993	IRFM 240
2N7221	59993	IRFM 340
2N7222	59993	IRFM 440
2N7218U	59993	IRFN 140
2N7219U	59993	IRFN 240
2N7221U	59993	IRFN 340
2N7222U	59993	IRFN 440

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 11
 NASA - NA
 DLA - CC

Preparing activity:
 DLA - CC
 (Project 5961-2768)

Review activities:
 Army - MI, SM
 Navy - AS, MC
 Air Force - 19

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

INSTRUCTIONS

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2. The submitter of this form must complete blocks 4, 5, 6, and 7.
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I RECOMMEND A CHANGE:	1. DOCUMENT NUMBER MIL-PRF-19500/596F	2. DOCUMENT DATE 1 October 2003
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3. DOCUMENT TITLE
SEMICONDUCTOR DEVICE, REPETITIVE AVALANCHE, FIELD EFFECT, TRANSISTOR, N-CHANNEL, SILICON, TYPES 2N7218, 2N7219, 2N7221, 2N7222, 2N7218U, 2N7219U, 2N7221U, 2N7222U, JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

4. NATURE OF CHANGE (Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)

5. REASON FOR RECOMMENDATION

6. SUBMITTER

a. NAME (Last, First, Middle initial)	b. ORGANIZATION		
c. ADDRESS (Include Zip Code)	d. TELEPHONE (Include Area Code)	7. DATE SUBMITTED	
	COMMERCIAL DSN FAX EMAIL		

8. PREPARING ACTIVITY

a. Point of Contact Alan Barone	b. TELEPHONE Commercial DSN FAX EMAIL 614-692-0510 850-0510 614-692-6939 alan.barone@dla.mil
c. ADDRESS Defense Supply Center Columbus ATTN: DSCC-VAC P.O. Box 3990 Columbus, OH 43216-5000	IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT: Defense Standardization Program Office (DLSC-LM) 8725 John J. Kingman, Suite 2533 Fort Belvoir, VA 22060-6221 Telephone (703) 767-6888 DSN 427-6888