

The documentation and process conversion measures necessary to comply with this revision shall be completed by 7 February 2004.

INCH-POUND

MIL-PRF-19500/685A
 7 November 2003
 SUPERSEDING
 MIL-PRF-19500/685
 6 October 2000

PERFORMANCE SPECIFICATION

SEMICONDUCTOR DEVICE, FIELD EFFECT RADIATION HARDENED
 TRANSISTOR, N-CHANNEL, SILICON TYPES 2N7475T1, 2N7476T1 AND 2N7477T1
 (TOTAL DOSE AND SINGLE EVENT EFFECTS)
 JANTXVR AND JANSR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for N-Channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistors, with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}). Two levels of product assurance are provided for each device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. See figure 1, (TO-254AA).

* 1.3 Maximum ratings. T_A = +25°C, unless otherwise specified.

Type	P _T (1) T _C = +25°C	P _T T _A = +25°C	V _{DS}	V _{DG}	V _{GS}	I _{D1} (2) (3) T _C =+25°C	I _{D2} (2) T _C = +100°C	I _S	I _{DM} (3)	T _J and T _{STG}
	<u>W</u>	<u>W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A (pk)</u>	<u>°C</u>
2N7475T1	200	3.0	130	130	±20	45	45	45	180	-55
2N7476T1			200	200		45	30.5	45	180	to
2N7477T1			250	250		40.5	25.5	40.5	162	+150

- (1) Derate linearly 1.67 W/°C for T_C > +25°C;
- (2) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal wires and may be limited by pin diameter:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$
- (3) See figure 2, maximum drain current graph.
- (4) I_{DM} = 4 X I_{D1} as calculated in note (2).

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Defense Supply Center, Columbus, ATTN: DSCC-VAC, Post Office Box 3990, Columbus, OH 43216-5000, by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Primary electrical characteristics at $T_C = +25^\circ\text{C}$.

Type	Min $V_{(BR)DSS}$ $V_{GS} = 0$ $I_D = 1.0\text{mA}$ dc	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ $I_D = 1.0\text{ mA dc}$	Max I_{DSS1} $V_{GS} = 0$ $V_{DS} = 80\%$ of rated V_{DS}	Max $r_{DS(on)}$ (1) $V_{GS} = 12\text{V}, I_D = I_{D2}$		$R_{\theta JC}$ Max	E_{AS}
				$T_J = +25^\circ\text{C}$	$T_J = +150^\circ\text{C}$		
	<u>V dc</u>	<u>V dc</u> Min Max	<u>$\mu\text{A dc}$</u>	<u>Ω</u>	<u>Ω</u>	<u>$^\circ\text{C/W}$</u>	<u>mJ</u>
2N7475T1	130	2.5 4.5	10	0.0145	0.029	0.60	363
2N7476T1	200	2.5 4.5	10	0.039	0.085	0.60	500
2N7477T1	250	2.5 4.5	10	0.061	0.134	0.60	500

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

DEPARTMENT OF DEFENSE

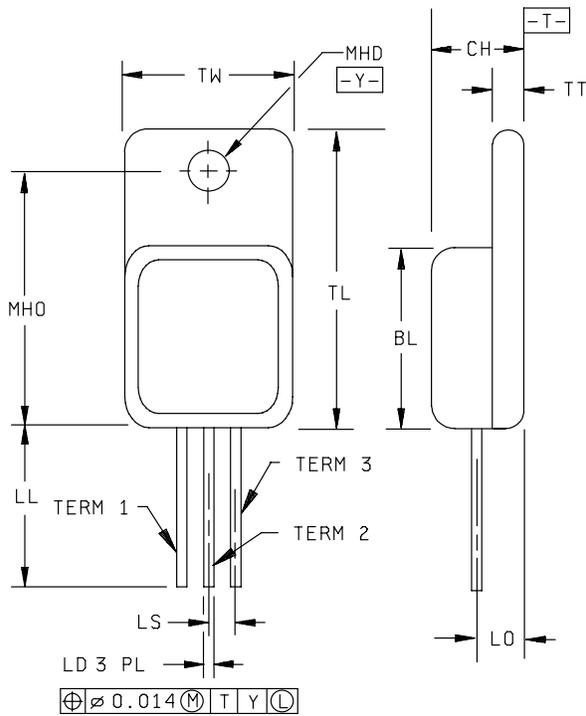
MIL-PRF-19500 - Semiconductor Devices, General Specification for.

STANDARD

DEPARTMENT OF DEFENSE

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from the Document Automation and Production Services (DAPS), Building 4D (NPM-DODSSP), 700 Robbins Avenue, Philadelphia, PA 19111-5094.)



Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.535	.545	13.59	13.89
CH	.249	.260	6.32	6.60
LD	.035	.045	0.89	1.14
LL	.510	.570	12.95	14.48
LO	.150 BSC		3.81 BSC	
LS	.150 BSC		3.81 BSC	
MHD	.139	.149	3.53	3.78
MHO	.665	.685	16.89	17.40
TL	.790	.800	20.07	20.32
TT	.040	.050	1.02	1.27
TW	.535	.545	13.59	13.89
Term 1	Drain			
Term 2	Source			
Term 3	Gate			

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from case.

* FIGURE 1. Dimensions and configuration (TO-254AA).

3. REQUIREMENTS

* 3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500, and figure 1 (TO-254AA) herein. Methods used for electrical isolation of the terminals shall employ materials that contain a minimum of 90 percent Al₂O₃ (ceramic).

3.4.1 Lead finish. Unless otherwise specified, lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking may be omitted from the body, but shall be retained on the initial container.

3.6 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.6.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.6).

- a. Devices should be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq$ or 100 k Ω , whenever bias voltage is applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3 and 1.4 herein.

3.8 Electrical test requirements. The electrical test requirements shall be the subgroups as specified in table I herein.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

* 4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein. Alternate flow is allowed for qualification inspection in accordance with figure 4 of MIL-PRF-19500.

* 4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the associated specification that did not request the performance of table III tests, the tests specified in table III herein shall be performed by the first inspection lot of this revision to maintain qualification.

* 4.2.1.1 SEE. Design capability shall be tested on the initial qualification and thereafter whenever a major die design or process change is introduced. End-point measurements shall be in accordance with table III.

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* 4.3 Screening (JANS and JANTXV). Screening shall be in accordance with table IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS	JANTXV
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, (see 4.3.2), E _{AS} test	Method 3470 of MIL-STD-750, (see 4.3.2), E _{AS} test
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)
9	Subgroup 2 of table I herein I _{DSS1} , I _{GSSF1} , I _{GSSR1} , as a minimum	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(ON)} , V _{GS(TH)} Subgroup 2 of table I herein. ΔI _{GSSF1} = ±20 nA dc or ±100% of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100% of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100% of initial value, whichever is greater.	I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(ON)} , V _{GS(TH)} Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein ΔI _{GSSF1} = ±20 nA dc or ±100% of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100% of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100% of initial value, whichever is greater. Δr _{DS(ON)1} = ±20% of initial value. ΔV _{GS(TH)1} = ±20% of initial value.	Subgroups 2 and 3 of table I herein ΔI _{GSSF1} = ±20 nA dc or ±100% of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100% of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100% of initial value, whichever is greater. Δr _{DS(ON)1} = ±20% of initial value. ΔV _{GS(TH)1} = ±20% of initial value.

- (1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1} and V_{GS(th)1} shall be invoked.
- (3) Shall be performed anytime before screen 9.

* 4.3.1 Gate stress test. Apply $V_{GS} = -24$ V minimum for $t = 250$ μ s minimum.

* 4.3.2 Single pulse avalanche energy (E_{AS}).

- a. Peak current, $I_{AS} = I_{D1}$.
- b. Inductance, $L = (2 \cdot E_{AS} / (I_{D1})^2) \cdot ((V_{BR} - V_{DD}) / V_{BR})$ mH minimum.
- c. Gate to source resistor, R_{GS} : $25 \Omega \leq R_{GS} \leq 200 \Omega$.
- d. Supply voltage, $V_{DD} = \text{Rated } V_{DS}$.
- e. Initial case temperature, $T_C = +25^\circ \text{C}, -5^\circ \text{C}, +10^\circ \text{C}$.
- f. Gate voltage, $V_{GS} = 12$ V dc.
- g. Number of pulses to be applied: 1 pulse minimum.

* 4.3.3 Thermal impedance ($Z_{\theta JC}$ measurement). The $Z_{\theta JC}$ measurement (or equivalent ΔV_{SD} measurement) shall be performed in accordance with method 3161 of MIL-STD-750. The maximum limit (not to exceed figure 3, thermal impedance curves and the table I, subgroup 2 limits) for $Z_{\theta JC}$ in screening (table IV of MIL-PRF-19500) shall be derived by each vendor by means of statistical process control. When the process has exhibited control and capability, the capability data shall be used to establish the fixed limit. In addition to screening, once a fixed limit has been established, monitor all future sealing lots using a random five piece sample from each lot, to be plotted on the applicable X bar R chart. If a lot exhibits an out of control condition, the entire lot shall be removed from the line and held for engineering evaluation and disposition. This procedure may be used in lieu of an in line process monitor.

- a. Measuring current (I_M) 10 mA.
- b. Drain heating current (I_H) 13.33 A.
- c. Heating time (t_H) 100 ms.
- d. Drain-source heating voltage (V_H) 15 V.
- e. Measurement time delay (t_{MD}) 30 - 60 μ s.
- f. Sample window time (t_{SW}) 10 μ s maximum.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein. Alternate flow is allowed for conformance inspection in accordance with figure 4 of MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table V of MIL-PRF-19500 and table I herein.

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* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VIa (JANS) and table VIb (JANTXV) of MIL-PRF-19500, and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

* 4.4.2.1 Group B inspection, table VIa (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition G, 100 cycles.
B3	2077	SEM.
B4	1042	Intermittent operation life, condition D, 2,000 cycles. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, $V_{GS} = \text{rated}$; $T_A = +175^\circ\text{C}$, $t = 24$ hours minimum; or $T_A = +150^\circ\text{C}$, $t = 48$ hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, $V_{DS} = \text{rated}$; $T_A = +175^\circ\text{C}$, $t = 120$ hours minimum; or $T_A = +150^\circ\text{C}$, $t = 240$ hours minimum.
B5	2037	Bond strength, test condition A.
B6	3161	Thermal resistance, see 4.5.2.

* 4.4.2.2 Group B inspection, table VIb (JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G, 25 cycles.
B3	1042	Intermittent operation life, condition D, 2,000 cycles. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.
B3	2037	Test condition A. All internal bond wires for each device shall be pulled separately.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition A; weight = 10 pounds, $t = 10$ s
C5	3161	Thermal resistance, see 4.5.2.
C6	1042	Intermittent operation life, condition D, 2,000 cycles. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table VIII of MIL-PRF-19500 and table II herein.

* 4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

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* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal Impedance 2/	3161	See 4.3.3	$Z_{\theta JC}$		0.45	°C/W
Breakdown voltage drain to source 2N7475T1 2N7476T1 2N7477T1	3407	$V_{GS} = 0V$, $I_D = 1$ mA dc, bias condition C	$V_{(BR)DSS}$	130 200 250		V dc V dc V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1$ mA dc	$V_{GS(TH)1}$	2.5	4.5	V dc
Gate current	3411	$V_{GS} = \pm 20V$ dc, bias condition C, $V_{DS} = 0V$	I_{GSS1}		±100	nA dc
Drain current	3413	$V_{GS} = 0V$ dc, bias condition C, $V_{DS} = 80\%$ of rated V_{DS} ,	I_{DSS1}		10	μA dc
Static drain to source "ON" state resistance 2N7475T1 2N7476T1 2N7477T1	3421	$V_{GS} = 12V$ dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)1}$		0.0145 0.039 0.061	Ω Ω Ω
Forward voltage 2N7475T1 2N7476T1 2N7477T1	4011	$V_{GS} = 0V$ dc, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	V_{SD}		1.2 1.2 1.2	V dc V dc V dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 3</u>						
High temperature operation						
Gate current	3411	$T_C = T_J = +125^\circ\text{C}$ $V_{GS} = \pm 20\text{V dc}$, bias condition C, $V_{DS} = 0\text{V}$	I_{GSS2}		± 200	nA dc
Drain current	3413	$V_{GS} = 0\text{V dc}$, bias condition C, $V_{DS} = 80\%$ of rated V_{DS}	I_{DSS2}		25	$\mu\text{A dc}$
Static drain to source "ON"-state resistance 2N7475T1 2N7476T1 2N7477T1	3421	$V_{GS} = 12\text{V dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)3}$		0.029 0.085 0.134	Ω Ω Ω
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1\text{ mA dc}$	$V_{GS(TH)2}$	1.5		V dc
Low temperature operation						
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS(TH)3}$, $I_D = 1\text{ mA dc}$	$V_{GS(TH)3}$		5.5	V dc
<u>Subgroup 4</u>						
Forward transconductance 2N7475T1 2N7476T1 2N7477T1	3475	$I_D = I_{D2}$, $V_{DD} = 15\text{ V dc}$ (see 4.5.1)	g_{FS}		39 35 27	S S S
Switching time test	3472	$I_D = I_{D1}$, $V_{GS} = 12\text{ V dc}$; $R_G = 2.35\ \Omega$, $V_{DD} = 50\%$ percent of rated V_{DS}				
Turn-on delay time			$t_{D(on)}$		35	ns
Rise time			t_r		125	ns
Turn-off delay time			$t_{D(off)}$		80	ns
Fall time 2N7475T1 2N7476T1 2N7477T1			t_f		65 50 65	ns ns ns

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit			
	Method	Condition		Min	Max				
<u>Subgroup 5</u> Safe operating area test (high voltage)	3474	See figures 4, 5 and 6 $t_p = 10$ ms min. $V_{DS} = 80$ percent of max. rated V_{DS}							
Electrical measurements									
<u>Subgroup 6</u> Not applicable									
<u>Subgroup 7</u> Gate charge	3471	Condition B $I_D = I_{D1}$							
On-state gate charge 2N7475T1							$Q_{G(ON)}$	160	nC
2N7476T1								155	nC
2N7477T1								165	nC
Gate to source charge 2N7475T1							Q_{GS}	55	nC
2N7476T1								45	nC
2N7477T1								45	nC
Gate to drain charge 2N7475T1							Q_{GD}	75	nC
2N7476T1								75	nC
2N7477T1								75	nC
Reverse recovery time	3473	$di/dt = -100$ A/ μ s, $V_{DD} \leq 50$ V $I_D = I_{D1}$							
2N7475T1							t_{rr}	300	ns
2N7476T1								450	ns
2N7477T1								775	ns

1/ For sampling plan, see MIL-PRF-19500.

2/ This test is required for the following end-point measurement only (not intended for screen 9, 11, or 13): JANS, table VIa of MIL-PRF-19500, group B, subgroups 3 and 4; JANTXV, table VIb of MIL-PRF-19500, group B, subgroups 2 and 3; and table VII of MIL-PRF-19500, group C, subgroup 6, and table IX of MIL-PRF-19500, group E, subgroup 1.

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* TABLE II. Group D inspection.

Inspection 1/ 2/ 3/ 4/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Unit
	Method	Conditions		R		R		
				Min	Max	Min	Max	
Subgroup 1 Not applicable								
Subgroup 2 Steady-state total dose irradiation (VGS bias) 5/	1019	T _C = + 25°C V _{GS} = 12 V; V _{DS} = 0 V						
Steady-state total dose irradiation (VDS bias) 5/	1019	V _{GS} = 0 V; V _{DS} = 80 percent of rated V _{DS} (preirradiation)						
End-point electricals Breakdown voltage, drain to source	3407	V _{GS} = 0 V; I _D = 1 mA; bias condition C	V _{(BR)DSS}					
2N7475T1				130		130		V dc
2N7476T1				200		200		V dc
2N7477T1				250		250		V dc
Gate to source voltage (threshold)	3403	V _{DS} ≥ V _{GS} I _D = 1 mA	V _{GS(th)1}	2.5	4.5	2.0	4.5	V dc
Gate current	3411	V _{GS} = +20 V, V _{DS} = 0 V bias condition C	I _{GSSF1}		100		100	nA dc
Gate current	3411	V _{GS} = -20 V V _{DS} = 0 V bias condition C	I _{GSSR1}		-100		-100	nA dc
Drain current	3413	V _{GS} = 0 V V _{DS} = 80 percent of rated V _{DS} (preirradiation) bias condition C	I _{DSS}		10		10	μA dc
Static drain to source on-state voltage	3405	V _{GS} = 12 V; condition A, pulsed (see 4.5.1)	V _{DS(on)}					
2N7475T1		I _D = 45			0.675		0.675	V dc
2N7476T1		I _D = 35			1.365		1.365	V dc
2N7477T1		I _D = 26			1.586		1.586	V dc
Forward voltage source drain diode	4011	V _{GS} = 0 V, I _D = I _{D1} bias condition C	V _{SD}					
2N7475T1		I _D = 45			1.2		1.2	V dc
2N7476T1		I _D = 45			1.2		1.2	V dc
2N7477T1		I _D = 40			1.2		1.2	V dc

1/ For sampling plan see MIL-PRF-19500.

2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification utilizing the same die design.

3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in it's qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

4/ The R designation represents devices which pass endpoints at 100K rads (Si).

5/ Separate samples shall be pulled for each bias.

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* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification inspection
	Method	Conditions	
<u>Subgroup 1</u>			12 devices c = 0
Temperature cycle	1051	Condition G, 500 cycles	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2	12 devices c = 0
<u>Subgroup 2 1/</u>			
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state reverse bias	1042	Condition A, 1,000 hours	3 devices, c = 0
Electrical measurements		See table I, subgroup 2	
<u>Subgroup 3</u>			
DPA	2102		sample size N/A
<u>Subgroup 4</u>			
Thermal impedance curves		Each supplier shall submit their (typical) design thermal impedance curves. In addition, test conditions and $Z_{\theta JX}$ limit shall be provided to the qualifying activity in the qualification report	
<u>Subgroup 5</u>			3 devices
Not applicable			
<u>Subgroup 6</u>			22 devices c = 0
ESD	1020	Not required for devices classified as ESD class 1.	
<u>Subgroup 7</u>			
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476		

See footnotes at end of table.

* TABLE III. Group E inspection (all quality levels) for or re-qualification qualification only - Continued.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection	
	Method	Conditions		
<u>Subgroup 7</u> - Continued			3 devices	
Single Event Effects (SEE) <u>2/ 3/ 4/</u>	1080	I_{GSS1} and I_{DSS1} per table I, subgroup 2 Fluence = $3E5 \pm 20\%$ ions/cm ² Flux = 2E3 to 2E4 ions/cm ² /sec, temperature = 25 ± 5 °C LET = 37 MeV-cm ² /mg, Range = 39 microns, Energy = 305 MeV Insitu bias conditions: $V_{DS} = 130V$ & $V_{GS} = -20V$ Insitu bias conditions: $V_{DS} = 200V$ & $V_{GS} = -20V$ Insitu bias conditions: $V_{DS} = 250V$ & $V_{GS} = -20V$ LET = 60 MeV-cm ² /mg, Range = 32 microns, Energy = 340 MeV Insitu bias conditions: $V_{DS} = 130V$ & $V_{GS} = -10V$ $V_{DS} = 100V$ & $V_{GS} = -15V$ $V_{DS} = 50V$ & $V_{GS} = -20V$ Insitu bias conditions: $V_{DS} = 200V$ & $V_{GS} = -10V$ $V_{DS} = 185V$ & $V_{GS} = -15V$ $V_{DS} = 120V$ & $V_{GS} = -20V$ Insitu bias conditions: $V_{DS} = 250V$ & $V_{GS} = -15V$ $V_{DS} = 240V$ & $V_{GS} = -20V$ LET = 82 MeV-cm ² /mg, Range = 28 microns, Energy = 350 MeV Insitu bias conditions: $V_{DS} = 130V$ & $V_{GS} = 0V$ $V_{DS} = 120V$ & $V_{GS} = -5V$ $V_{DS} = 30V$ & $V_{GS} = -10V$ Insitu bias conditions: $V_{DS} = 200V$ & $V_{GS} = -5V$ $V_{DS} = 150V$ & $V_{GS} = -10V$ $V_{DS} = 50V$ & $V_{GS} = -15V$ $V_{DS} = 25V$ & $V_{GS} = -20V$ Insitu bias conditions: $V_{DS} = 250V$ & $V_{GS} = -5V$ $V_{DS} = 225V$ & $V_{GS} = -10V$ $V_{DS} = 175V$ & $V_{GS} = -15V$ $V_{DS} = 50V$ & $V_{GS} = -20V$		
Electrical measurements <u>5/</u>				
SEE irradiation				
2N7475T1				
2N7476T1				
2N7477T1				
2N7475T1				
2N7476T1				
2N7477T1				
2N7475T1				
2N7476T1				
2N7477T1				
Electrical measurements <u>5/</u>		I_{GSS1} and I_{DSS1} in accordance with table I, subgroup 2		

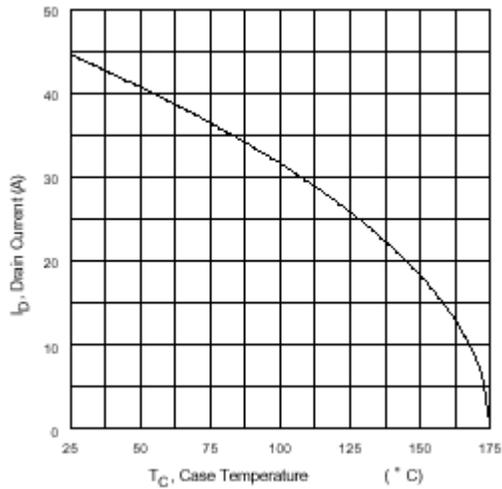
1/ A separate sample for each test shall be pulled.

2/ Group E qualification of SEE testing may be performed prior to lot formation. Qualification may be extended to other performance specifications utilizing the same structurally identical die design.

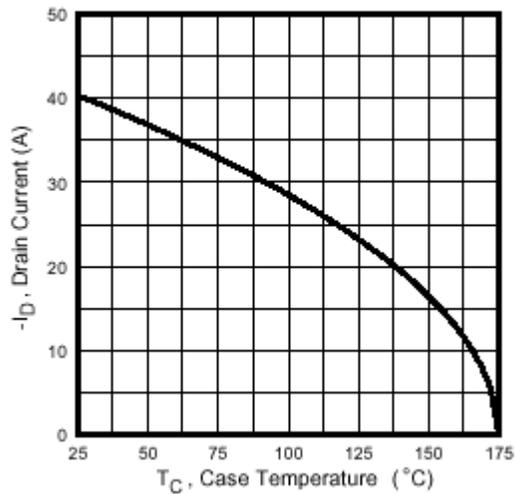
3/ Device qualification to a higher level LET is sufficient to qualify all lower level LET's.

4/ The sampling plan applies to each bias condition.

5/ Examine I_{GSS1} and I_{DSS1} before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.

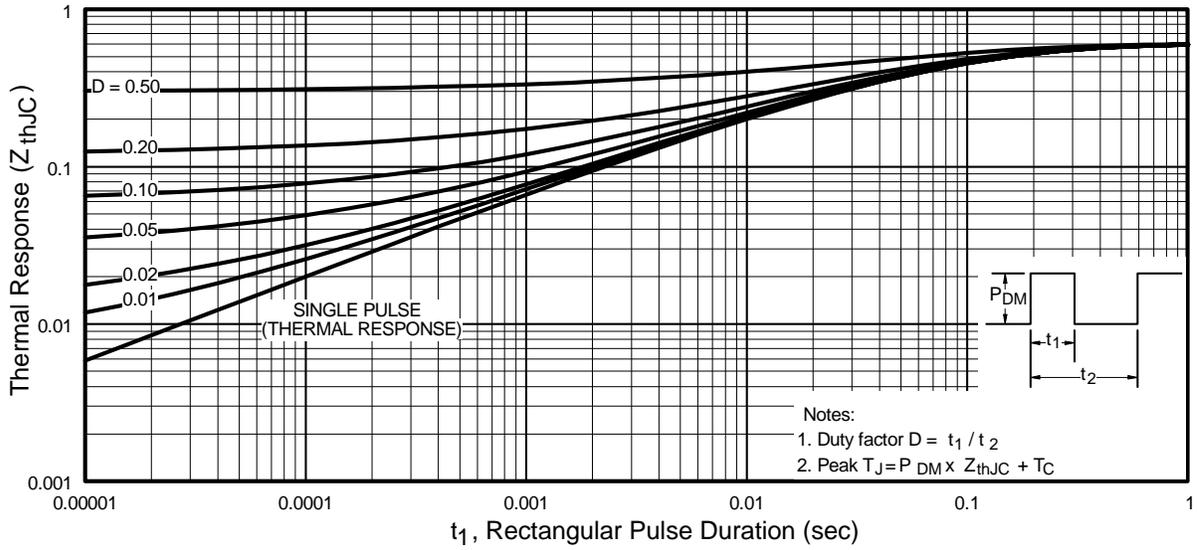


2N7475T1 and 2N7476T1

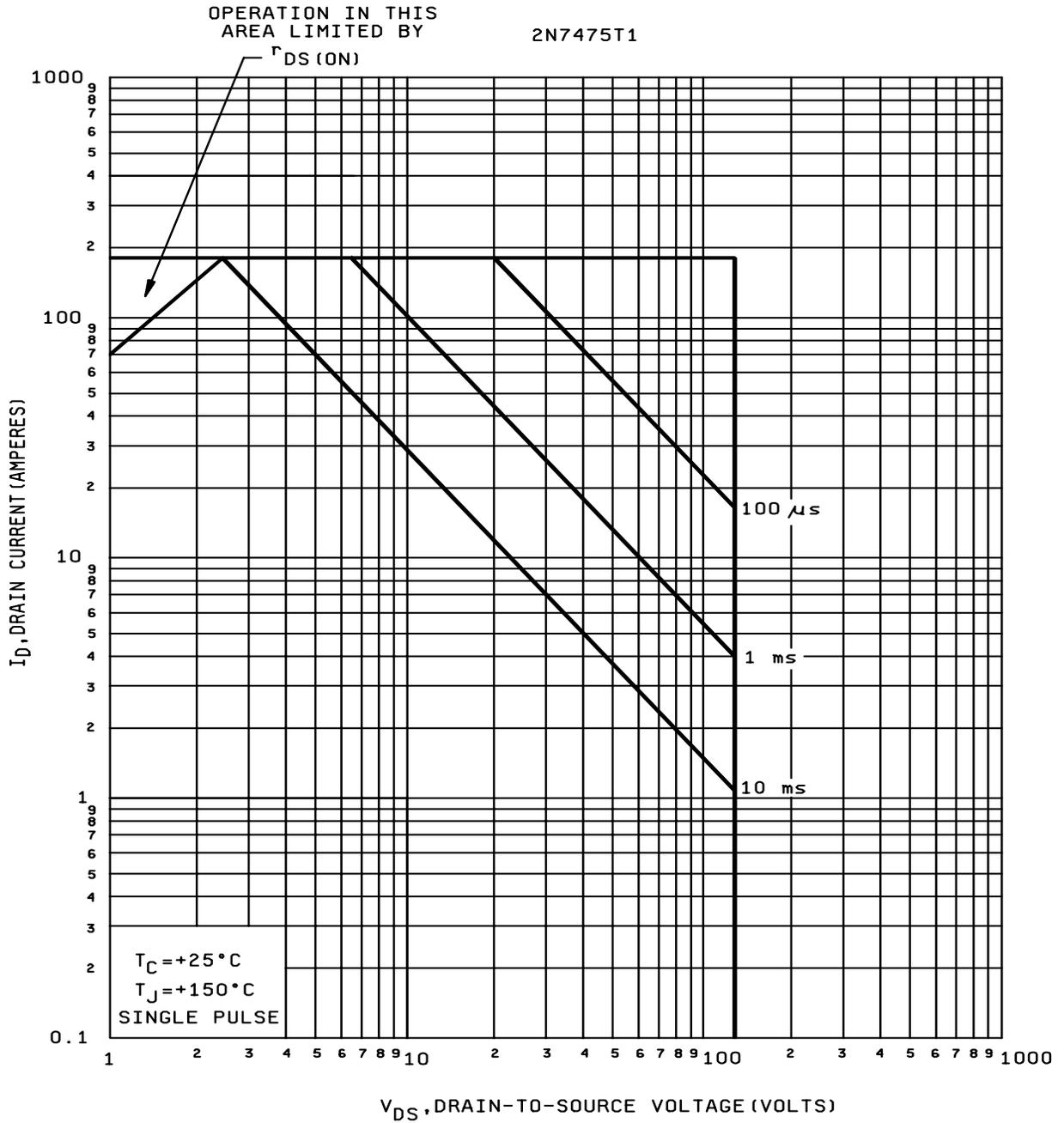


2N7477T1

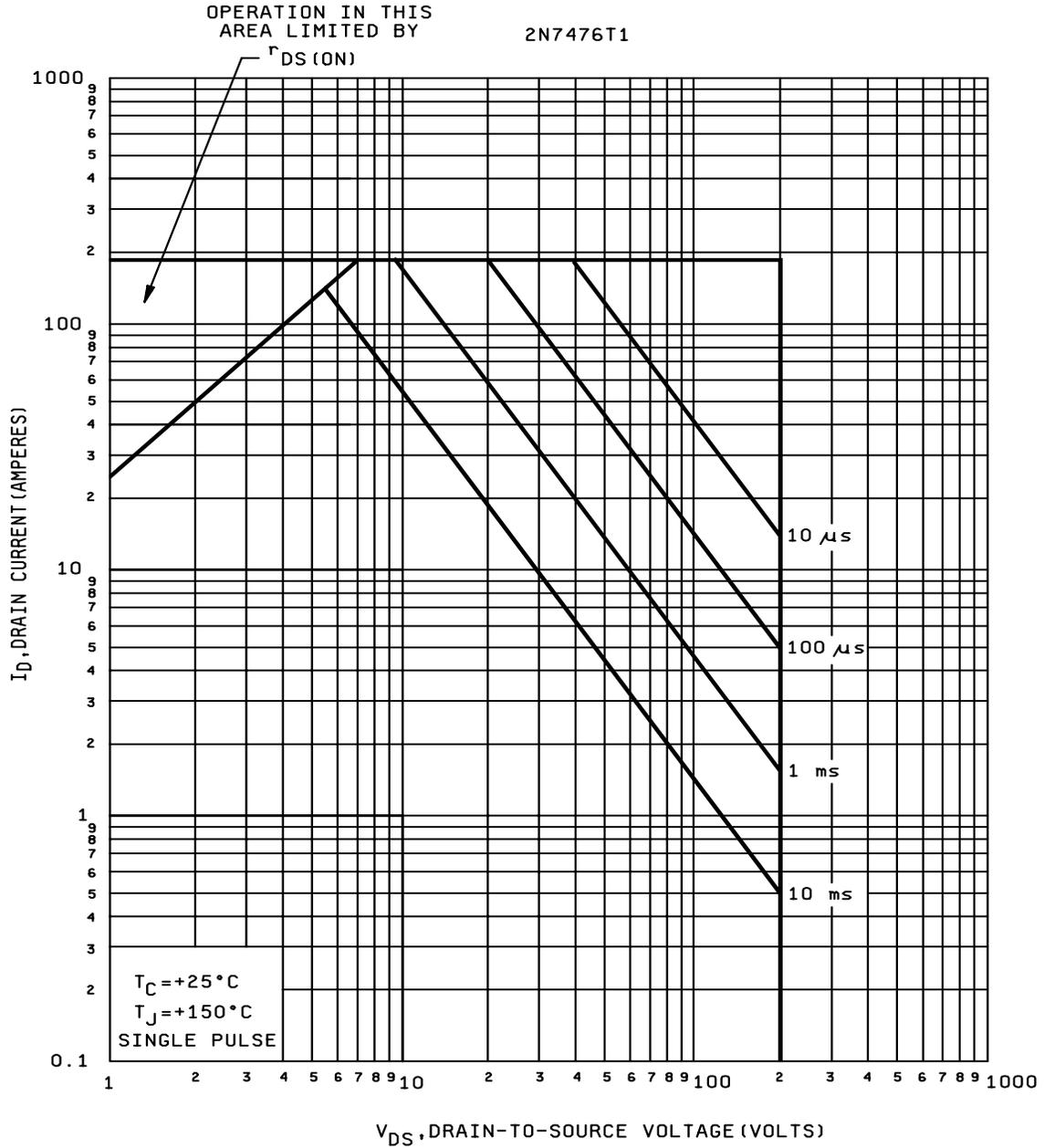
* FIGURE 2. Maximum drain current vs case temperature graphs.



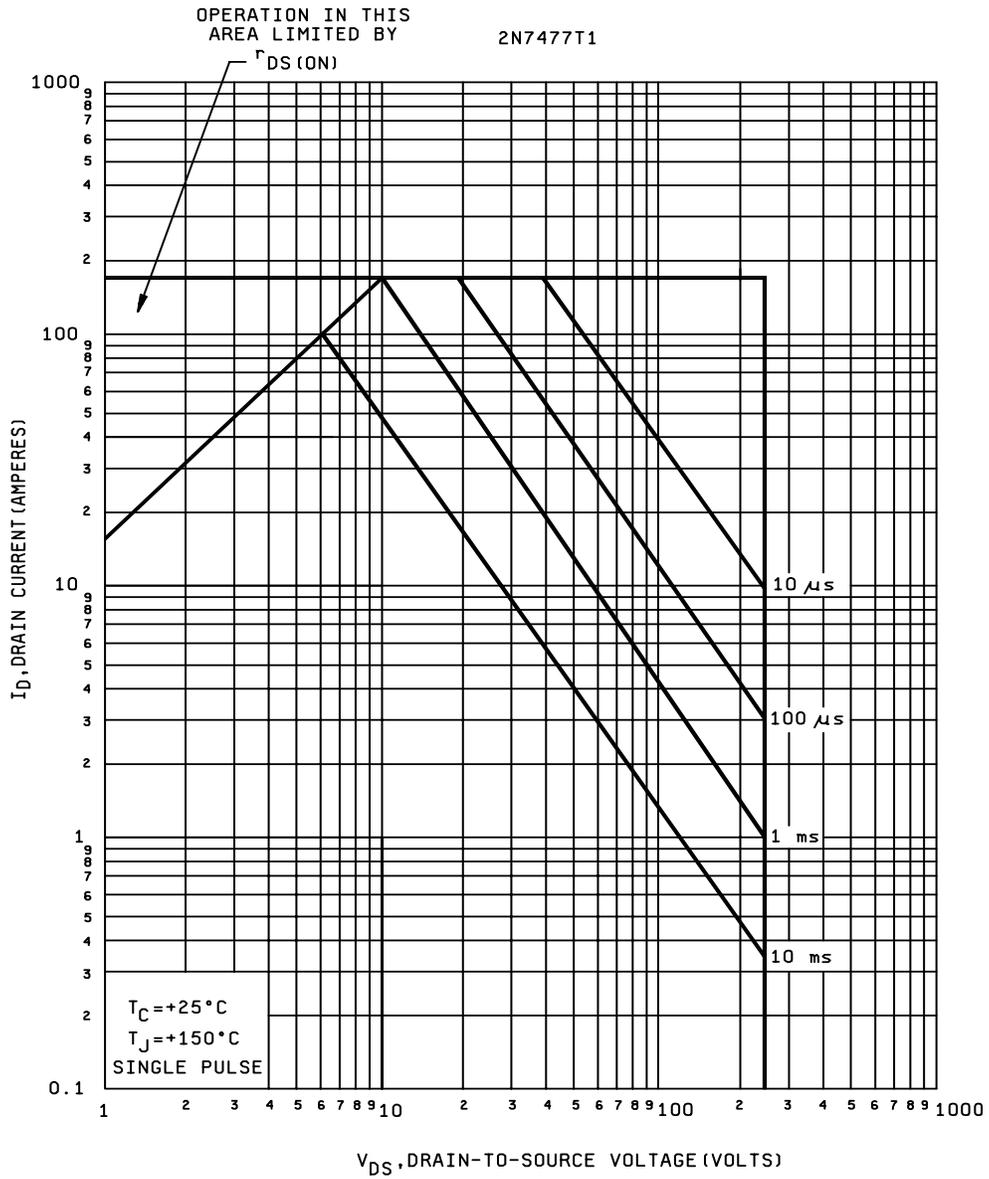
* FIGURE 3. Thermal response curve.



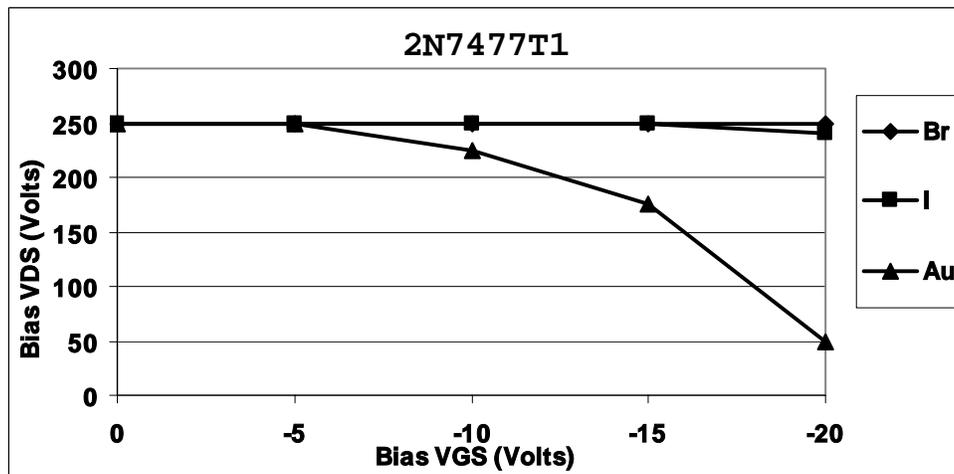
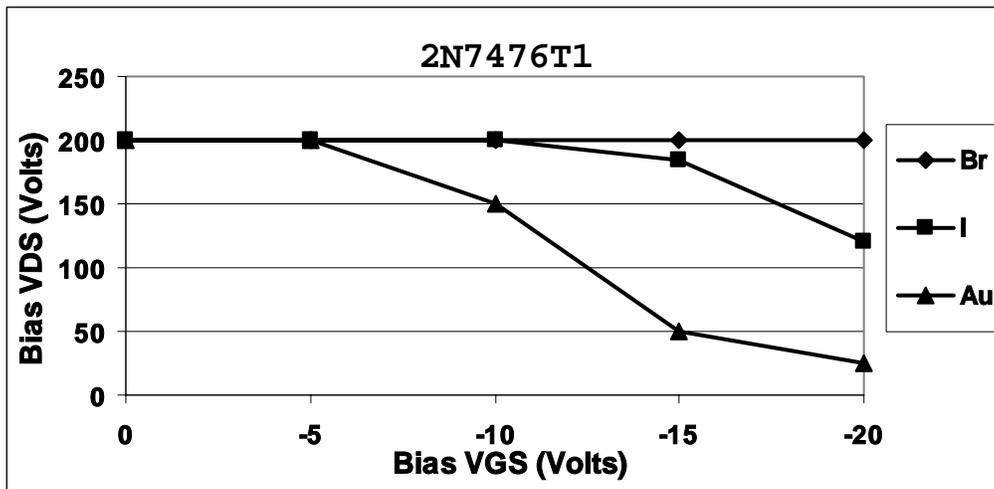
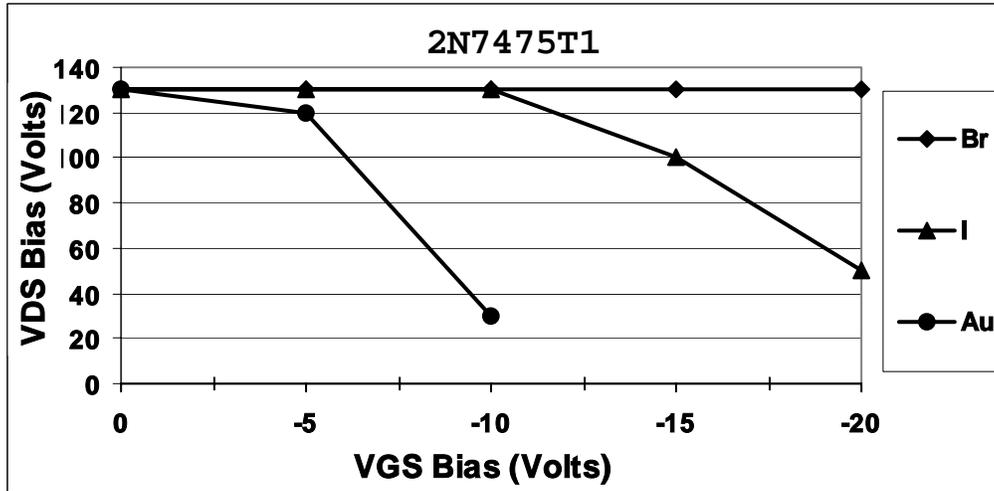
* FIGURE 4. Safe operating area graph.



* FIGURE 5. Safe operating area graph.



* FIGURE 6. Safe operating area graph.



* FIGURE 7. SEE safe operating area graph.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal resistance. Thermal resistance measurements shall be performed in accordance with method 3161 of MIL-STD-750. The maximum limit of $R_{\theta JC} = 0.60 \text{ }^{\circ}\text{C/W}$. The following parameters shall apply:

- a. Measuring current (I_M)..... 10 mA.
- b. Drain heating current (I_H) 11.11 A.
- c. Heating time (t_H)..... Steady-state (see method 3161 of MIL-STD-750).
- d. Drain-source heating voltage (V_H)..... 12 V.
- e. Measurement time delay (t_{MD})..... 30 to 60 μs .
- f. Sample window time (t_{SW})..... 10 μs maximum.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Points' packaging activity within the Military Department or Defense Agency, or within the Military Departments' System Command. Packaging data retrieval is available from the managing Military Departments' or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Issue of DODISS to be cited in the solicitation and, if required, the specific issue of individual documents referenced (see 2.2.1).
- c. Packaging requirements (see 5.1).
- d. Lead finish (see 3.4.1).
- e. Type designation and product assurance level.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-19500 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC-VQE, P.O. Box 3990, Columbus, OH 43216-5000.

6.4 Cross-reference list. The following table shows the generic P/N and its associated military P/N (without JAN and RHA prefix).

Generic P/N	Military P/N
IRHMS57163SE	2N7475T1
IRHMS57260SE	2N7476T1
IRHMS57264SE	2N7477T1

* 6.5 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 11
 NASA - NA
 DLA - CC

Preparing activity:
 DLA - CC
 (Project 5961-2834)

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I RECOMMEND A CHANGE:	1. DOCUMENT NUMBER MIL-PRF-19500/685A	2. DOCUMENT DATE 7 November 2003
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3. DOCUMENT TITLE
SEMICONDUCTOR DEVICE, FIELD EFFECT RADIATION HARDENED (TOTAL DOSE & SINGLE EVENT EFFECTS) TRANSISTOR, N-CHANNEL SILICON TYPES 2N7475T1, 2N7476T1 AND 2N7477T1 JANTXVR AND JANSR.

4. NATURE OF CHANGE (Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)

5. REASON FOR RECOMMENDATION

6. SUBMITTER

a. NAME (Last, First, Middle initial)	b. ORGANIZATION	
c. ADDRESS (Include Zip Code)	d. TELEPHONE (Include Area Code) COMMERCIAL DSN FAX EMAIL	7. DATE SUBMITTED

8. PREPARING ACTIVITY

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c. ADDRESS Defense Supply Center, Columbus ATTN: DSCC-VAC P.O. Box 3990 Columbus, OH 43216-5000	IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT: Defense Standardization Program Office (DLSC-LM) 8725 John J. Kingman, Suite 2533 Fort Belvoir, VA 22060-6221 Telephone (703) 767-6888 DSN 427-6888		