

The documentation and process conversion measures necessary to comply with this document shall be completed by 30 September 2004.

INCH-POUND

MIL-PRF-19500/728  
30 June 2004

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON, SWITCHING,  
TYPES 2N3724, 2N3724L, 2N3724UB, 2N3725, 2N3725L, 2N3725UB,  
JAN, JANS, JANTX, AND JANTXV

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN, silicon, switching transistors. Four levels of product assurance are provided for each device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. See figure 1 (TO-5 and TO-39), figure 2 (UB), and figure 3 (JANHC and JANKC).

1.3 Maximum ratings.

Types	$I_C$ mA dc	$V_{CBO}$ V dc	$V_{CEO}$ V dc	$V_{EBO}$ V dc	$T_J$ and $T_{STG}$ °C
2N3724, L, UB	500	50	30	6.0	-65 to +200
2N3725, L, UB	500	80	50	6.0	-65 to +200

Types	$P_T$ $T_A = +25^\circ\text{C}$ (1) (2) W	$P_T$ $T_C = +25^\circ\text{C}$ (1) (2) W	$P_T$ $T_{SP(IS)} = +25^\circ\text{C}$ (1) (2) W	$R_{\theta JA}$ (2) (3) °C/W	$R_{\theta JC}$ (2) (3) °C/W	$R_{\theta JSP(IS)}$ (2) (3) (4) °C/W
2N3724	0.800	5	N/A	175	35	N/A
2N3725	0.800	5	N/A	175	35	N/A
2N3724L	0.800	5	N/A	175	35	N/A
2N3725L	0.800	5	N/A	175	35	N/A
2N3724UB	0.500	N/A	1.5	325	N/A	90
2N3725UB	0.500	N/A	1.5	325	N/A	90

(1) For derating, see figures 4, 5, 6, and 7.

(2) See 3.3.

(3) For thermal impedance curves, see figures 8, 9, 10, and 11.

(4) For non-thermal conductive PCB or unknown PCB surface mount conditions in free air, substitute figures 7 and 10 for the UB package and use  $R_{\theta JA}$ .

Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [Semiconductor@dsc.dla.mil](mailto:Semiconductor@dsc.dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://www.dodssp.daps.mil/>.

1.4 Primary electrical characteristics at  $T_A = +25^\circ\text{C}$ .

Types	$h_{FE1}$ $I_C = 10 \text{ mA dc}$ $V_{CE} = 5 \text{ V dc}$		$h_{FE2}$ $I_C = 1 \text{ A dc}$ $V_{CE} = 5 \text{ V dc}$		$h_{FE3}$ $I_C = 100 \text{ mA dc}$ $V_{CE} = 1.0 \text{ V dc}$		/hfe/ $f = 100 \text{ MHz}$ $V_{CE} = 10 \text{ V dc}$ $I_C = 50 \text{ mA dc}$		$C_{obo}$ $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$ $V_{CB} = 10 \text{ V dc}$ $I_E = 0$	
	Min	Max	Min	Max	Min	Max	Min	Max	Min pF	Max pF
2N3724, L	30		25		60	150	3.0		12	
2N3724UB	30		25		60	150	3.0		12	
2N3725, L	30		25		60	150	3.0		12	
2N3725UB	30		25		60	150	3.0		12	

Types	$V_{CE(sat)1}$ (1) $I_C = 100 \text{ mA dc}$ $I_B = 10 \text{ mA dc}$		$V_{CE(sat)2}$ (1) $I_C = 10 \text{ mA dc}$ $I_B = 1.0 \text{ A dc}$		$V_{BE(sat)1}$ (1) $I_C = 10 \text{ mA dc}$ $I_B = 1.0 \text{ mA dc}$		$V_{BE(sat)2}$ (1) $I_C = 1.0 \text{ A dc}$ $I_B = 100 \text{ mA dc}$		Switching (saturated)			
	$\frac{V \text{ dc}}{\text{Min}}$	$\frac{V \text{ dc}}{\text{Max}}$	$\frac{V \text{ dc}}{\text{Min}}$	$\frac{V \text{ dc}}{\text{Max}}$	$\frac{V \text{ dc}}{\text{Min}}$	$\frac{V \text{ dc}}{\text{Max}}$	$\frac{V \text{ dc}}{\text{Min}}$	$\frac{V \text{ dc}}{\text{Max}}$	ns Min	ns	ns Min	ns
2N3724, L, UB, 2N3725, L, UB	0.95		0.95		0.76		1.7		35		60	
	0.95		0.95		0.76		1.7		35		60	

(1) Pulsed see 4.5.1.

## 2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

## DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

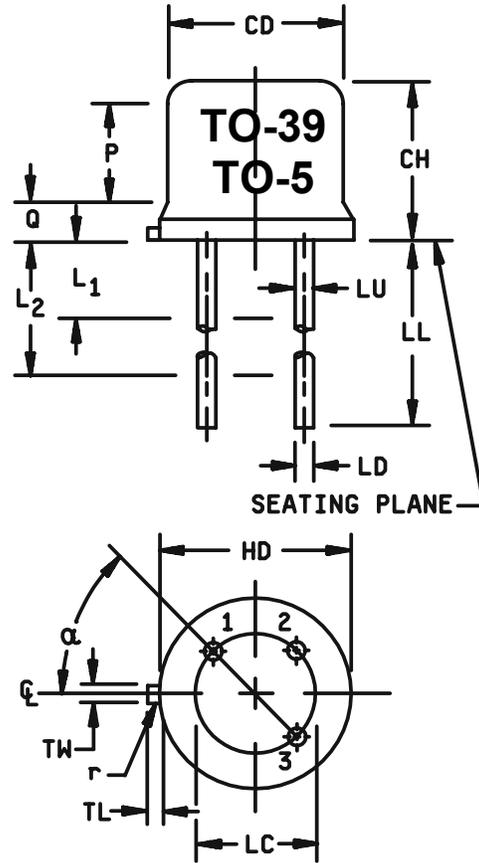
## DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://www.dodssp.daps.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

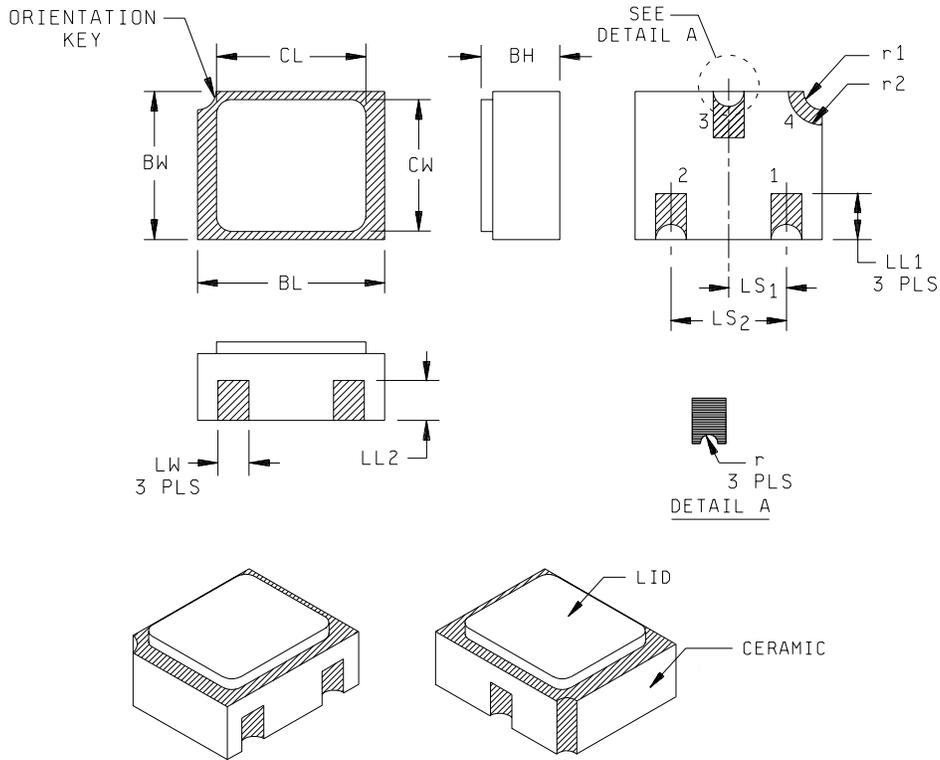
Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.12	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		7
LD	.016	.019	0.41	0.48	8,9
LL	See note 14				
LU	.016	.019	0.41	0.48	8,9
L1		.050		1.27	8,9
L2	.250		6.35		8,9
P	.100		2.54		7
Q		.030		0.76	5
TL	.029	.045	0.74	1.14	3,4
TW	.028	.034	0.71	0.86	3
r		.010		0.25	10
$\alpha$	45° TP		45° TP		7



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
7. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
8. Dimension LU applies between L<sub>1</sub> and L<sub>2</sub>. Dimension LD applies between L<sub>2</sub> and LL minimum. Diameter is uncontrolled in L<sub>1</sub> and beyond LL minimum.
9. All three leads.
10. The collector shall be internally connected to the case.
11. Dimension r (radius) applies to both inside corners of tab.
12. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi$ x symbology.
13. Lead 1 = emitter, lead 2 = base, lead 3 = collector.
14. For L suffix devices (TO-5), dimension LL = 1.5 inches (38.10 mm) min. and 1.75 inches (44.45 mm) max. For non-L suffix types (TO-39), dimension LL = .5 inch (12.70 mm) min. and .750 inch (19.05 mm) max.

FIGURE 1. Physical dimensions for 2N3724, and 2N3725 (TO-5 and TO-39).

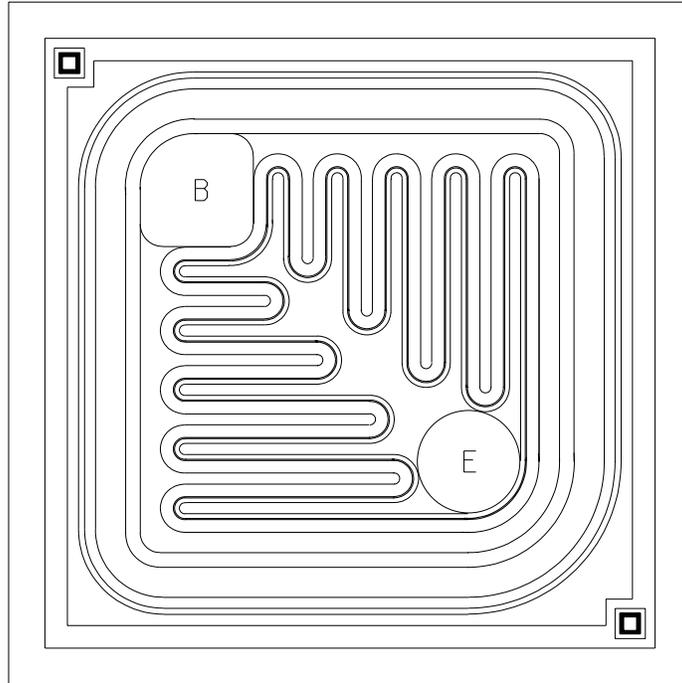


Symbol	Dimensions				Note	Symbol	Dimensions				Note
	Inches		Millimeters				Inches		Millimeters		
	Min	Max	Min	Max			Min	Max	Min	Max	
BH	.046	.056	1.17	1.42		LS1	.035	.039	0.89	0.99	
BL	.115	.128	2.92	3.25		LS2	.071	.079	1.80	2.01	
BW	.085	.108	2.16	2.74		LW	.016	.024	0.41	0.61	
CL	.115	.128	2.92	3.25		r		.008		0.20	
CW	.085	.108	2.16	2.74		r1		.012		0.31	
LL1	.022	.038	0.56	0.96		r2		.022		0.56	
LL2	.017	.035	0.43	0.89							

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi x$  symbology.

FIGURE 2. Physical dimensions, surface mount 2N3724UB and 2N3725UB (UB version).



NOTES:

- |                         |   |
|-------------------------|---|
| 1. Die size:            | .025 x .025 inch $\pm$ .002 inch (0.635 mm x 0.635 mm). |
| 2. Die thickness:       | .010 $\pm$ .0015 inch (0.254 mm $\pm$ 0.0381 mm).       |
| 3. Base bonding pad:    | .004 x .004 inch (0.1016 mm x 0.1016 mm).               |
| 4. Emitter bonding pad: | .004 x .004 inch (0.1016 mm x 0.1016 mm).               |
| 5. Back metal:          | Gold, 5,000 Å.  |
| 6. Top metal:           | Aluminum, 15,000Å minimum, 18,000 Å nominal.            |
| 7. Back side:           | Collector.  |
| 8. Glassivation:        | Si <sub>3</sub> N <sub>4</sub> , 8,000 Å nominal.       |

FIGURE 3. JANHC and JANKC die dimensions.

### 3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figures 1, 2, and 3 herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in paragraph 1.3, 1.4, and table I.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table I, subgroup 2.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500, except for the UB suffix package. Marking on the UB package shall consist of an abbreviated part number, the date code, and the manufacturers symbol or logo. The prefixes JAN, JANTX, JANTXV, and JANS can be abbreviated as J, JX, JV, and JS respectively. The "2N" prefix and the "UB" suffix can also be omitted.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

### 4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table IV MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
2	Optional	Optional
3a 3b 3c	Required Not applicable Thermal impedance (transient), method 3131 of MIL-STD-750 (1)	Required Not applicable Thermal impedance (transient), method 3131 of MIL-STD-750 (1)
4	Required	Optional
5	Required	Not applicable
7a and 7b	Optional	Optional
8	Required	Not required
9	$I_{CB02}$ , $h_{FE4}$	Not applicable
10	48 hours minimum	48 hours minimum
11	$I_{CB02}$ ; $h_{FE4}$ ; $\Delta I_{CB02}$ = 100 percent of initial value or 5 nA dc, whichever is greater. $\Delta h_{FE4}$ = $\pm 15$ percent	$I_{CB02}$ ; $h_{FE4}$
12	See 4.3.2 240 hours minimum	See 4.3.2 80 hours minimum
13	Subgroups 2 and 3 of table I herein; $\Delta I_{CB02}$ = 100 percent of initial value or 5 nA dc, whichever is greater; $\Delta h_{FE4}$ = $\pm 15$ percent	Subgroup 2 of table I herein; $\Delta I_{CB02}$ = 100 percent of initial value or 5 nA dc, whichever is greater; $\Delta h_{FE4}$ = $\pm 15$ percent
14a and 14b	Required	Required
15	Required	Not required
16	Required	Not required

(1) Thermal impedance limits shall not exceed figures 8, 9, 10, and 11.

4.3.2 Power burn-in conditions. Power burn-in conditions are as follows:  $V_{CB}$  = 10 - 30 V dc. Power shall be applied to achieve  $T_J$  = +135°C minimum using a minimum  $P_D$  = 75 percent of  $P_T$  maximum,  $T_A$  ambient rated as defined in 1.3.

4.3.3 Thermal impedance ( $Z_{\theta JX}$  measurements). The  $Z_{\theta JX}$  measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining  $I_M$ ,  $I_H$ ,  $t_H$ ,  $t_{MD}$  (and  $V_C$  where appropriate). The  $Z_{\theta JX}$  limit used in screen 3c shall comply with the thermal impedance graph in figures 8, 9, 10, and 11 (less than or equal to the curve value at the same  $t_H$  time) and/or shall be less than the process determined statistical maximum limit as outlined in method 3131.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of table I, subgroup 1, and 2 inspection only (table VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table VIa (JANS) of MIL-PRF-19500 and 4.4.2.1. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.3 herein: delta requirements only apply to subgroups B4, and B5. See 4.4.2.2 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) and delta requirements for JAN, JANTX, and JANTXV shall be after each step in 4.4.2.2 and shall be in accordance with table I, subgroup 2 and 4.5.3 herein.

4.4.2.1 Group B inspection (JANS), table VIa of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
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B4	1037	$V_{CB} = 10$ V dc.
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B5	1027	$V_{CB} = 10$ V dc; $P_D \geq 100$ percent of maximum rated $P_T$ (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.)
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Option 1: 96 hours minimum sample size in accordance with MIL-PRF-19500, table VIa, adjust  $T_A$  or  $P_D$  to achieve  $T_J = +275^\circ\text{C}$  minimum.

Option 2: 216 hours minimum, sample size = 45,  $c = 0$ ; adjust  $T_A$  or  $P_D$  to achieve a  $T_J = +225^\circ\text{C}$  minimum.

4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot and /or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failure mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

<u>Step</u>	<u>Method</u>	<u>Condition</u>
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1	1027	Steady-state life: Test condition B, 1,000 hours minimum, $V_{CB} = 10$ V dc, power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum using a minimum of $P_D = 75$ percent of maximum rated $P_T$ as defined in 1.3. $n = 45$ devices, $c = 0$ .
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2	1048	HTRB: Test condition A, 48 hours minimum. $n = 45$ devices, $c = 0$ .
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3	1032	High-temperature life (non-operating), $t = 340$ hours, $T_A = +200^\circ\text{C}$ . $n = 22$ , $c = 0$ .
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4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

- a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.
- b. Must be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the test and conditions specified for subgroup testing in table VII of MIL-PRF-19500, and in 4.4.3.1 (JANS) and 4.4.3.2 (JAN, JANJ, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.3 herein; delta requirements only apply to subgroup C6.

4.4.3.1 Group C inspection (JANS), table VII of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E; (not applicable for UB devices).
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3) and applied thermal impedance curves.
C6	1026	Test condition B, 1,000 hours at $V_{CB} = 10$ V dc; power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum and a minimum of $P_D = 75$ percent of maximum rated $P_T$ as defined in 1.3 $n = 45$ , $c = 0$ .

4.4.3.2 Group C inspection (JAN, JANJ, JANTX, and JANTXV), table VII of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E; not applicable for UB devices.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3) and applied thermal impedance curves.
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein. Delta measurements shall be in accordance with the applicable steps of 4.5.3.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Input capacitance. This test shall be conducted in accordance with method 3240 of MIL-STD-750, except the output capacitor shall be omitted.

4.5.3 Delta requirements. Delta requirements shall be as specified below:

Step	Inspection	MIL-STD-750		Symbol	Limit	Unit
		Method	Conditions			
1	Collector-base cutoff current	3036	Bias condition D, $V_{CB} = 60 \text{ V dc}$	$\Delta I_{CB02}$ (1)	100 percent of initial value or 8 nA dc, whichever is greater.	
2	Forward current transfer ratio	3076	$V_{CE} = 10 \text{ V dc};$ $I_C = 150 \text{ mA dc};$ pulsed see 4.5.1	$\Delta h_{FE4}$ (1)	$\pm 25$ percent change from initial reading.	

(1) Devices which exceed the table I limits for this test shall not be accepted.

TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 2/</u>						
Visual and mechanical examination <u>3/</u>	2071	n = 45 devices, c = 0				
Solderability <u>3/ 4/</u>	2026	n = 15 leads, c = 0				
Resistance to solvents <u>3/ 4/ 5/</u>	1022	n = 15 devices, c = 0				
Temp cycling <u>3/ 4/</u>	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Electrical measurements <u>4/</u>		table I, subgroup 2				
Hermetic seal <u>4/ 6/</u> Fine leak Gross leak	1071	n = 22 devices, c = 0				
Bond strength <u>3/ 4/</u>	2037	Precondition T <sub>A</sub> = +250°C at t = 24 hours or T <sub>A</sub> = +300°C at t = 2 hours n = 11 wires, c = 0				
Decap internal visual (design verification) <u>4/</u>	2075	n = 4 devices, c = 0				
<u>Subgroup 2</u>						
Thermal impedance	3131	See 4.3.3	Z <sub>θJX</sub>			°C/W
Collector to base cutoff current	3036	V <sub>CB</sub> = 40 V dc, I <sub>E</sub> = 0 mA dc T <sub>A</sub> = +100°C	I <sub>CBO1</sub>		120	μA dc
Collector to emitter cutoff current	3041	Bias condition C; V <sub>CE</sub> = 50 V dc	I <sub>CES</sub>		10	nA dc
Collector to base cutoff current	3036	Bias condition D; V <sub>CB</sub> = 40 V dc, I <sub>E</sub> = 0 mA dc	I <sub>CBO2</sub>		1.7	μA dc
Forward-current transfer ratio 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3076	V <sub>CE</sub> = 1 V dc; I <sub>C</sub> = 100 mA dc	h <sub>FE1</sub>	60 60	150	
Forward-current transfer ratio 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3076	V <sub>CE</sub> = 1.0 V dc; I <sub>C</sub> = 300 mA dc	h <sub>FE2</sub>	35 40		
Forward-current transfer ratio 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3076	V <sub>CE</sub> = 1.0 V dc; I <sub>C</sub> = 500 mA dc	h <sub>FE3</sub>	40 35		

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/  <u>Subgroup 2</u> - Continued	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Forward-current transfer ratio 2N3724, L, 2N3724UB	3076	$V_{CE} = 5 \text{ V dc}; I_C = 1 \text{ A dc};$ pulsed (see 4.5.1)	$h_{FE4}$	30		
Forward-current transfer ratio 2N3725, L, 2N3725UB	3076	$V_{CE} = 1 \text{ V dc}; I_C = 10 \text{ mA dc};$ pulsed (see 4.5.1)	$h_{FE4}$	30		
Forward-current transfer ratio 2N3724, L, 2N3724UB	3076	$V_{CE} = 1 \text{ V dc}; I_C = 10 \text{ mA dc};$ pulsed (see 4.5.1)	$h_{FE5}$	30		
Forward-current transfer ratio 2N3725, L, 2N3725UB	3076	$V_{CE} = 2 \text{ V dc}; I_C = 800 \text{ mA dc};$ pulsed (see 4.5.1)	$h_{FE5}$	20		
Forward-current transfer ratio 2N3724, L, 2N3724UB	3076	$V_{CE} = 2 \text{ V dc}; I_C = 800 \text{ mA dc};$ pulsed (see 4.5.1)	$h_{FE6}$	25		
Forward-current transfer ratio 2N3725, L, 2N3725UB	3076	$V_{CE} = 5 \text{ V dc}; I_C = 1 \text{ A dc};$ pulsed (see 4.5.1)	$h_{FE6}$	25		
Collector-emitter saturation voltage 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3071	$I_C = 10 \text{ mA dc}; I_B = 1.0 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{CE(sat)1}$ $V_{CE(sat)1}$		0.25 0.25	V dc V dc
Collector-emitter saturation voltage 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3071	$I_C = 100 \text{ mA dc}; I_B = 10 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{CE(sat)2}$ $V_{CE(sat)2}$		0.2 0.26	V dc V dc
Collector-emitter saturation voltage 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3071	$I_C = 300 \text{ mA dc}; I_B = 30 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{CE(sat)3}$ $V_{CE(sat)3}$		0.32 0.4	V dc V dc
Collector-emitter saturation voltage 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3071	$I_C = 500 \text{ mA dc}; I_B = 50 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{CE(sat)4}$ $V_{CE(sat)4}$		0.42 0.52	V dc V dc
Collector-emitter saturation voltage 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3071	$I_C = 800 \text{ mA dc}; I_B = 80 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{CE(sat)5}$ $V_{CE(sat)5}$		0.65 0.8	V dc V dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - Continued						
Collector-emitter saturation voltage 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3071	$I_C = 1 \text{ A dc}; I_B = 100 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{CE(sat)6}$ $V_{CE(sat)6}$		0.75 0.95	V dc V dc
Base-emitter saturation voltage 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3066	Test condition A; $I_C = 10 \text{ mA dc};$ $I_B = 1 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{BE(sat)1}$ $V_{BE(sat)1}$		0.76 0.76	V dc V dc
Base-emitter saturation voltage 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3066	Test condition A; $I_C = 100 \text{ mA dc};$ $I_B = 10 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{BE(sat)2}$ $V_{BE(sat)2}$		0.86 0.86	V dc V dc
Base-emitter saturation voltage 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3066	Test condition A; $I_C = 300 \text{ mA dc};$ $I_B = 30 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{BE(sat)3}$ $V_{BE(sat)3}$		1.1 1.1	V dc V dc
Base-emitter saturation voltage 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3066	Test condition A; $I_C = 800 \text{ mA dc};$ $I_B = 80 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{BE(sat)4}$ $V_{BE(sat)4}$		1.5 1.5	V dc V dc
Base-emitter saturation voltage 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3066	Test condition A; $I_C = 1 \text{ A dc};$ $I_B = 100 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{BE(sat)5}$ $V_{BE(sat)5}$		1.7 1.7	V dc V dc
Base-emitter voltage 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3066	Test condition A; $I_C = 500 \text{ mA dc};$ $I_B = 50 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{BE}$ $V_{BE}$	0.9 0.8	1.2 1.1	V dc V dc
<u>Subgroup 3</u>						
High temperature operation		$T_A = +150^\circ\text{C}$				
Collector to base cutoff current	3036	Bias condition D; $V_{CB} = 60 \text{ V dc}$ for 2N3725 $V_{CB} = 40 \text{ V dc}$ for 2N3724	$I_{CBO3}$		5 5	$\mu\text{A dc}$ $\mu\text{A dc}$

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u> - Continued						
Low temperature operation						
Forward-current transfer ratio 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3076	$T_A = -55^\circ\text{C}$ $V_{CE} = 2\text{ V dc}; I_C = 800\text{ mA dc}$	$h_{FE7}$	30		
			$h_{FE7}$	20		
Forward-current transfer ratio 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3076	$V_{CE} = 1.0\text{ V dc}; I_C = 1\text{ A dc}$	$h_{FE8}$	20		
			$h_{FE8}$	25		
<u>Subgroup 4</u>						
Magnitude of small-signal short-circuit forward current transfer ratio 2N3724, L, 2N3724UB 2N3725, L, 2N3725UB	3306	$V_{CE} = 10\text{ V dc}; I_C = 50\text{ mA dc};$ $f = 100\text{ MHz}$	$ h_{fe} $	3.0		
			$ h_{fe} $	3.0		
Open circuit output capacitance	3236	$V_{CB} = 10\text{ V dc}; I_E = 0;$ $100\text{ kHz} \leq f \leq 1\text{ MHz}$	$C_{obo}$		12	pF
Input capacitance (output open-circuited)	3240	$V_{EB} = -0.5\text{ V dc}; I_C = 0;$ $100\text{ kHz} \leq f \leq 1\text{ MHz}$	$C_{ibo}$		55	pF
Switching time	3251					
Turn-on delay time		$V_{CC} = 30\text{ V dc}, I_{CS} = 500\text{ mA dc},$ $I_{B1} = 50\text{ mA dc}, V_{BE(\text{off})} = -3.8\text{ V dc}.$ See figure 12.				
2N3724, L, 2N3724UB 2N3725, L, 2N3725UB			$t_d$		10	ns
			$t_d$		10	ns
Rise time		$V_{CC} = 30\text{ V dc}, I_{CS} = 500\text{ mA dc},$ $I_{B1} = 50\text{ mA dc}, V_{BE(\text{off})} = -3.8\text{ V dc}.$ See figure 12.				
2N3724, L, 2N3724UB 2N3725, L, 2N3725UB			$t_r$		30	ns
			$t_r$		30	ns

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u> - Continued						
Storage time	3251	$V_{CC} = 30 \text{ V dc}$ , $I_{CS} = 500 \text{ mA dc}$ , $I_{B1} = 50 \text{ mA dc}$ , $I_{B2} = -50 \text{ mA dc}$ . See figure 12.				
2N3724, L, 2N3724UB			$t_s$		50	ns
2N3725, L, 2N3725UB			$t_s$		50	ns
Fall time		$V_{CC} = 30 \text{ V dc}$ , $I_{CS} = 500 \text{ mA dc}$ , $I_{B1} = 50 \text{ mA dc}$ , $I_{B2} = -50 \text{ mA dc}$ . See figure 12.				
2N3724, L, 2N3724UB			$t_f$		30	ns
2N3725, L, 2N3725UB			$t_f$		30	ns
Turn-off time		$I_C = 500 \text{ mA dc}$ , $I_{B1} = 50 \text{ mA dc}$ , $I_{B2} = -50 \text{ mA dc}$ . See figure 12.				
2N3724, L, 2N3724UB			$t_{off}$		60	ns
2N3725, L, 2N3725UB			$t_{off}$		60	ns
<u>Subgroups 5 and 6</u>						
Not required						

1/ For sampling plan see MIL-PRF-19500.

2/ For resubmission of failed in table I, subgroup 1, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.

3/ Separate samples may be used.

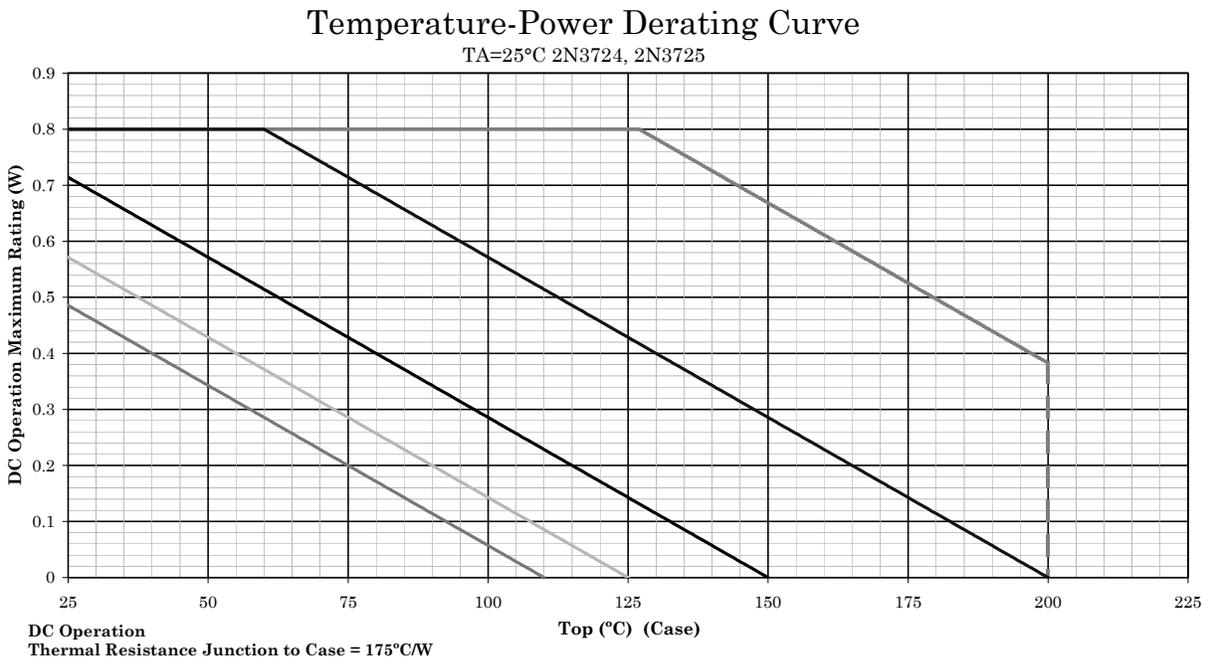
4/ Not required for JANS devices.

5/ Not required for laser marked devices.

6/ This hermetic seal test is an end-point to temp cycling in addition to electrical measurements.

TABLE II. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	45 devices c = 0
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 and 4.5.3 herein.	
<u>Subgroup 2</u>			
Intermittent life	1037	Intermittent operation life: $V_{CB} = 10$ V dc, 6000 cycles	45 devices c = 0
Electrical measurements		See table I, subgroup 2 and 4.5.3 herein.	
<u>Subgroup 3</u>			
Destructive physical analysis (DPA)	2102		3 devices c = 0
<u>Subgroup 4</u>			
Thermal resistance	3131	$R_{\theta JSP(IS)}$ can be calculated but shall be measured once in the same package with a similar die size to confirm calculations (may apply to multiple slash sheets). $R_{\theta JA}$ , $R_{\theta JC}$ only	15 devices, c = 0
Thermal impedance, thermal resistance curves		Each supplier shall submit their (typical) design maximum thermal impedance curves. In addition, the optimal test conditions and $Z_{\theta JX}$ limit shall be provided to the qualifying activity in the qualification report. See figures 8, 9, 10, and 11.	sample size N/A
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 6</u>			
ESD	1020		3 devices
<u>Subgroup 8</u>			
Reverse stability	1033	Condition A for devices $\geq 400$ V, condition B for devices $< 400$ V.	45 devices c = 0



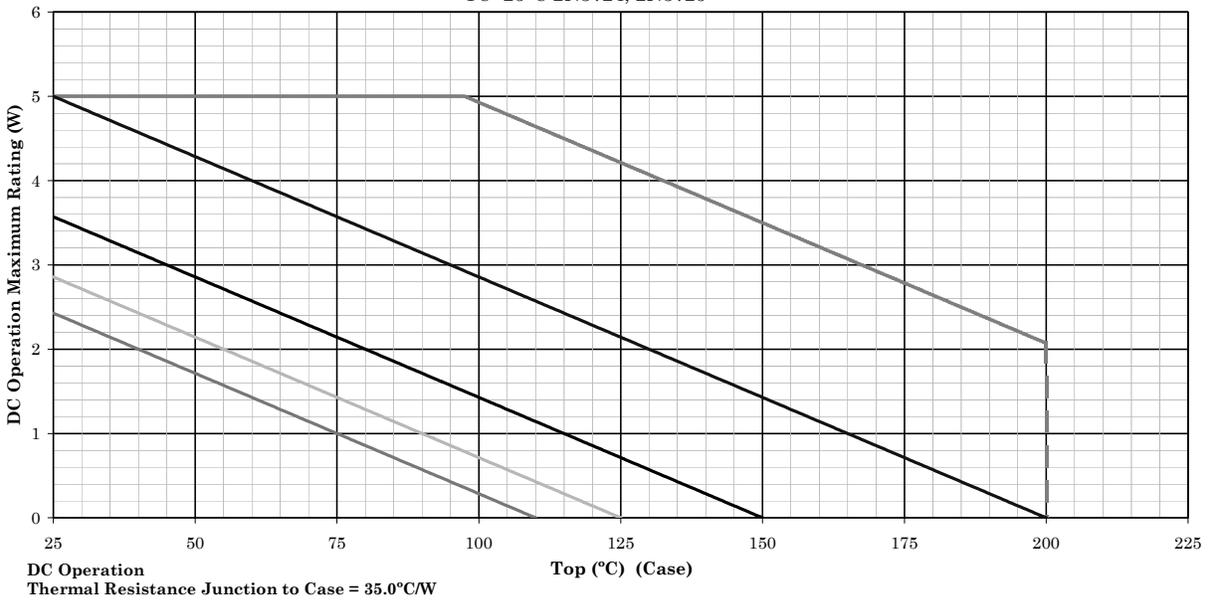
## NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
2. Derate design curve constrained by the maximum junction temperature ( $T_J \leq 200^\circ\text{C}$ ) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 4. Derating for 2N3724 and 2N3725 ( $R_{\theta JC}$ ) .125 inch (3.175 mm) PCB (TO-5 and TO-39).

## Temperature-Power Derating Curve

TC=25°C 2N3724, 2N3725



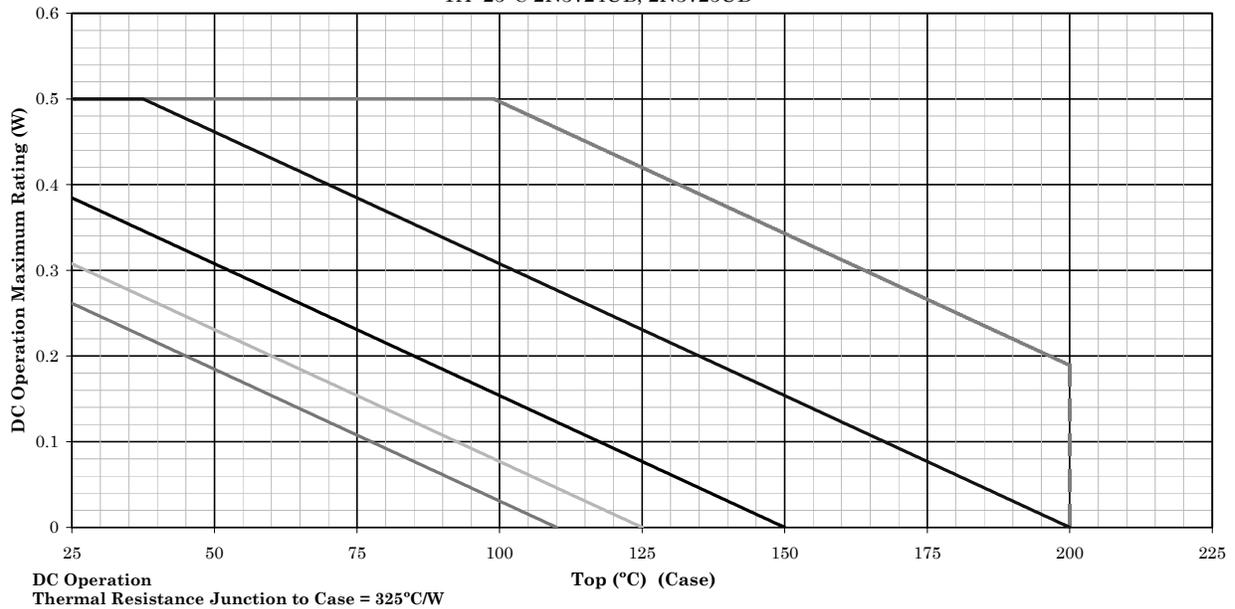
### NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
2. Derate design curve constrained by the maximum junction temperature ( $T_J \leq 200^\circ\text{C}$ ) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application..

FIGURE 5. Derating for 2N3724 and 2N3725 ( $R_{\theta JC}$ ), (TO-5 and TO-39).

## Temperature-Power Derating Curve

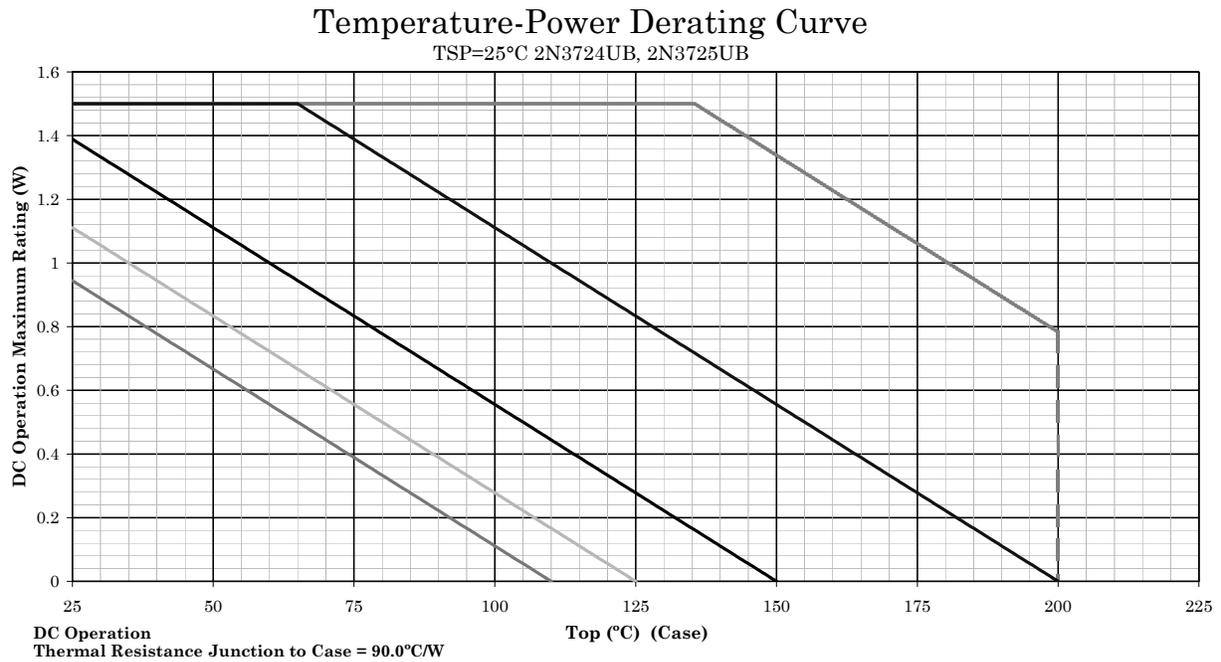
TA=25°C 2N3724UB, 2N3725UB



### NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
2. Derate design curve constrained by the maximum junction temperature ( $T_J \leq 200^\circ\text{C}$ ) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 6. Derating for 2N3724UB and 2N3725UB ( $R_{\theta JC}$ ).

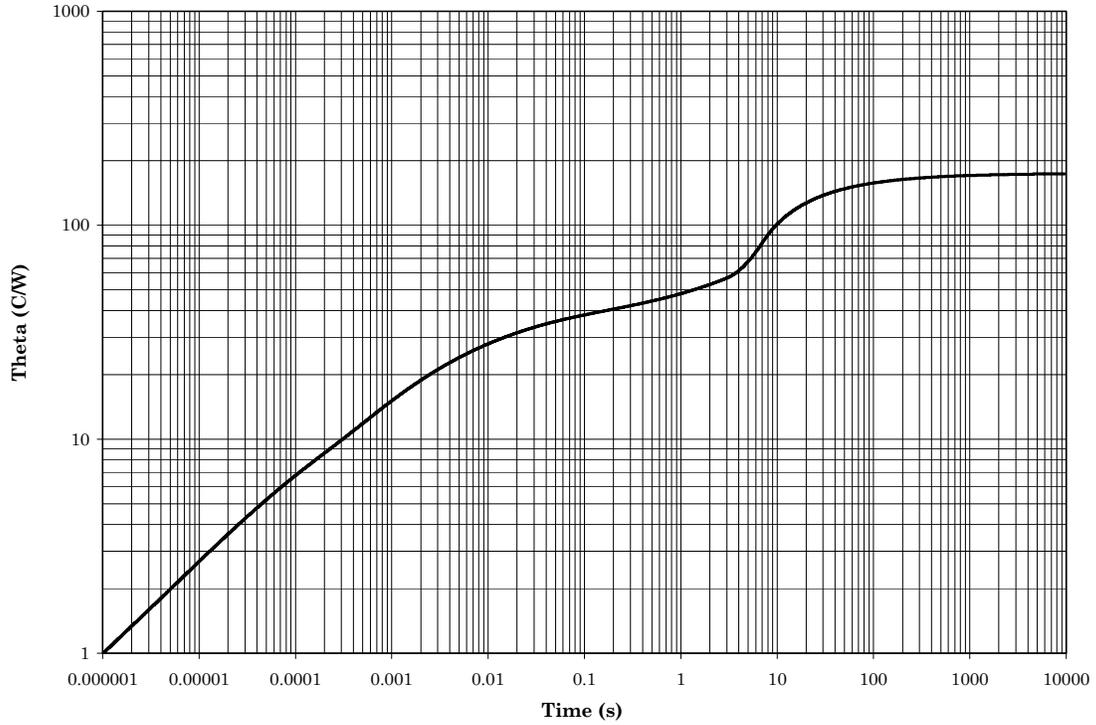


## NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
2. Derate design curve constrained by the maximum junction temperature ( $T_J \leq 200^\circ\text{C}$ ) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 7. Derating for 2N3724UB and 2N3725UB ( $R_{\theta JSP}$ ).

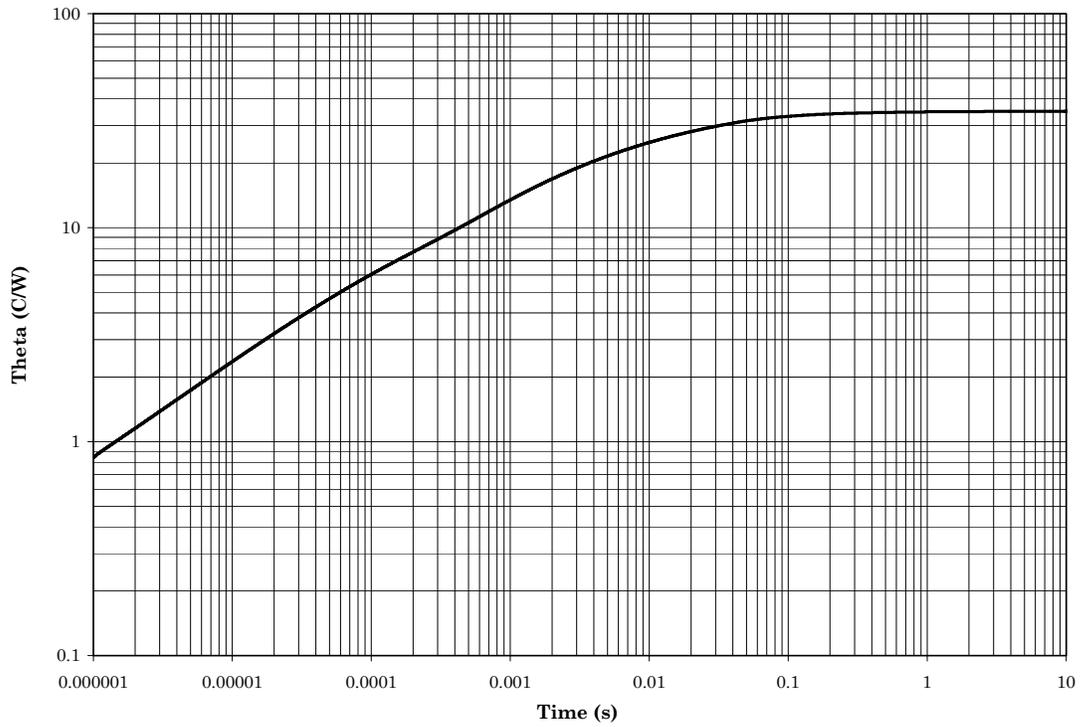
### Maximum Thermal Impedance



Ambient free air cooled  $T_A = +25^\circ\text{C}$ , 800mW, Thermal Resistance  $R_{\theta JA} = 175^\circ\text{C/W}$ .

FIGURE 8. Thermal impedance graph ( $R_{\theta JA}$ ) for 2N3724 and 2N3725 (TO-5 and TO-39).

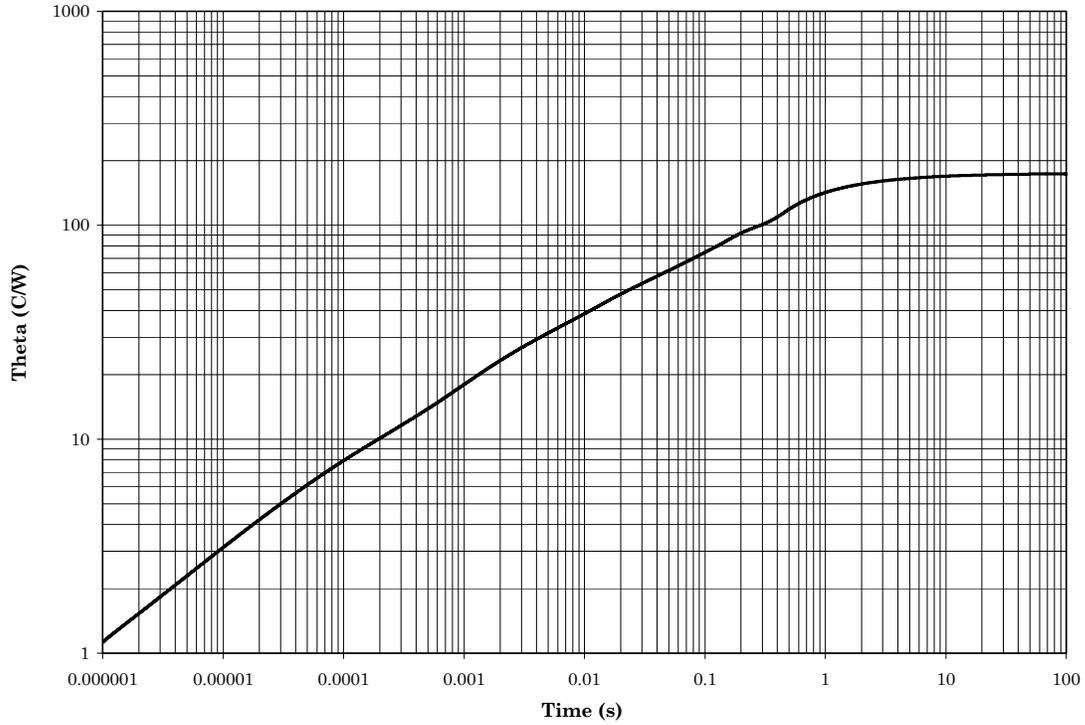
### Maximum Thermal Impedance



Ambient Case Mounted  $T_C = +25^\circ\text{C}$ , Thermal resistance  $R_{\theta JC} = 35^\circ\text{C/W}$ .

FIGURE 9. Thermal impedance graph ( $R_{\theta JC}$ ) for 2N3724 and 2N3725 (TO-5 and TO-39).

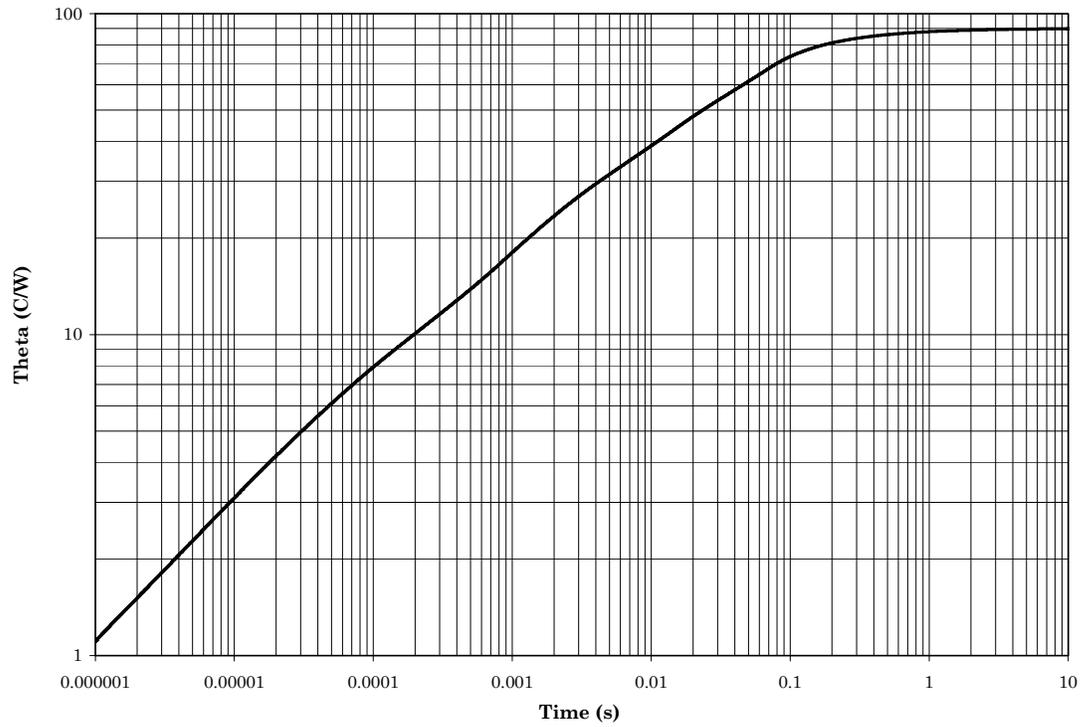
**Maximum Thermal Impedance**



Mounted to minimal copper clad PCB at  $T_A = +25^\circ\text{C}$  (no heat sinking except air). Thermal resistance  $R_{\theta JA} = 175^\circ\text{C/W}$

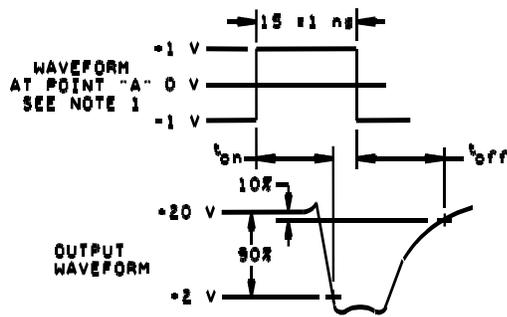
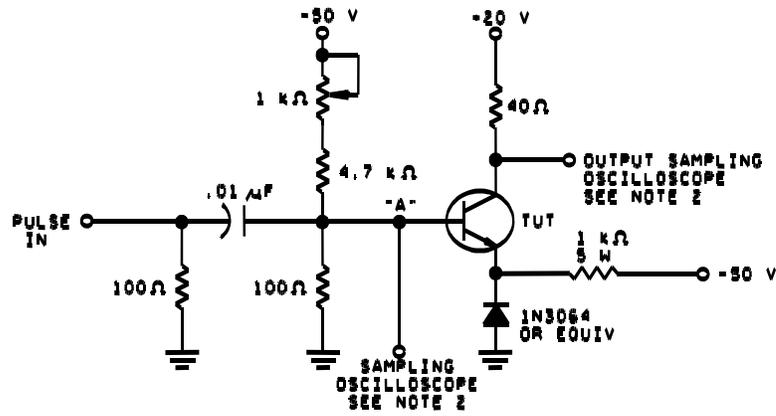
FIGURE 10. Thermal impedance graph ( $R_{\theta JA}$ ) for 2N3724UB and 2N3725UB (UB).

### Maximum Thermal Impedance



Solder mounted to very heavy copper clad PCB at  $T_{\theta_{JSP}(IS)} = +25^{\circ}\text{C}$ . Thermal Resistance  $R_{\theta_{JSP}(IS)} = 90^{\circ}\text{C/W}$

FIGURE 11. Thermal impedance graph ( $R_{\theta_{JSP}(IS)}$ ) for 2N3724UB and 2N3725UB (UB).



NOTES:

1. The rise time ( $t_r$ ) of the applied pulse shall be  $\leq 2.0$  ns, duty cycle  $\leq 2$  percent and the generator source impedance shall be 50 ohms.
2. Sampling oscilloscope:  $Z_{IN} \geq 100$  k $\Omega$ ,  $C_{IN} \leq 12$  pF, rise time  $\leq 2.0$  ns.

FIGURE 12. Nonsaturated switching-time test circuit.

## 5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

## 6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. Product assurance level and type designator.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

6.4 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:  
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