

PERFORMANCE SPECIFICATION SHEET

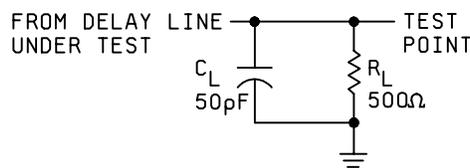
DELAY LINES, ACTIVE, 14-PIN SURFACE MOUNT, 5 TAP

This amendment forms a part of MIL-PRF-83532/8, dated 15 May 1999, and is approved for use by all Departments and Agencies of the Department of Defense.

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Output rise time (applied to leading edge only), delete and substitute:

"5 ns maximum. Measurement conditions ($-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$): $V_{CC} = 5.0 \text{ V dc}$; $T_{RI} \leq 3 \text{ ns}$. The load circuit shall be as follows (C_L includes probe and test fixture capacitance):



Custodians:
Army - CR
Navy - EC
Air Force - 11
DLA - CC

Preparing activity:
DLA - CC

(Project 5999-0363)