3000 Series

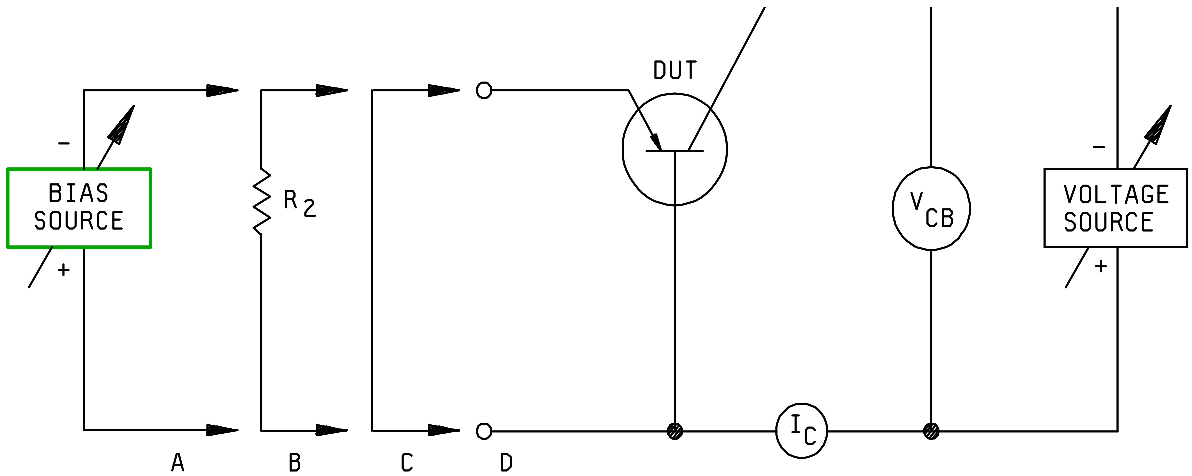
Electrical characteristics tests for bipolar transistors

METHOD 3001.1

BREAKDOWN VOLTAGE, COLLECTOR TO BASE

1. Purpose. The purpose of this test is to determine if the breakdown voltage of the device under the specified conditions is greater than the specified minimum limit.

2. Test circuit. See figure 3001-1.



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the ammeter drop.

FIGURE 3001-1. Test circuit for breakdown voltage, collector to base.

3. Procedure. The resistor R_1 is a current-limiting resistor and should be of sufficiently high resistance to avoid excessive current flowing through the device and current meter. The voltage shall be gradually increased, with the specified bias conditions (condition A, B, C, or D) applied, from zero until either the minimum limit for $V_{(BR)CBX}$ or the specified test current is reached. The device is acceptable if the minimum limit for $V_{(BR)CBX}$ is reached before the test current reaches the specified value. If the specified test current is reached first, the device is rejected.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test current (see 3.).

b. Bias condition:

A: Emitter to base: Reverse bias (specify bias voltage).

B: Emitter to base: Reverse return (specify resistance of R_2).

C: Emitter to base: Short circuit.

D: Emitter to base: Open circuit.

METHOD 3005.1

BURNOUT BY PULSING

1. Purpose. The purpose of this test is to determine the capabilities of the device to withstand pulses.

2. Procedure. The device shall be subjected to a pulse or pulses of the length, voltages, currents, and repetition rate specified with the specified prepulse conditions.

3. Summary. The following conditions shall be specified in the detail specification:

a. Prepulse conditions (see 2.).

b. Pulse width (see 2.).

c. Pulse voltages and currents (see 2.).

d. Repetition rate (see 2.).

e. Measurements after test.

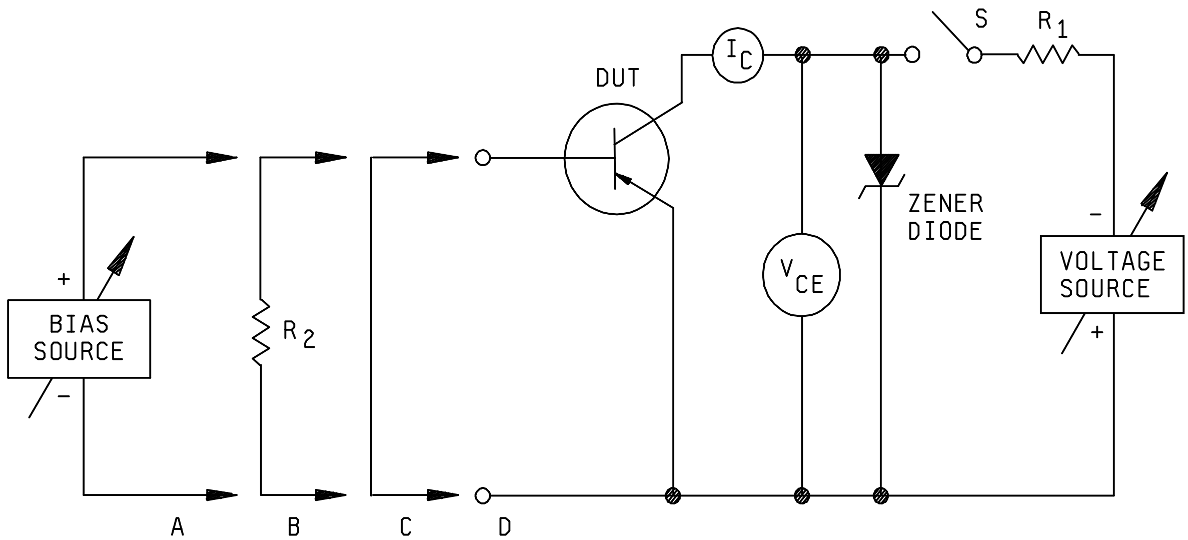
f. Length of test or number of cycles.

METHOD 3011.2

BREAKDOWN VOLTAGE, COLLECTOR TO EMITTER

1. Purpose. The purpose of this test is to determine if the breakdown voltage of the device under the specified conditions is greater than the specified minimum limit.

2. Test circuit. See figure 3011-1.



NOTES:

1. A PNP device is shown. For NPN types, reverse the polarities of the voltage and bias sources and zener diode.
2. An electronic switch, "S" may be necessary to provide pulses of short duty cycle to minimize the rise of junction temperature.
3. The current sensor, or ammeter, shall present essentially a short circuit to the terminals between which the current is being measured, or the voltage readings shall be corrected accordingly.
4. It is important to prevent, or dampen, potentially damaging oscillations in devices exhibiting negative resistance breakdown characteristics. Protection can be in the form of a circuit which circumvents the negative resistance region, such as one which provides suitable base current as the collector voltage is increased; however, the specified bias condition and test current must be applied when the voltage is measured. Additional protection can be provided with a zener diode, or transient voltage protection circuit to limit to collector voltage at, or slightly above, the specified minimum limit.
5. Regardless of the protection used, extreme care must be exercised to ensure the collector current and junction temperature remain at a safe value, as given in the applicable device specification.

FIGURE 3011-1. Test circuit for breakdown voltage, collector to emitter.

3. Procedure. The resistor R_1 is a current-limiting resistor and should be of sufficiently high resistance to avoid excessive current flowing through the device and current sensor. The voltage shall be increased, with the specified bias conditions (condition A, B, C, or D) applied, until the specified test current is reached. The device is acceptable if the voltage applied at the specified test current is greater than the minimum limit for $V_{(BR)CEX}$.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test current (see 3.).

b. Duty cycle and pulse width, when required (see note 1 above).

c. Bias condition as follows:

A: Emitter to base: Reverse bias (specify bias voltage).

B: Emitter to base: Resistance return (specify resistance value of R_2).

C: Emitter to base: Short circuit.

D: Emitter to base: Open circuit.

METHOD 3015

DRIFT

1. Purpose. The purpose of this test is to determine the drift of a parameter specified in the detail specification of the device.

2. Apparatus. The apparatus used for the performance of the drift test shall be the same as that utilized for testing the associated parameter.

3. Procedure. The voltages and currents specified in the detail specification shall be applied. In the period from 10 seconds to 1 minute, the measurement specified in the detail specification shall drift no more than the amount specified in the detail specification.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test currents and voltages (see 3.).

b. Test parameter (see 3.).

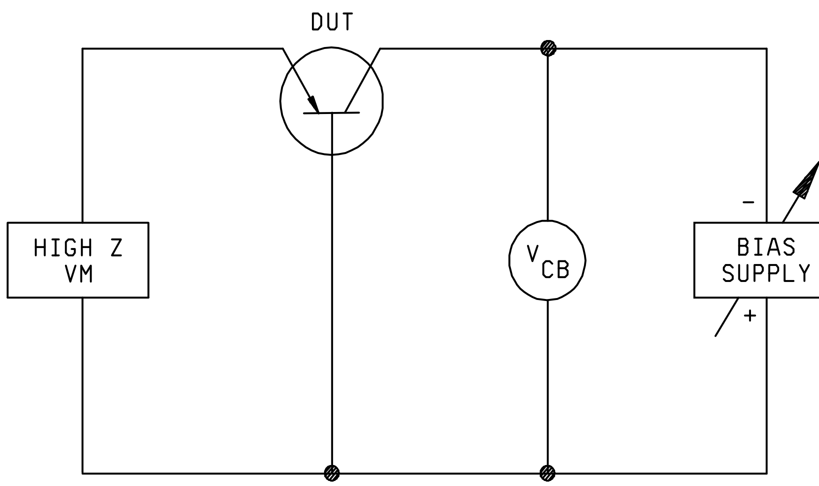
c. Test apparatus or test circuit (see 2.).

METHOD 3020

FLOATING POTENTIAL

1. Purpose. The purpose of this test is to measure the dc potential between the specified, open-circuited terminal and reference terminal when a dc potential is applied to the other specified terminals.

2. Test circuit. See figure 3020-1.



NOTE: The circuit shown is for measuring the emitter floating potential. For other device configurations the above circuitry should be modified in such a manner that is capable of demonstrating device conformance to the minimum requirements of the individual specification.

FIGURE 3020-1. Test circuit for floating potential.

3. Procedure. The specified dc voltage shall be applied to the specified terminals and the dc voltage of the open-circuited terminal and reference terminal shall be monitored.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltage (see 3.).

b. Input resistance of high impedance voltmeter (see figure 3020-1).

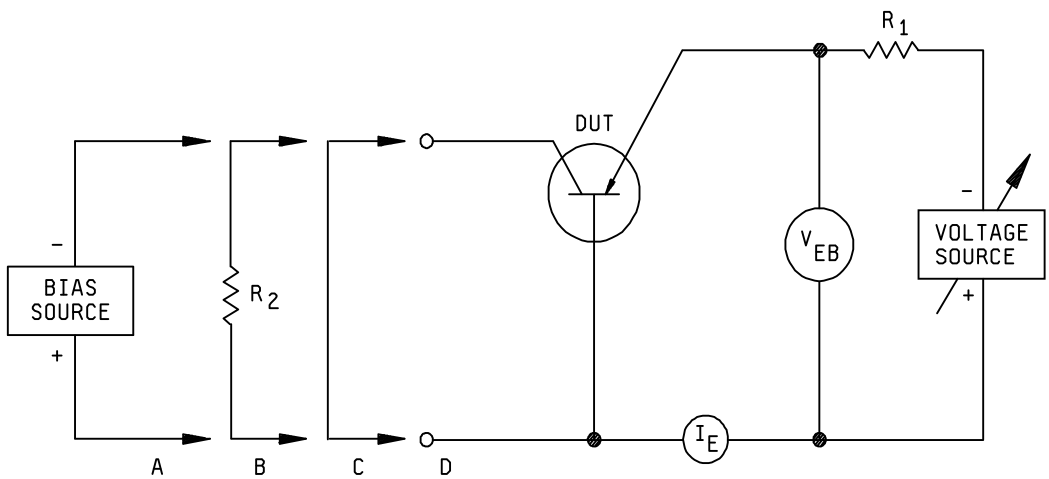
c. Test voltage application and reference terminals (see 3.).

METHOD 3026.1

BREAKDOWN VOLTAGE, EMITTER TO BASE

1. Purpose. The purpose of this test is to determine if the breakdown voltage of the device under the specified conditions is greater than the specified minimum limit.

2. Test circuit. See figure 3026-1.



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the ammeter drop.

FIGURE 3026-1. Test circuit for breakdown voltage, emitter to base.

3. Procedure. The resistor R_1 is a current-limiting resistor and should be of sufficiently high resistance to avoid excessive current flowing through the device and current meter. The voltage shall be gradually increased, with the specified condition (A, B, C, or D) applied, from zero until either the minimum limit for $V_{(BR)EBX}$ or the specified test current is reached. The device is acceptable if the minimum limit for $V_{(BR)EBX}$ is reached before the test current reaches the specified value. If the specified test current is reached first, the device is rejected.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test current (see 3.).

b. Bias condition:

A: Collector to base: Reverse bias (specify bias voltage).

B: Collector to base: Resistance return (specify resistance of R_2).

C: Collector to base: Short circuit.

D: Collector to base: Open circuit.

METHOD 3030

COLLECTOR TO EMITTER VOLTAGE

1. Purpose. The purpose of this test is to measure the voltage between the collector and emitter of the device under specified conditions.

2. Test circuit. See figure 3030-1.

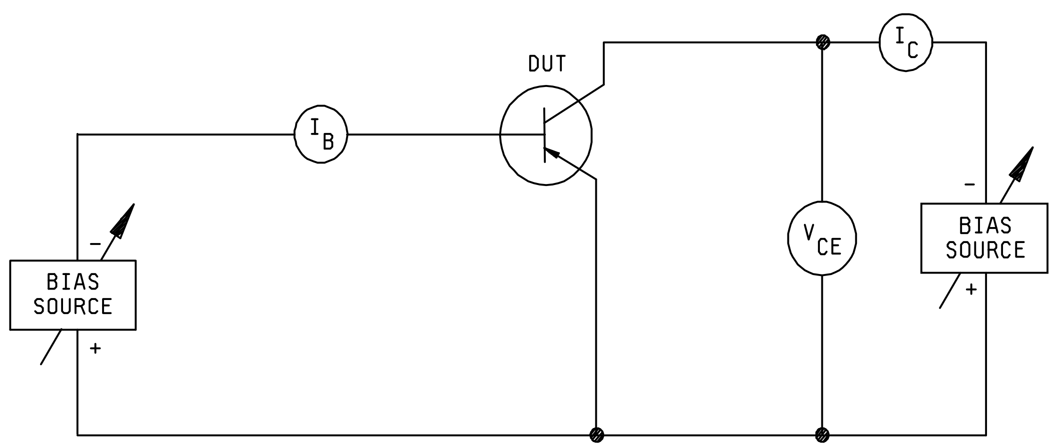


FIGURE 3030-1. Test circuit for collector to emitter voltage.

3. Procedure. The bias supplies shall be adjusted until the specified voltages and currents are achieved. The voltage between the collector and emitter shall then be measured. If high current values are to be used in this measurement, suitable pulse techniques may be used to provide pulses of short duty cycle to minimize the rise in junction temperature.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltages and currents (see 3.).

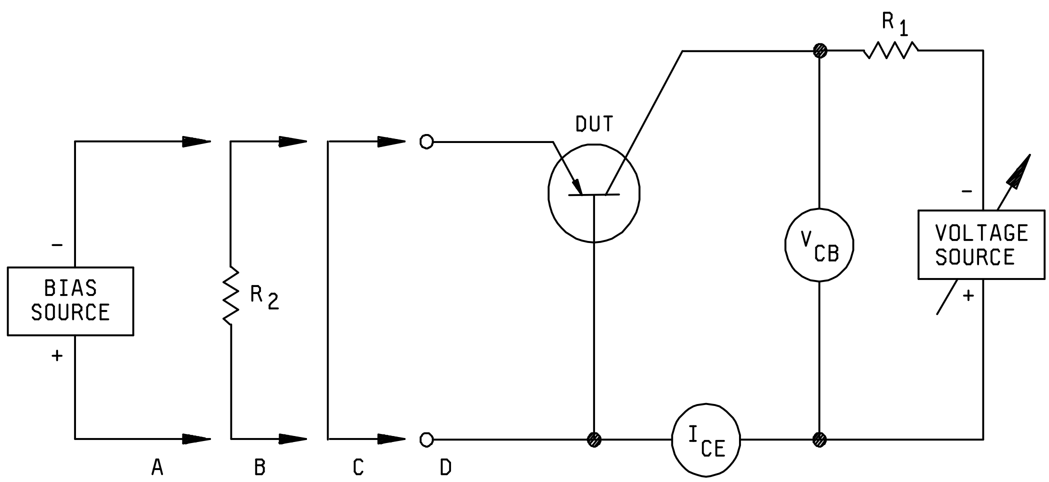
b. Duty cycle and pulse width if applicable (see 3.).

METHOD 3036.1

COLLECTOR TO BASE CUTOFF CURRENT

1. Purpose. The purpose of this test is to measure the cutoff current of the device under the specified conditions.

2. Test circuit. See figure 3036-1.



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter shall be corrected for the drop across the ammeter.

FIGURE 3036-1. Test circuit for collector to base cutoff current.

3. Procedure. The specified dc voltage shall be applied between the collector and the base with the specified bias condition (A, B, C, or D) applied to the emitter. The measurement of current shall be made at the specified ambient or case temperature.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltage (see 3.).

b. Test temperature if other than +25°C ±3°C and whether case or ambient (see 3.).

c. Bias condition:

A: Emitter to base: Reverse bias (specify bias voltage).

B: Emitter to base: Resistance return (specify resistance of R_2).

C: Emitter to base: Short circuit.

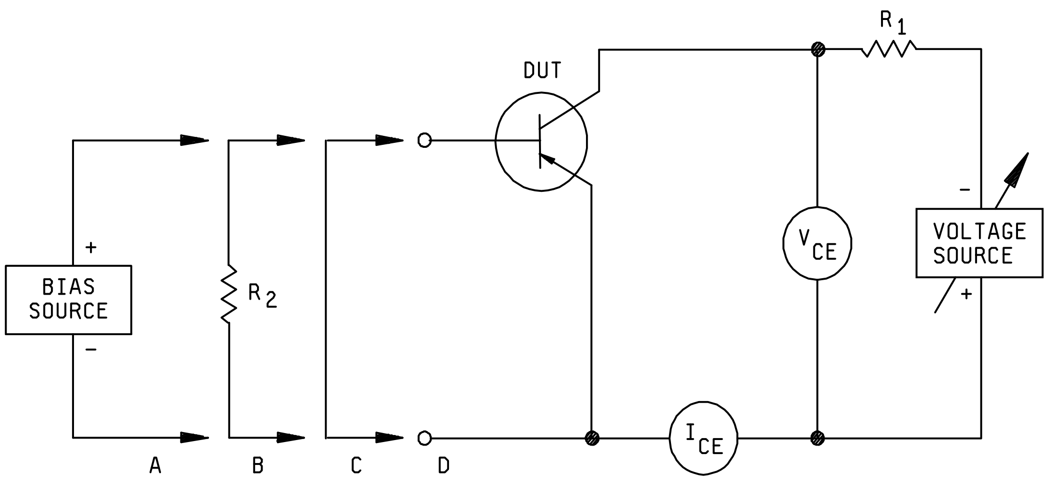
D: Emitter to base: Open circuit.

METHOD 3041.1

COLLECTOR TO EMITTER CUTOFF CURRENT

1. Purpose. The purpose of this test is to measure the cutoff current of the device under the specified conditions.

2. Test circuit. See figure 3041-1.



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter shall be corrected for the drop across the ammeter.

FIGURE 3041-1. Test circuit for collector to emitter cutoff current.

3. Procedure. The specified voltage shall be applied between the collector and emitter with the specified bias condition (A, B, C, or D) applied to the base. The measurement of current shall be made at the specified ambient or case temperature.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltage (see 3.).

b. Test temperature if other than +25°C ±3°C and whether case or ambient (see 3.).

c. Bias condition:

A: Emitter to base: Reverse bias (specify bias voltage).

B: Emitter to base: Resistance return (specify resistance value of R_2).

C: Emitter to base: Short circuit.

D: Emitter to base: Open circuit.

METHOD 3051

SAFE OPERATING AREA (CONTINUOUS DC)

1. Purpose. The purpose of this test is to verify the boundary of the SOA of a transistor as constituted by the interdependency of the specified voltage, current, power, and temperature in a temperature stable circuit.

2. Test circuit. See figure 3051-1.

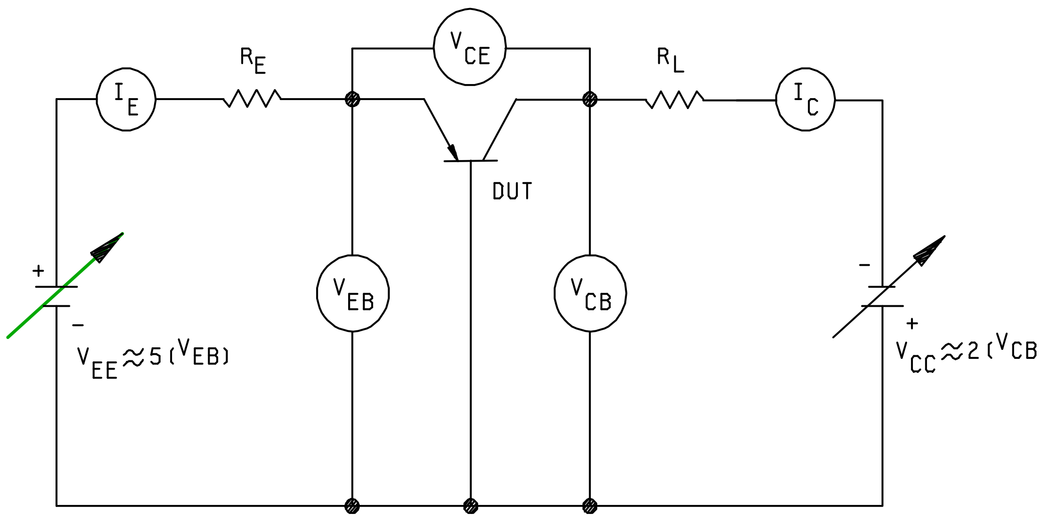


FIGURE 3051-1. Test circuit for SOA (continuous dc).

3. Procedure.

a. Starting with V_{CC} and V_{EE} at a low value, increase V_{CC} to approximately obtain specified V_{CE}. Increase V_{EE} to approximately obtain specified I_C. Increase V_{CC} and subsequently adjust V_{EE} to obtain specified V_{CE} and I_C. Operate the transistor at the specified temperature and for the specified time duration.

b. Decrease V_{CC} to obtain V_{CE} near zero. Turn off V_{EE}. Turn off V_{CC}.

c. The transistor shall be considered a failure if I_C varies ±10 percent during operation, or exceeds the end points.

4. Summary. The following conditions shall be specified in the detail specification:

a. Maximum SOA graph: I_C versus V_{CE} (see 3.).

b. Temperature, case or ambient (see 3.).

c. Values of V_{CE} and I_C.

d. Operating time (see 3.).

e. Measurements after test.

METHOD 3052

SAFE OPERATING AREA (PULSED)

1. Purpose. The purpose of this test is to verify the capability of a transistor to withstand pulses of specific voltage, current and time, establishing a SOA.

2. Test circuit. See figure 3052-1.

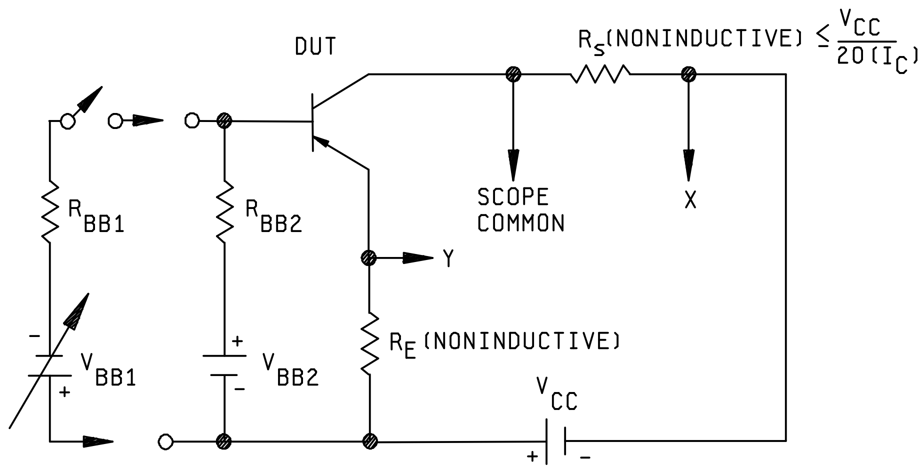


FIGURE 3052-1. Test circuit for SOA (pulsed).

3. Procedure. Starting at a low value, adjust V_{BB2} and V_{CC} to the specified levels. With the duty cycle and pulse width preset to specified conditions, increase V_{BB1} voltage to achieve the specified I_C.

4. Summary. The following conditions shall be specified in the detail specification:

a. Maximum SOA graph: I_C versus V_{CE}.

b. Temperature, case or ambient.

c. Input pulse and bias conditions:

(1) Pulse duty cycle.

(2) Pulse width.

(3) t_r and t_f.

(4) Values for R_{BB2}, R_{BB1}, and V_{BB2} (see figure 3052-1).

(5) Number of pulses or test duration.

d. Values of R_E, V_{CC}, and I_C (see 3.).

e. Measurements after test.

METHOD 3053

SAFE OPERATING AREA (SWITCHING)

1. Purpose. The purpose of this test is to verify the capability of a transistor to withstand switching between saturation and cut-off for various specified loads, establishing a SOA.

2. Test circuit. See figure 3053-1.

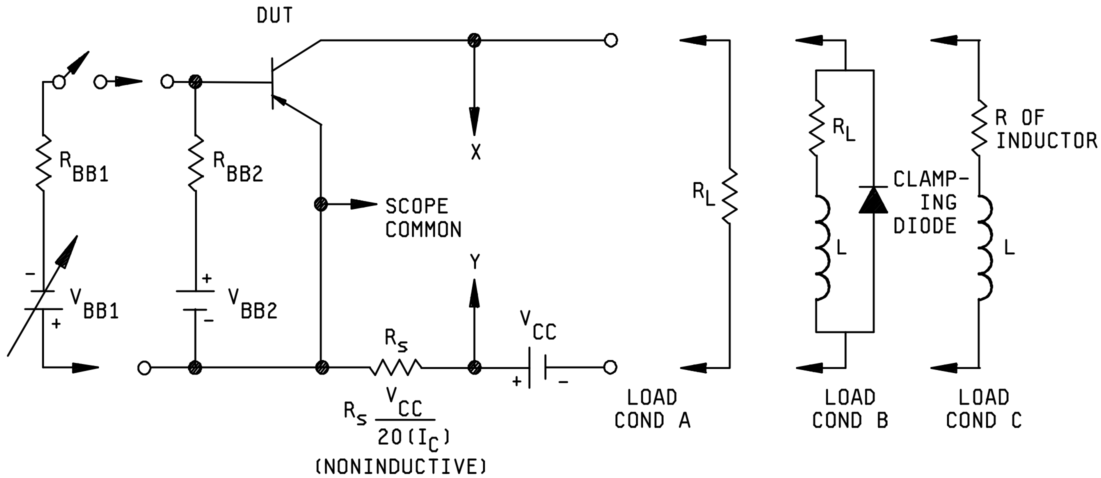


FIGURE 3053-1. Test circuit for SOA (switching).

3. Procedure. The output load circuit configuration shall be as specified (condition A, B, or C). Starting at a low value, adjust V_{BB2} and V_{CC} to the specified levels. With the duty cycle and repetition rate preset to specified conditions, increase V_{BB1} voltage to achieve the specified I_C; and the output waveform (I_C versus V_{CE}) shall be observed on the scope. When the transistor is turned off (switched), the observed trace shall be a smooth curve between saturation and cut-off. Any oscillations or inconsistencies on the trace shall be cause for rejection.

4. Summary. The following conditions shall be specified in the detail specification:

a. Maximum SOA graph, with parameter coordinates as follows:

(1) I_C versus V_{CE} for load condition A.

(2) I_C versus V_{CE} for load condition B.

(3) I_C versus L as functions of R_{BB2} and V_{BB2}, for load condition C.

b. Load condition as follows:

A: Resistive load.

B: Clamped inductive load.

C: Unclamped inductive load.

c. Temperature, case or ambient.

d. Input pulse and bias conditions:

(1) Number of pulses or test duration.

(2) Pulse width.

(3) Pulse duty cycle.

(4) t_r and t_f.

(5) R_{BB1} and V_{BB1}.

(6) R_{BB2} and V_{BB2}.

e. Specific conditions for load and output bias:

Condition A: Values of R_L, I_C, and V_{CC}.

Condition B: Values of R_L, I_C, V_{CC}, diode type or characteristics, inductance and dc resistance of L.

Condition C: Values of I_C, V_{CC}, and characteristics of inductor L including its inductance, "Q", dc resistance, and resonant frequency.

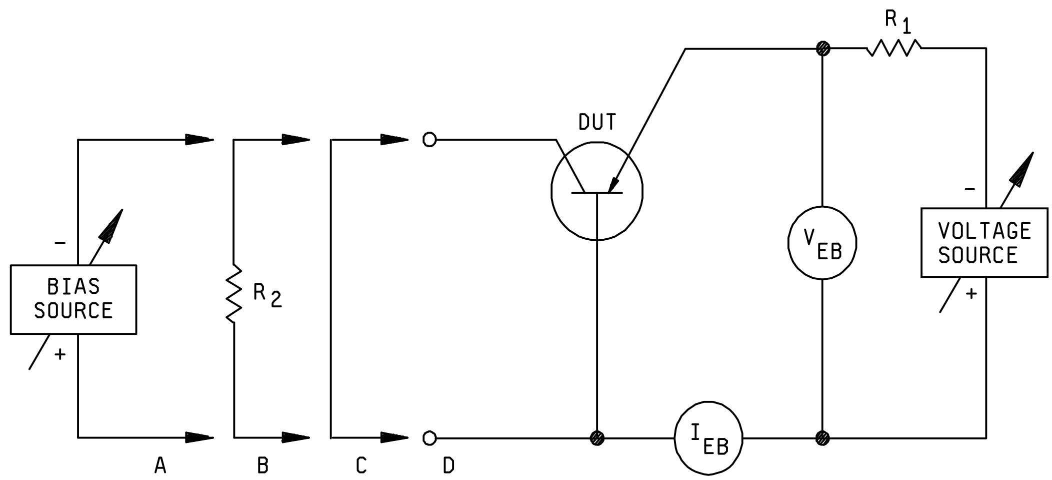
f. Measurements after test.

METHOD 3061.1

EMITTER TO BASE CUTOFF CURRENT

1. Purpose. The purpose of this test is to measure the cutoff current of the device under the specified conditions.

2. Test circuit. See figure 3061-1.



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter shall be corrected for the drop across the ammeter.

FIGURE 3061-1. Test circuit for emitter to base cutoff current.

3. Procedure. The specified direct current voltages shall be applied between the emitter and the base with the specified bias condition (condition A, B, C, or D) applied to the collector. The measurement of current shall be made at the specified ambient or case temperature.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltage (see 3.).

b. Test temperature if other than +25°C ±3°C and whether case or ambient (see 3.).

c. Bias condition (A, B, C, or D):

A: Collector to base: Reverse bias (specify bias voltage).

B: Collector to base: Resistance return (specify resistance of R_2).

C: Collector to base: Short circuit.

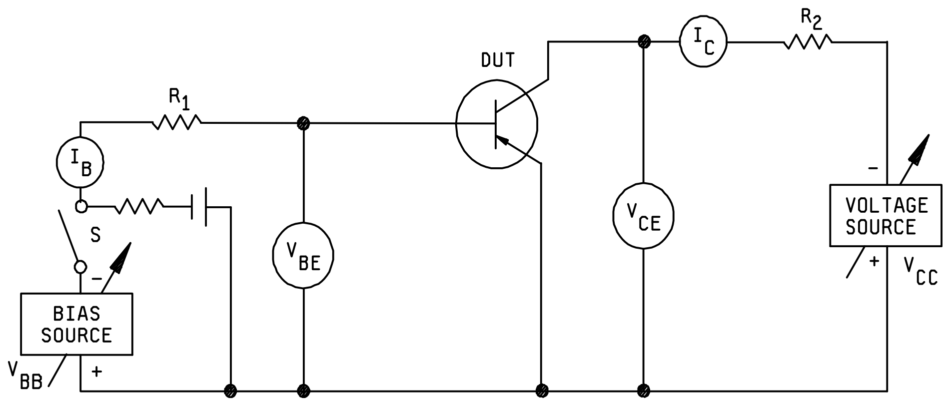
D: Collector to base: Open circuit.

METHOD 3066.1

BASE EMITTER VOLTAGE (SATURATED OR NONSATURATED)

1. Purpose. The purpose of this test is to measure the base to emitter voltage of the device in either a saturated or nonsaturated condition.

2. Test circuit. Circuit and procedure shown are for base to emitter. For other parameters the circuit and procedure should be changed accordingly.



NOTE: If necessary, switch S shall be used to provide pulses of short- duty cycle to minimize the rise in junction temperature. When pulsing techniques are used, oscillograph methods shall be used to measure V_{BE} and the other necessary parameters, and the duty cycle and pulse width shall be specified.

FIGURE 3066-1. Test circuit for base emitter voltage (saturated or nonsaturated).

3. Procedure.

3.1 Test condition A (saturated). The resistor R_1 shall be made large. If the pulse method is used, the resistor R_2 shall be chosen in combination with V_{CC} so that the specified collector current is achieved at a value of V_{CC} low enough to ensure that the device will not be operated in breakdown between pulses. If the pulse method is not used, resistor R_2 can be any convenient value. The current I_B and voltage V_{CC} shall be adjusted until I_B and I_C achieve their specified values. Then, $V_{BE} = V_{BE(sat)}$.

3.2 Test condition B (nonsaturated). For this test resistor R_2 shall be zero. The specified values of I_B and V_{CE} shall be applied. V_{BE} is then measured. Alternately, the specified V_{CE} shall be applied and I_B adjusted to obtain the specified I_C.

4. Summary. The following conditions shall be specified in the detail specification:

a. Duty cycle and pulse width, when required.

b. Test condition letter (see 3.).

c. Test voltages or currents (see 3.).

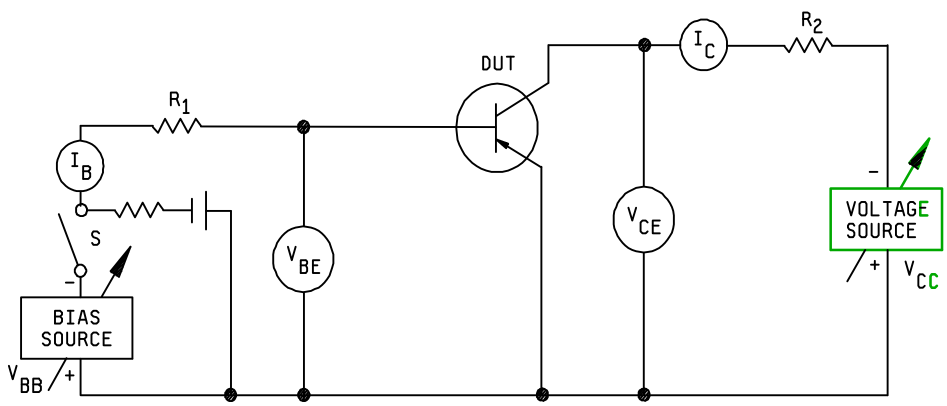
d. Parameter to be measured.

METHOD 3071

SATURATION VOLTAGE AND RESISTANCE

1. Purpose. The purpose of this test is to measure the saturation voltage and resistance of the device under the specified conditions.

2. Test circuit. Circuit and procedure shown are for collector to emitter. For other parameters the circuit and procedure should be changed accordingly.



NOTE: If necessary, switch S shall be used to provide pulses of short- duty cycle to minimize the rise in junction temperature. When pulsing techniques are used, oscillograph methods shall be used to measure V_{BE} and the other necessary parameters, and the duty cycle and pulse width shall be specified.

FIGURE 3071-1. Test circuit for saturation voltage and resistance.

3. Procedure. The resistor R_1 shall be made large. If the pulse method is used, resistor R_2 shall be chosen in combination with V_{CC} so that the specified collector current may be achieved at a value of V_{CC} which is low enough to ensure that the device is not operated in breakdown between pulses. If pulse methods are not used R_2 may be any convenient value. The current I_B and V_{CC} shall be adjusted until I_B and I_C achieve their specified values. $V_{CE(sat)}$ is then equal to the voltage measured by voltmeter V_{CE} under the specified conditions. Saturation resistance may be determined from the same circuit conditions, as follows:

$$r_{CE(sat)} = \frac{V_{CE}(sat)}{I_C}$$

4. Summary. The following conditions shall be specified in the detail specification:

a. Duty cycle and pulse width, when required (see 3.).

b. Test voltages or currents (see 3.).

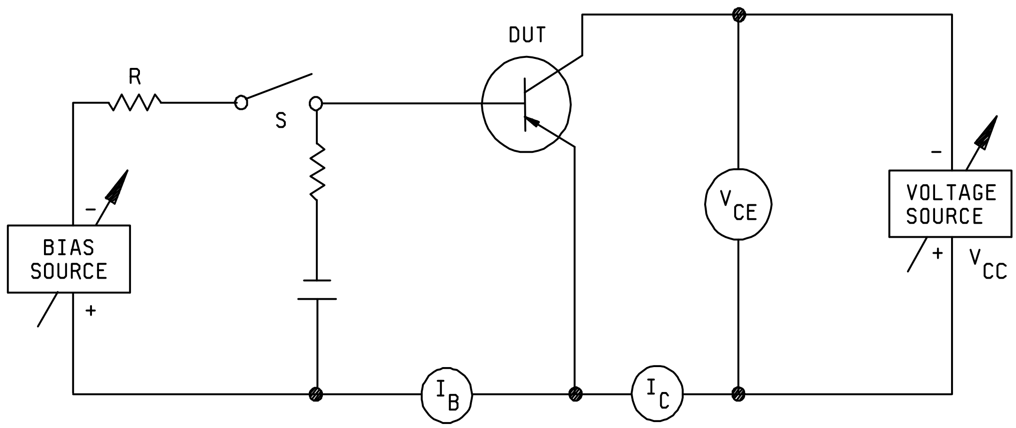
c. Parameter to be measured.

METHOD 3076.1

FORWARD-CURRENT TRANSFER RATIO

1. Purpose. The purpose of this test is to measure the forward-current transfer ratio of the device under the specified conditions.

2. Test circuit. Circuit and procedure shown are for common emitter. For other parameters the circuit and procedure should be changed accordingly.



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter shall be corrected for the drop across the ammeter.

FIGURE 3076-1. Test circuit for forward-current transfer ratio.

3. Procedure. The voltage V_{CE} shall be set to the specified value and the current I_B shall be adjusted until the specified current I_C is achieved.

Then, $h_{FE} = \frac{I_C}{I_B}$

If high-current values are to be used in this measurement, switch S shall be used to provide pulses of short-duty cycle to minimize the rise in junction temperature. When pulsing techniques are used, oscillograph methods may be used to measure I_C and I_B.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltage or current (see 3.).

b. Duty cycle and pulse width, when required (see 3.).

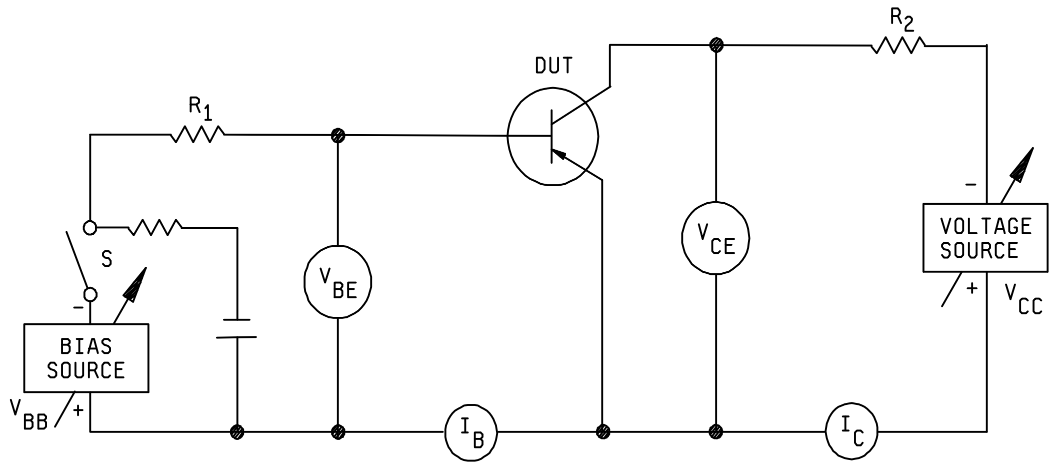
c. Parameter to be measured.

METHOD 3086.1

STATIC INPUT RESISTANCE

1. Purpose. The purpose of this test is to measure the input resistance of the device under the specified conditions.

2. Test circuit. Circuit and procedure shown are for common emitter. For other parameters the circuit and procedure should be changed accordingly.



NOTE: If necessary, switch S shall be used to provide pulses of short-duty cycle to minimize the rise in junction temperature. When pulsing techniques are used, oscillograph methods shall be used to measure V_{BE} and other necessary parameters, and the duty cycle and pulse width shall be specified.

FIGURE 3086-1. Test circuit for static input resistance.

3. Procedure. The resistor R_1 shall be made large. If the pulse method is used, resistor R_2 shall be chosen in combination with V_{CC} so that the specified collector current is achieved at a value of V_{CC} low enough to ensure that the device will not be operated in breakdown between pulses. If the pulse method is not used, resistor R_2 can be any convenient value. The current I_B and V_{CC} shall be adjusted until I_B and I_C achieve their specified values.

$$\text{Then:}\quad h_{IE} = \frac{V_{BE}}{I_B}$$

4. Summary. The following conditions shall be specified in the detail specification:

a. Pulse duty cycle and width, when required (see 3.).

b. Test voltages or currents (see 3.).

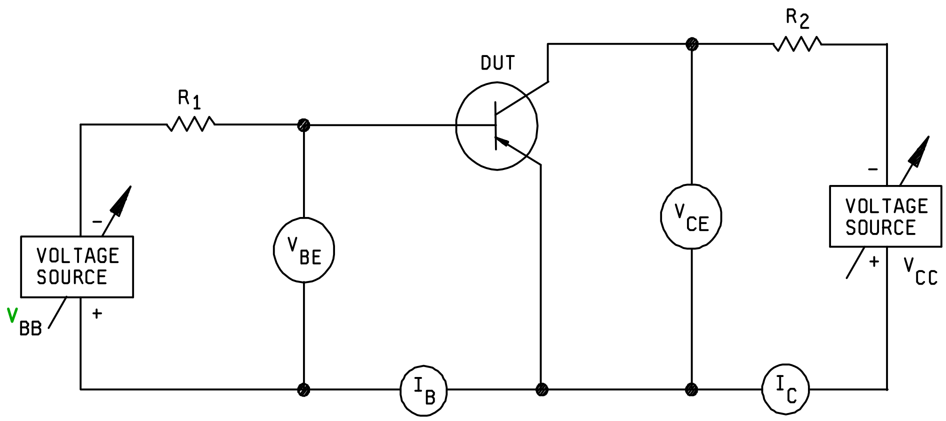
c. Parameter to be measured.

METHOD 3092.1

STATIC TRANSCONDUCTANCE

1. Purpose. The purpose of this test is to measure the static transconductance of the device under the specified conditions.

2. Test circuit. See figure 3092-1.



NOTE: For other configurations, the circuit may be modified in such a manner that it is capable of demonstrating device conformance to the minimum requirements of the individual specification.

FIGURE 3092-1. Test circuit for static transconductance.

3. Procedure. The resistor R_1 shall be made large or the voltage source V_{BB} shall be replaced by a constant current source. The resistor R_2 shall be chosen in combination with V_{CC} so that the specified collector current is achieved at a value of V_{CC} which is lower than $V_{(BR)CEO}$. The current I_B shall be adjusted until V_{CE} and I_C achieve their specified values. The current I_C or I_E and the voltages V_{BE}, V_{BC}, or V_{EB} shall then be measured. Using the values obtained through these measurements, the static transconductance shall be calculated as follows:

For common emitter | *For common collector* | *For common base*

$$g_{ME} = \frac{I_C}{V_{BE}} \qquad g_{MC} = \frac{I_E}{V_{BC}} \qquad g_{MB} = \frac{I_C}{V_{EB}}$$

If high current values are to be used in the measurement, suitable pulse techniques may be used to provide pulses of short-duty cycle to minimize the rise in junction temperature.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltage or current.

b. Duty cycle and pulse width, if applicable.

3100 Series

Circuit-performance and thermal-resistance measurements

For thermal-resistance measurements, at least three temperature sensitive parameters (TSP) of the transistor can be used; the collector to base cutoff current, I_{CBO}; the forward voltage drop of the emitter to base diode, V_{EB}; and the forward voltage drop of the collector to base diode, V_{CB}. The methods described in this standard refer to the thermal resistance between specified reference points of the device. For this type of measurement, power is applied to the device at two values of case, ambient, or other reference point temperature, such that identical values of I_{CBO}, V_{EB}, or V_{CB} are read during the cooling portion of the measurement.

METHOD 3100

JUNCTION TEMPERATURE MEASUREMENT AT BURN-IN & LIFE TEST

1. Purpose. This test is conducted on a representative sample of devices to verify a desired junction temperature (T_J) is achieved during burn-in and life-test environments. There are two methods that may be used. Both use a temperature sensitive parameter (TSP) that is initially measured at the desired T_J and selected test-current levels. In the first test method A, a selected low measuring current that does not cause significant self-heating is used (similar to thermal resistance test methods). In the second test method B, a series of sequential current pulses are taken to characterize the TSP at the desired T_J in the same operating current region expected for the burn-in and life-test environments. These TSP values are again later compared during burn-in or life-test to verify the same T_J. In either case, a direct sampling method of T_J in the burn-in or life test environment minimizes or eliminates possible errors introduced by ambient conditions, K factor, and non-linearity of component thermal resistance when applied at high temperatures. The method also allows the burn-in and life-test environment to be accurately characterized for thermal resistance junction to ambient ($R_{\theta JA}$) that can be used again to further advantage for similar products in the same test environment.

2. Scope. This applies to diode and transistor bipolar products requiring junction temperature verification during power burn-in that generates self-heating of T_J well above ambient or case temperature with applied power. It may also use an oven chamber or hot plate for achieving elevated ambient or case temperatures. The applied power testing may include ac operating life (ACOL) conditions for rectifiers, dc power in the operating breakdown region for zeners, and forward dc power conditions for signal diodes and others. Transistors also involve applied dc power conditions. This generally does not apply to high temperature reverse bais (HTRB) unless sufficient power is applied to cause significant self-heating. Equivalent heating power options are also described in method A to accommodate existing TSP equipment measurement methods for thermal resistance.

3. Rationale. Increased requirements for semiconductor performance, reliability, and quality have forced the need for knowledge and greater accuracy of semiconductor device junction temperatures at burn-in and life testing. This is necessary for making long-term calculations for reliability levels if using accelerating effects of burn-in or life testing. Accurate T_J measurements can be difficult because of the many variables. Electrical considerations (power, voltage-current levels, waveforms, etc), environmental consideration (mounting configuration, surroundings, mounting methodology, etc.) and selection of the junction temperature sensing method will affect results. It should also be noted that the thermal resistance characteristics of any semiconductor device are not necessarily constant with temperature or power dissipation, thus requiring thermal measurements under conditions that best duplicate actual operation in the burn-in or life-test environment for determining T_J.

4. Definitions. Many features are identical to those used for measuring thermal resistance for test method A. For both methods, the burn-in and life test environment shall simply be known as the "test environment." Further details may be found in other references including EIA-531, JESD51-1, and methods 3101, 3131, and 4081 of MIL-STD-750.

a. TSP Temperature sensitive parameter at the measuring current.

b. T_J Junction temperature.

c. T_A Ambient temperature in the test environment.

d. $R_{\theta JA}$ Thermal resistance from junction to ambient.

e. $R_{\theta JL}$ Thermal resistance from junction to lead.

f. $R_{\theta JC}$ Thermal resistance from junction to case.

g. $R_{\theta JEC}$ Thermal resistance from junction to end cap.

h. I_M Measuring current for the TSP (V_F or V_{BE}).

i. I_H Heating current.

j. t_H Heating time.

k. t_{MD} Measurement delay time

l. P_H Heating power.

m. V_F Forward voltage.

n. V_{BE} Base-emitter voltage.

o. V_{CE} Collector-emitter voltage.

p. I_C Collector current.

q. I_B Base current.

r. $V_{(BR)}$ Breakdown voltage.

s. V_Z Zener voltage.

t. I_F Forward current.

u. I_O Average I_F for 50 or 60 Hz sine wave and 180 degree conduction angle.

v. I_R Reverse standby current.

w. EC End cap.

x. DUT Device under test.

5. Equipment. Applicable to both methods unless otherwise noted.

5.1 TSP measurement. Test equipment to initially measure the TSP in a controlled temperature chamber, bath, or hot plate is required at a desired T_J for sample DUT.

5.2 Power supplies and arrays. The equipment used shall also include the burn-in or life-test power supplies and panel/socket arrays for electrical contacts or heat sinking where the T_J is to be sample measured for the DUTs. This “test environment” is the same as used for all other remaining devices intended for burn-in screening or life test.

5.3 Oven chamber. An oven chamber, bath, or hot plate to place the panel socket arrays with all the devices shall be used if elevated ambient temperatures are required.

5.4 Measuring TSP. For test method A, equipment for measuring the TSP shall be similar to that described for thermal resistance in EIA-531, JESD51-1, TM3101, TM3131, or TM4081. The TSP is sampled in a short measurement delay time (t_{MD}) after switching to a low measuring current I_M from the applied heating power source. The duty factor for sampling the TSP shall be 1percent or less of the heating time (t_H). It is considered optimum to use the same mode of power or heating current (I_H) as the power used in the test environment conditions. However, this method also allows for a dc forward heating current (I_H) power source often used in thermal resistance test methods to provide equivalent rms power.

5.5 Sample-and -hold tester. For test method B, a sample-and-hold tester for recording a sequential set of TSP measurements at operating currents in the same vicinity as the test environment operating current is required such as a Frothingham VF40 or equivalent with the approval of the quality activity. The test pulses must be kept narrow and widely spaced where additional heating of the junction will be insignificant.

5.6 Voltage and current measurements. In test method B, a voltmeter and current meter shall be used to accurately measure the expected voltage and current levels in the test.

5.7 Thermocouple. A small bare-wire thermocouple of 36 AWG is required for ACOL evaluation.

6. Procedure for method A. This method uses a selected low measuring current for the TSP that does not cause significant self-heating (similar to thermal resistance test methods). The DUTs are a sample of serialized devices where the TSP is initially recorded at the desired temperature. They shall also be of the same construction as other devices in the "test environment" and be of sufficient quantity to provide a good sample for averaging. Unless otherwise specified, this shall be a minimum of five devices.

6.1 TSP measurement. First determine the nominal T_J desired for the burn-in or life test. For military burn-in screening, the minimum T_J shall be specified by the applicable detail spec. The maximum T_J is the rating for the DUT unless otherwise specified.

6.1.1 Desired T_J. In a separate temperature controlled chamber, bath, or hot-plate environment, the nominal T_J desired for the burn-in or life test will initially be established within plus or minus 2°C (or as required) for recording the TSP. Additional T_J tolerance considerations are also noted in step 6.3.3.

6.1.2 Recording TSP. After the DUTs have been introduced and brought to thermal equilibrium, the TSP shall be recorded in a serialized manner at a low steady-state-measuring current (I_M) for method A. This would be the forward voltage of a diode (V_F) or base-emitter voltage (V_{BE}) of a transistor. The magnitude of I_M shall be large enough to ensure the V_F or V_{BE} is turned on, but not large enough to cause significant self-heating. For transistors, it is optimum to remove any bias voltage to the collector that generates current gain affecting I_M. However some thermal resistance equipment requires use of a collector voltage for a V_{BE} measurement. If so, that same test condition shall be used for measuring the TSP in burn-in as described in 6.3.2 and 6.4.1e.

6.2 Test environment mounting.

6.2.1 Verifing T_J. The sample DUTs shall then be mounted in the test environment using sockets strategically located representing the coolest and hottest regions to verify T_J. This shall also include all other devices intended for the power test environment to duplicate the same cumulative heating effects. Those sockets used for the DUTs shall also be the same design as all others in the test environment. The DUTs shall also be electrically connected to the TSP measuring equipment that requires a set of Kelvin-sense leads to monitor junction voltage. The leads shall be attached so as to minimize heat sinking. Also see step 6.5 on further ACOL considerations.

6.3 Test environment measurement.

6.3.1 Ambient temperature. The ambient temperature (T_A) shall be as specified at thermal equilibrium conditions including any convection or circulating air effects in an oven chamber where applicable. For hot-plate applications, the surface temperature and uniformity shall also be as specified to achieve desired case temperature (T_C) control as exemplified in 6.1.1 and 6.4.1c.

6.3.2 Appling current or power. The same heating current (or equivalent rms power) shall be applied in increasing increments for all devices while sampling for TSP on each DUT with a low duty factor at I_M in accordance with equipment description in 5.4. Working with each serialized DUT one at a time, monitor the junction voltage TSP at I_M while slowly increasing the heating current. The TSP will decline with increasing T_J for V_F or V_{BE}.

6.3.3 TSP for the desired T_J. Step 6.3.1 and 6.3.2 shall be repeated until the same TSP is achieved for the desired T_J in step 6.1.2 on the sample DUTs after the same equivalent current or rms power is applied for all devices in the test environment. The power applied for this desired T_J level for each DUT shall be recorded. The average power for the DUTs shall also be determined and used as the value thereafter for applied power per unit during burn-in or life test in step 6.3.4. If thermal resistance from junction to ambient $R_{\theta JA}$ is desired for future reference as described in 10.2, the T_A should also be recorded at this time.

NOTE: The T_J is also selected based on overall tolerances of the test environment. Also see 10.3 and EQ 9 for slight T_J variations with the averaging effects of applied power above. For worst-case tolerances, the T_J should be placed nominally at the midpoint between the minimum and maximum allowed T_J required for the test environment. For example this may be 155°C if the minimum is 135°C and maximum is 175°C. If either the applied heating-power P_H or the desired T_J exceeds the DUT ratings, see steps 6.3.3.1 and 6.3.3.2. If not, proceed to 6.3.4.

6.3.3.1 Current and power ratings. If applied heating current or power P_H exceeds the rating of the device for burn-in screening to achieve the desired T_J, the following options apply:

a. The heat sinking may be reduced in the test environment.

b. The ambient temperature (T_A) may be increased until the desired T_J is achieved when allowed in the applicable performance specification.

c. The current or power may be increased not to exceed the current density capability of the device.

6.3.3.2 T_J for JANS. The T_J may be higher than typical device ratings of 150°C to 200°C when applied to JANS life test of MIL-PRF-19500 for a faster accelerated test environment. These may be specified at T_J values of 225°C to 275°C. However these options shall not exceed temperatures where the DUTs (and remaining devices) cannot operate effectively as a semiconductor in the test environment. This may also be identified as the intrinsic or secondary breakdown region (thermal generation of electron-hole pairs starts approaching or exceeding the background doping levels of the pn junctions). This may also be observed by significant increases in reverse leakage current or in more severe cases the decline (or collapse) of reverse breakdown voltage V_{BR} on rectifiers, V_Z for higher voltage zeners, or V_{CE} for transistors. Also see note in 6.4.1b for rectifiers.

6.3.4 Criteria once T_J is achieved. After the desired T_J is achieved for all devices, the burn-in or life test may proceed with the average power per unit in 6.3.3 until completed for the required number of hours.

6.4 Power requirements. It is desirable to apply the same type of rms heating power required for the test environment in 6.3 for each DUT as applied to all other devices before switching to the I_M level for measuring the TSP. However power supply equipment for thermal resistance test methods using dc forward heating current I_H and a low duty factor sample-and-hold method at I_M for the TSP may not offer that added flexibility. In such cases, the same equivalent rms heating power (P_H) may be used with a forward-heating current (I_H) as described in thermal resistance test methods where $P_H = I_H \times V_H$. When equivalent rms heating power is in question, the duplication of lead, case, or end-cap temperatures (T_L, T_C or T_{EC}) is required to verify identical rms power as described in step 6.5 for ACOL considerations.

6.4.1 Test environment and DUT power options

a. Signal and Schottky Diodes (dc burn-in with I_F): The required heating power is forward dc current (I_F) multiplied times the forward voltage (V_F) observed during the dc burn-in or life test (or $P_H = I_F \times V_F$). No equipment handicaps should exist with this test environment since I_F equates to the forward heating current I_H for thermal resistance test methods.

b. Rectifiers (ACOL burn-in with I_O): The required ac operating life at rated I_O may be approximated in equivalent rms heating power by $P_H = I_O(0.107 + 0.785\ V_{FM})$ where V_{FM} is the peak forward voltage observed during the half-sine wave and I_O is the rated average rectified output current for 50 Hz or 60 Hz sine-wave input and a 180 degree conduction angle (see JESD282-B). With this definition, the peak forward current in each half-sine wave is $3.14 \times I_O$. This P_H also assumes the power in the reverse direction is negligible due to leakage current (I_R) and applied reverse voltage (V_{RRM}) as defined in JESD282-B or method 1038 of MIL-STD-750.

For equipment limitations to measure TSP, the DUT samples may also use the same effective forward power where P_H is the forward heating current I_H multiplied times the forward heating voltage V_H as described in 6.4. The same effective power with ACOL may be verified with identical T_L, T_C or T_{EC}. See step 6.5 to measure T_L, T_C, or T_{EC}. Also see Background information in 9.3 for the "Correlation of RMS Power with T_L, T_C or T_{EC}".

NOTE: A reverse power loss may not be observed if "limiting resistors" have externally absorbed the intended reverse voltage (V_{RRM}) in an ACOL test environment due to high leakage currents ($I_R \times R$ voltage drop), or due to collapsing voltage as described in 6.3.3.2. The required V_{RRM} must be sample monitored to verify it has been successfully applied where applicable to all the other remaining rectifier devices under ACOL power. Limiting or ballast resistors are often used in series with each device that are then placed in parallel array connections with typical power supplies for burn-in or life test methods. This regulates I_O or limits excessive current flow if a device electrically degrades or shorts to allow continued burn-in or life testing of remaining devices for the period of time required.

c. Schottky (HTRB burn-in with I_R): To minimize high power and burn-in current levels, the required P_H is applied as an HTRB with reverse voltage (V_R) and selected range of reverse current (I_R) for all devices at elevated temperature. At low power where there is no significant self-heating, the T_C may be assumed the same value as T_J. In this example, the $P_H = I_R \times V_R$ where I_R is increased at elevated temperature. For test equipment options the DUT sample may also use the equivalent forward rms power (P_H) as described in 6.4. Where applicable, the T_C may simply be measured directly for the T_J equivalent as described in 8.

d. Zeners (dc burn-in with I_Z): The required P_H is the zener burn-in current (I_Z) multiplied times the nominal zener voltage (V_Z) where $P_H = I_Z \times V_Z$. The V_Z is also adjusted for the expected T_J using the rated temperature coefficient of the zener (α_{VZ}). For equipment limitations, the DUT sample may use the equivalent forward rms power (P_H) as described in 6.4.

e. Transistors (dc burn-in with I_C): The required heating power is the collector current (I_C) multiplied times the collector emitter voltage (V_{CE}) during the dc burn-in or life test plus any significant base current (I_B) multiplied times base-emitter voltage (V_{BE}) where $P_H = I_C \times V_{CE} + I_B \times V_{BE}$. Typically the $I_B \times V_{BE}$ power may be negligible. The low duty factor sample measurement for the TSP shall be with the same conditions as in step 6.1.2.

6.5 ACOL considerations (rectifiers). If the parts for burn-in or life test are to receive ACOL conditions, an additional step must be added after step 6.2.1 to ensure equivalent heating and T_J to the DUT samples.

6.5.1 Thermocouple mounting. When the voltage monitoring leads are being attached to the DUTs for testing in the burn-in configuration in step 6.2.1, also solder on a fine 36 AWG bare-wire thermocouple to each of them. The thermocouple should be mounted at zero distance from the body of the part. The thermocouple must be mounted to not interfere when the DUT is placed in the burn-in or life test fixtures.

6.5.2 Thermocouple usage. Also solder a thermocouple as described in 6.5.1 to the nearest device of each DUT location that receives ACOL power in the test environment.

6.5.3 Thermocouple temperature. As each of the serialized DUT parts are set to the desired junction temperature using the dc current method in the burn-in or life-test environment, also record the thermocouple temperature reading. These thermocouple readings are then used to set the ac power levels in the next step.

6.5.4 Average T_J. Apply power to heat the remaining diodes using the required ACOL while monitoring the thermocouple temperature. Increase the ac power input until the thermocouple in 6.5.2 reaches the temperature level of the DUTs in 6.5.3 at the desired junction temperature. Record the ACOL power conditions applied for each device described in 6.5.2. These values are then averaged for determining ACOL power applied for all devices. This process guarantees that all the devices will be tested at the required average junction temperature for burn-in or life test. Also see 9.3 for further background information.

NOTE: The rectifier diode with the lowest V_F and (or) the lowest ambient temperature T_A position in the test environment would require the greatest power for a given thermocouple reading to ensure the same T_J is achieved.

7. Procedure for method B. This method uses a sequential set of current pulses to characterize the TSP at the T_J in the same operating current region expected for the burn-in or life-test environment. The DUTs are a sample of devices where the TSP is recorded at the desired temperature. They shall also be of the same construction as other devices in the test environment and shall be of sufficient quantity to provide a good sample for averaging. Unless otherwise specified, this shall be a minimum of five devices.

7.1 TSP measurement. First determine the nominal T_J desired for the burn-in or life test. For military burn-in screening, the minimum T_J shall be specified by the applicable performance specification. The maximum T_J is the rating for the DUT unless otherwise specified.

7.1.1 T_J desired. In a separate temperature controlled chamber, bath, or hot plate environment, the nominal T_J desired for the burn-in or life test will initially be established within plus or minus 2°C (or as required) for recording the TSP. Additional T_J tolerance considerations are also noted in 7.3.3.

7.1.2 Recording TSP measurements. A sample-and-hold tester must be programmed for recording a sequential set of TSP measurements at operating currents in the same vicinity as anticipated for the test environment. This will perform incremental pulse V_F-I_F, V_Z-I_Z, or V_{BE}-I_{CE} tests.

a. Choose the incremental current range so that the recorded values will be centered near the current level that is expected for the burn-in or life test environment.

b Program the sample-and-hold test equipment to record junction TSP voltage readings with a sufficiently low duty factor that will not warm the DUT when taking sequential readings. Typical test parameters for a leaded-switching diode might be as follows:

(1) 0.5 ms pulse width.

(2) 1 second wait interval.

(3) 500 mA starting level for I_F.

(4) 20 steps at 5 mA increasing increments.

NOTE: The smaller the incremental steps, the more accurate the chart will be when correlating to values taken in burn-in or life test. Since this test is performed with a low duty-factor power and thermally stable parts, any holding fixture may be used, but Kelvin leads are required.

7.1.3 Data. After the DUTs have been introduced and brought to thermal equilibrium, the TSP shall be recorded in a serialized manner by cycling each part through the expected current range and printing out the data for each identified device. Each set of data is applicable only for that particular serialized part and junction temperature.

7.2 Test environment mounting

7.2.1 Verify T_J. The sample DUTs shall then be mounted in the test environment using sockets strategically located representing the coolest and hottest regions to verify T_J. All other devices intended for burn-in or life-test shall also be mounted in the test environment to duplicate the same cumulative heating effects. Those sockets used for the DUTs shall also be the same design as all others in the test environment. The DUTS shall also be electrically connected to the TSP measuring equipment that requires a set of Kelvin sense leads to monitor junction voltage. These leads shall be attached so as to minimize heat sinking. Also see step 7.4 for ACOL considerations.

7.3 Test environment measurement.

7.3.1 Thermal equilibrium. The ambient temperature (T_A) shall be as specified at thermal equilibrium conditions including any convection or circulating air effects in an oven chamber where applicable.

7.3.2 Desired level. A common heating current shall be applied in increasing increments for all devices while sampling for TSP on each DUT. Working with each serialized DUT one at a time, monitor the junction voltage TSP while slowly varying the common junction current. When the DUT being monitored is at thermal equilibrium where both its current and voltage readings match a set of readings on the chart taken in step 7.1.3, the T_J of that DUT is known to be at the desired level. This is graphically displayed on Figure 3100-1. For accuracy, the voltage readings should optimally use the same test equipment that can record in both a sample-and-hold mode in step 7.1.3 and continuously in this step.

7.3.3 Desired T_J. Paragraph 7.3.2 shall be repeated until both the current and voltage readings match a set of corresponding readings for the desired T_J level on each serialized DUT after the same equivalent rms power is applied for all devices in the test environment. The power applied for this desired T_J level for each DUT shall be recorded. The average power for the DUTs shall also be determined and used as the value thereafter for applied power per unit during burn-in or life test in 7.3.4. If the thermal resistance from junction to ambient $R_{\theta JA}$ is desired for later reference as indicated in 10.2, the T_A should also be recorded.

NOTE: The T_J is also selected based on overall tolerances of the test environment. Also see paragraph 10.3 and EQ 9 for slight T_J variations with the averaging effects of applied power above. For worst-case tolerances, the T_J should be placed nominally at the midpoint between the minimum and maximum allowed T_J required for the test environment. For example this may be 155°C if the minimum is 135°C and maximum is 175°C. If either the applied heating-power P_H or the desired T_J exceeds the DUT ratings, see 7.3.3.1 and 7.3.3.2. If not, proceed to 7.3.4.

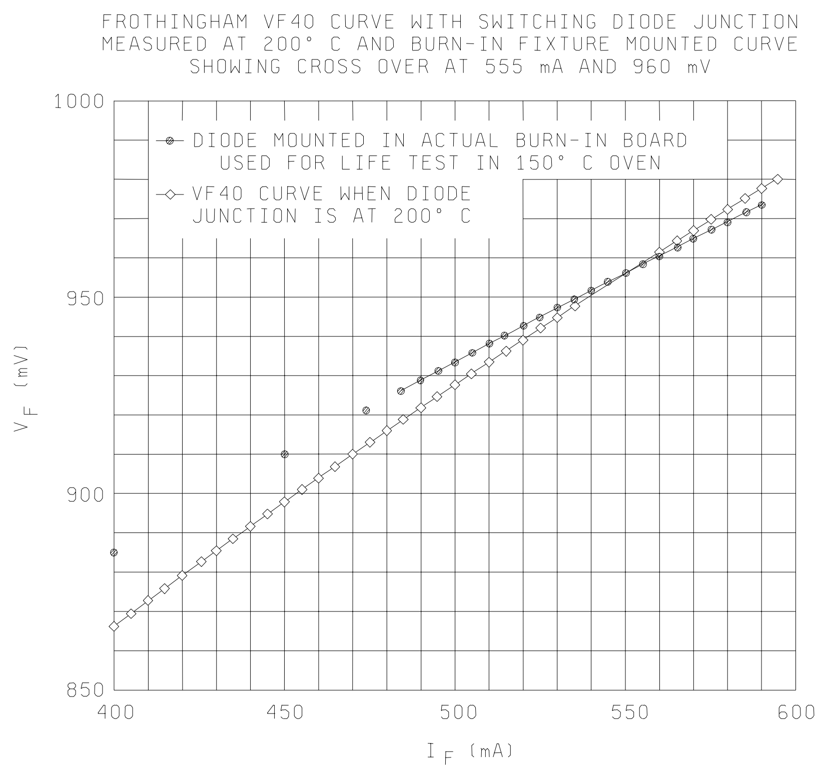


FIGURE 3100-1. Frothingham VF40 curve.

7.3.3.1 Power rating. If the applied heating power P_H exceeds the rating of the device for burn-in screening to achieve the desired T_J, the following options apply:

a. The heat sinking may be reduced in the test environment.

b. The ambient temperature T_A may be increased until the desired T_J is achieved when allowed by the applicable performance specification.

c. The current or power may be increased not to exceed the current density capability of the device.

7.3.3.2 T_J for JANS. The T_J may be higher than typical device ratings of 150°C to 200°C when applied to JANS life test in groups B, C, and E of MIL-PRF-19500 for a faster accelerated test environment. These may be specified at T_J values of 225°C to 275°C. However these options shall not exceed temperatures where the DUTs (and remaining devices) cannot operate effectively as a semiconductor in the test environment. This may also be identified as the intrinsic or secondary breakdown region (thermal generation of electron-hole pairs starts approaching or exceeding the background doping levels of the pn junctions). This may also be observed by significant increases in reverse leakage current or in more severe cases the decline (or collapse) of reverse breakdown voltage V_{BR} on rectifiers, V_Z for higher voltage zeners, or V_{CE} for transistors. Also see note in 6.4.1b for rectifiers.

7.3.4 Desired T_J After the desired T_J is achieved for all devices, the burn-in or life test may proceed with the average power per unit in 7.3.3 until completed for the required number of hours.

7.4 ACOL considerations (rectifiers). If the sample-and-hold test equipment is equipped with synchronized test capabilities for measuring the TSP voltage in the desired forward conducting half-cycle region for ACOL operation, this can again be tested in a similar manner described in 7.3. As described in 7.3.2, this should optimally be provided with the same voltage test equipment. For synchronized capabilities, a Frothingham model VF40DB or equivalent may be used. If a synchronized test capability is not available, alternative steps must be added after step 7.2.1 to ensure equivalent heating and T_J to the DUT samples. These are described in 7.4.1 through 7.4.4.

7.4.1 Thermocouple mounting. When the voltage monitoring leads are being attached to the DUTs for testing in the burn-in configuration in 7.2, also solder on a fine 36 AWG bare-wire thermocouple to each of them. The thermocouple should be mounted at zero inch distance from the body of the part. The thermocouple will have to be mounted so as to not interfere when the DUT is placed in the burn-in or life test fixtures.

7.4.2 Thermocouple usage. Also solder a thermocouple as described in 7.4.1 to the nearest device of each DUT location that receives ACOL power in the test environment.

7.4.3 Thermocouple temperature. As each of the serialized DUT parts is set to the desired junction temperature using the dc current method in the ACOL test environment, also record the thermocouple temperature reading. These thermocouple readings are then used to set the ac power levels in the next step.

7.4.4 Average T_J. Apply power to heat the remaining diodes using the required ACOL while monitoring the thermocouple temperature. Increase the ac power input until the thermocouple in 7.4.2 reaches the temperature level of the DUT in 7.4.3 at the desired junction temperature. Record the ACOL power conditions applied for each device described in 7.4.2. These values are then averaged for determining ACOL power applied for all devices. This process guarantees that all the devices will be tested at the required average junction temperature for burn-in or life test. Also see 9.3 for further background information.

NOTE: The rectifier diode with the lowest V_F and (or) the lowest ambient temperature (T_A) position in the test environment would require the greatest power for a given thermocouple reading to ensure the same T_J is achieved.

8. Procedure for method C. This method only applies to case mounted power devices where the operating power or current region expected for the burn-in or life-test environment is still well below that of the rating of the device. In these examples, the T_J of the device is not significantly higher than the case temperature T_C. This operating feature and direct measurement of case temperature may be used to confirm the minimum required T_J is met for the burn-in or life-test environment.

9. Background information.

9.1 Equations for T_J, T_A, P_H, and $R_{\theta JA}$. The observed values of the T_J rise above T_A in the test environment would be the product of effective rms heating power (P_H) multiplied times the total effects of component thermal resistance from junction to ambient ($R_{\theta JA}$).
This may also be stated as follows:

$$T_J = T_A + P_H \times R_{\theta JA} \qquad \text{EQ 1}$$

The T_A is the ambient temperature in the immediate vicinity of an open-burn-in rack or the ambient inside a convection-oven chamber for life test. If T_A is recorded at step 6.3.3 or 7.3.3, then the $R_{\theta JA}$ can also be determined as follows:

$$R_{\theta JA} = (T_J - T_A)/P_H \qquad \text{EQ 2}$$

9.2 Thermal resistance definitions for $R_{\theta JL}$, $R_{\theta JC}$, $R_{\theta JEC}$, $R_{\theta LA}$, $R_{\theta CA}$, and $R_{\theta ECA}$. The thermal resistance $R_{\theta JA}$ is the total of the DUT thermal resistance junction to lead or case ($R_{\theta JL}$ or $R_{\theta JC}$), and the thermal resistance of the test environment from lead or case (test socket) to ambient ($R_{\theta LA}$ or $R_{\theta CA}$). For example:

$$R_{\theta JA} = R_{\theta JL} + R_{\theta LA}$$

or

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

This also applies to surface mount devices that may use an end cap (EC) reference rather than case. In this example:

$$R_{\theta JA} = R_{\theta JEC} + R_{\theta ECA}$$

The T_J in each of these examples can be determined as follows:

$$T_J = T_A + P_H \times (R_{\theta JL} + R_{\theta LA}) = T_L + P_H \times R_{\theta JL} \qquad \text{EQ 3}$$

$$T_J = T_A + P_H \times (R_{\theta JC} + R_{\theta CA}) = T_C + P_H \times R_{\theta JC} \qquad \text{EQ 4}$$

$$T_J = T_A + P_H \times (R_{\theta JEC} + R_{\theta ECA}) = T_{EC} + P_H \times R_{\theta JEC} \qquad \text{EQ 5}$$

Earlier methods have also determined T_J based on these relations that use thermal resistance of the component and also the reference point temperature (T_L, T_C, T_{EC}) measured in the test environment with applied power P_H. Possible sources of error included the use of maximum rated thermal resistance rather than actual value (see note), nonlinear features affecting thermal resistance or K factor at notably higher temperatures during life test, and difficulty in measuring reference temperature (T_L, T_C, T_{EC}) particularly for enclosed convection air ovens.

NOTE: For accurate determination of T_J, this requires the actual component thermal resistance value rather than the maximum rating. This distinction is important to ensure adequate T_J values are achieved in 6.3.3 or 7.3.3.

9.3 Correlation of RMS power with T_L, T_C, or T_{EC}. The lead, case, or end-cap temperature reference points within the test environment are as follows:

$$T_L = T_A + P_H \times R_{\theta LA} \qquad \text{EQ 6}$$

$$T_C = T_A + P_H \times R_{\theta CA} \qquad \text{EQ 7}$$

$$T_{EC} = T_A + P_H \times R_{\theta ECA} \qquad \text{EQ 8}$$

If the T_L, T_C or T_{EC} is the same between any two devices in identical test environment conditions for ambient temperature and thermal resistance of the test socket from component to ambient, then the effective rms power must be the same between them as may be observed in EQ 6, 7, and 8. This feature may be used to advantage in determining equivalent heating power levels in different power modes as described in 6.5 and 7.4. Also when the same equivalent heating power levels are applied to devices of identical design with the same thermal resistance at the same T_L, T_C or T_{EC}, then the same T_J is achieved as shown in EQ 3, 4, and 5.

10. Summary.

10.1 Repeatable T_J values. This procedure may not require repeating for every lot processed for burn-in and life-test if this method verifies the same T_J values (within acceptable tolerances) for thermally identical test environments and devices to be tested as demonstrated in 9.1 and EQ 1. This would occur in a test environment with the same T_A and heat-sinking effects ($R_{\theta LA}$, $R_{\theta CA}$, or $R_{\theta ECA}$), as well as components of the same thermal resistance ($R_{\theta JL}$, $R_{\theta JC}$, or $R_{\theta JEC}$). These conditions provide the same effective $R_{\theta JA}$ and the same T_J values as demonstrated in 9.2. The value of $R_{\theta JA}$ is determined by the following in 10.2.

10.2 The effective thermal resistance. $R_{\theta JA}$ for the test environment can be determined for the devices or DUTs with the heating power P_H recorded at 6.3.3 or 7.3.3 with ambient temperature (T_A) and junction temperature (T_J) with EQ 2 in 9.1. The $R_{\theta JA}$ for identical test environments and products can then be used to advantage for determining other desired T_J values when needed at applied power levels P_H or ambient temperature (T_A) conditions.

10.3 Average power. When an individual (average) power level P_H is selected for the test environment in 6.3.3 or 7.3.3, small variations in power ΔP_H to this average will exist over the sample number of DUTs to achieve the same TSP or T_J. As a result, slight variations in ΔT_J will also occur for continuing the burn-in or life test in 6.3.4 or 7.3.4 with typical power supplies and wiring harnesses. This ΔT_J may also be determined from EQ 1 as shown below in EQ 9.

$$\Delta T_J = T_A + \Delta P_H \times R_{\theta JA} \qquad \text{EQ 9}$$

This added consideration for T_J tolerances in 6.3.3 or 7.3.3 is of interest since the same operating current or power condition is applied to all devices for continuing burn-in or life test in 6.3.4 or 7.3.4 with typical power supplies and wiring harnesses. These slight T_J variations may be from small variations in socket and component thermal resistance. It may also be from notable variations in ambient temperature in the immediate vicinity of each DUT placed at different locations in the test environment.

METHOD 3101.3

THERMAL IMPEDANCE (RESPONSE) TESTING OF DIODES

1. Purpose. The purpose of this test is to determine the thermal performance of diode devices. This can be done in two ways, steady-state thermal impedance or thermal transient testing. Steady state thermal impedance (referred to as thermal resistance) determines the overall thermal performance of devices. A production-oriented screening process, referred to as thermal transient testing, is a subset of thermal impedance testing and determines the ability of the diode chip-to-header interface to transfer heat from the chip to the header, and is a measure of the thermal quality of the die attachment. It is relevant to designs which use headers, or heat conducting plugs, with mass and thermal conductivity allowing effective discrimination of poor die attachments. This is particularly true with power devices. The method can be applied to rectifier diodes, transient voltage suppressors, power zener diodes, and some zener, signal and switching diodes. This method is intended for production monitoring, incoming inspection, and pre-burn in screening applications. Some zener constructions, particularly when used with small junction area designs, cool too rapidly (from a heating current) to provide accurate measurement when forward (diode) current is used for this test. For such devices, a method is provided to apply currents in the zener direction and make a measurement much closer to the termination of the heating current. In this way, no minority carriers are involved and inductive effects are minimized due to lower test current. This may be considered a lab measurement because cable lengths in an ATE may prevent accurate measurements so close to cessation of the heating current. This laboratory method is intended on initial zener device design verification for correlation to forward direction thermal impedance testing (such as with ATE) prior to establishing a production test limit. Correlation assurance must be provided in the forward production monitoring that thermal impedance in the reverse direction (zener) must not exceed the specified limit. If this zener test method exceeds the forward method by 10 percent or more, production monitoring (with an ATE in the forward direction) will require a lower limit, for some devices, than that required by the more accurate lab method (see 5.1).

1.1 Background and scope for thermal transient testing. Steady-state thermal response (transient thermal impedance) of semiconductor devices are sensitive to the presence of these voids in the die attachment material between the semiconductor chip and package since voids impede the flow of heat from the chip to the substrate (package). Due to the difference in the thermal time constants of the chip and package, the measurement of transient thermal response can be made more sensitive to the presence of voids than can the measurement of steady-state thermal response. This is because the chip thermal time constant is generally several orders of magnitude shorter than that of the package. Thus, the heating power pulse width can be selected so that only the chip and the chip-to-substrate interface are heated during the pulse by using a pulse width somewhat greater than the chip thermal time constant but less than that of the substrate. Heating power pulse widths ranging from 1 to 400 ms for various package designs have been found to satisfy this criterion. This enables the detection of voids to be greatly enhanced, with the added advantage of not having to heat sink the DUT. Thus, the transient thermal impedance or thermal response techniques are less time-consuming than the measurement of thermal resistance for use as a manufacturing screen, process control, or incoming inspection measure for die attachment integrity evaluation.

2. Definitions. The following symbols and terminology shall apply for the purpose of this test method in the forward direction: (When using the zener method, see NOTES below):

a. V_F: The forward biased junction voltage of the DUT used for junction temperature sensing.
NOTE: When using the zener method, delete “forward” and use “zener” bias.
V_{Fi}: The initial V_F value before application of heating power.
V_{Ff}: The final V_F value after application of heating power.

b. ΔV_F The change in the TSP, V_F, due to the application of heating power to the DUT.

c. I_H: The current applied to the DUT during the heating time in order to cause power dissipation.

d. V_H: The heating voltage resulting from the application of I_H to the DUT.

e. P_H: The heating power pulse magnitude; product of V_H and I_H.

f. t_H: The duration of P_H applied to the DUT.

g. I_M: The measurement current used to forward bias the temperature sensing diode junction for measurement of V_F.

NOTE: When using the zener, delete “forward” and use “zener” bias.

h. t_{MD}: Measurement delay time is defined as the time from the start of heating power (P_H) removal to the start of the final V_F measurement time, referred to as t_{SW}.

i. t_{SW}: Sample window time during which final V_F measurement is made. The value of t_{SW} should be small; it can approach zero if an oscilloscope is used for manual measurements.

j. VTC: Voltage-temperature coefficient of V_F with respect to T_J at a fixed value of I_M; in mV/°C.

k. K: Thermal calibration factor equal to the reciprocal of VTC; in °C/mV.

l. CU: The comparison unit, consisting of ΔV_F divided by V_H, that is used to normalize the transient thermal response for variations in power dissipation; in units of mV/V.

m. T_J: The DUT junction temperature.

n. ΔT_J: The change in T_J caused by the application of P_H for a time equal to t_H.

o. $Z_{\theta JX}$: Thermal impedance from device junction to a time defined reference point; in units of °C/W.

p. $Z_{\theta JC}$: Thermal impedance from device junction to a point on the outside surface of the case immediately adjacent to the device chip measured using time equal time constant of device; in units of °C/W.

q. $R_{\theta JX}$: Thermal resistance from device junction to a defined reference point; in units of °C/W.

$R_{\theta JC}$: Thermal resistance from device junction to a point on the outside surface of the case immediately adjacent to the device chip; in units of °C/W.

$R_{\theta JA}$: Thermal resistance from device junction to an ambient (world); in units of °C/W.

*r. TSP: The temperature sensitive parameter of V_F or V_Z.

*s. V_Z: The zener voltage. (Also see note 1.)

NOTES: 1. When using the zener method, the following changes shall further apply to the definitions whenever they appear in the text.

Letter symbols: I_F becomes I_Z
V_F becomes V_{ZL}
V_H becomes V_{ZH}
V_{Fi} becomes V_{ZLi}
V_{Ff} becomes V_{ZLf}
ΔV_F becomes ΔV_{ZL}
wording: “forward” bias becomes “reverse” bias

2. ΔV_F, K, and CU parameter values will be substantially different when using the zener method (as

compared to the forward biased method). Some difference will be observed between zeners with different nominal voltages.

3. Apparatus. The apparatus required for this test shall include the following, configured as shown on figure 3101-1, as applicable to the specified test procedure:

a. A constant current source capable of adjustment to the desired value of I_H and able to supply the V_H value required by the DUT. The current source should be able to maintain the desired current to within ±2 percent during the entire length of heating time.

b. A constant current source to supply I_M with sufficient voltage compliance to turn the TSP junction fully on.

c. An electronic switch capable of switching between the heating period conditions and measurement conditions in a time frame short enough to avoid DUT cooling during the transition; this typically requires switching in the microsecond or tens of microseconds range.

d. A voltage measurement circuit capable of accurately making the V_{Ff} measurement within the time frame with millivolt resolution.

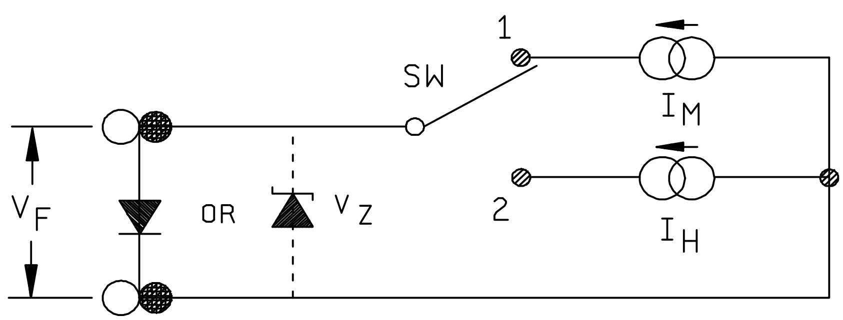
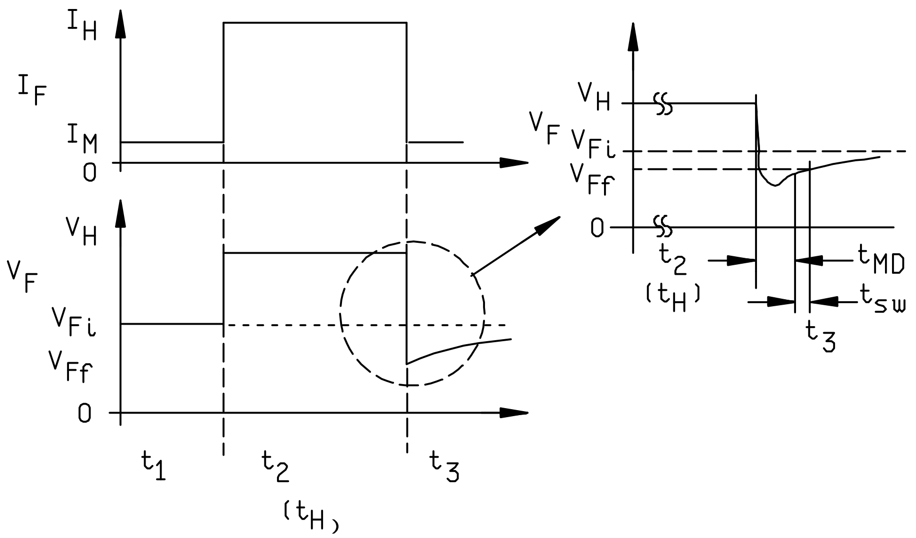


FIGURE 3101-1. Thermal impedance testing setup for diodes.

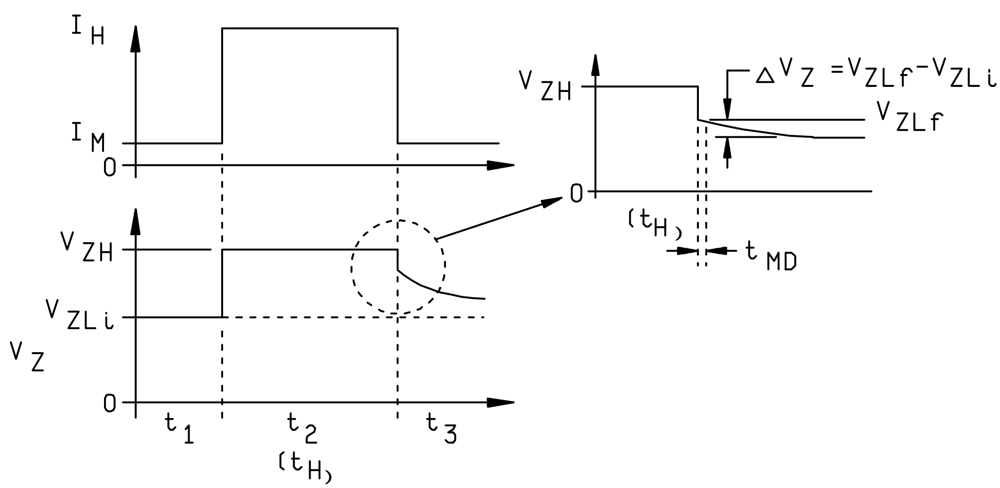
4. Test operation.

4.1 General description. The test begins with the adjustment of I_M and I_H to the desired values. The value of I_H is usually at least 50 times greater than the value of I_M. Then with the electronic switch in position 1, the value of V_{Fi} is measured. The switch is then moved to position 2 for a length of time equal to t_H and the value of V_H is measured. Finally, at the conclusion of t_H, the switch is again moved to position 1 and the V_{Ff} value is measured within a time period defined by t_{MD} (or t_{MD} + t_{SW}, depending on the definitions stated previously). The two current sources are then turned off at the completion of the test.



Forward biased method

FIGURE 3101-2a. Thermal impedance testing waveforms.



Zener biased method

FIGURE 3101-2b. Thermal impedance testing waveforms - Continued.

4.2 Notes.

a. Some test equipment may provide a ΔV_F directly instead of V_{Fi} and V_{Ff}; this is an acceptable alternative. Record the value of ΔV_F.

b. Some test equipment may provide $Z_{\theta JX}$ directly instead of V_{Fi} and V_{Ff} for thermal resistance calculations; this is an acceptable alternative. Record the value of $Z_{\theta JX}$.

c. Alternative waveforms, as may be generated by ATE using the general principles of this method, may be used upon approval of the qualifying activity.

*d. The zener biased method in Fig 3101-2b illustrates a positive TSP when the zener is in avalanche breakdown. It is also possible to portray a negative TSP for low voltage zeners when they are in the field-emmission or tunneling mode. A near-zero TSP can also result from these two off-setting factors of a specific operating current that must be avoided by changing to a higher or lower current. Also see paragraph 6 for TSP.

5. Acceptance limit.

5.1 General discussion. Variations in diode characteristics from one manufacturer to another cause difficulty in establishing a single acceptance limit for all diodes tested to a given specification. Ideally, a single acceptance limit value for ΔV_F would be the simplest approach. However, different design, materials, and processes can alter the resultant ΔV_F value for a given set of test conditions. Listed below are several different approaches to defining acceptance limits. The ΔV_F limit is the simplest approach and is usually selected for screening purposes. 5.3 through 5.6 require increasingly greater detail or effort. In some examples, absolute thermal impedance limits are required for correlation to surge performance such as for zeners. In such examples, setting a limit for zener diode construction with the forward biased (usual ATE) method requires prior evaluation of $Z_{\theta JX}$ (and $R_{\theta JX}$, when desired) by the zener biased method. If the zener method result is more than 10 percent higher, the limit shall be based on the more accurate zener biased measurement. In such case, if it is desired to use the forward biased method, the limit (of ΔV_F, $Z_{\theta JX}$, or $R_{\theta JX}$) shall be reduced by the extent (percentage) difference between the two methods.

5.2 ΔV_F limit. A single ΔV_F limit is practical if the K factor and V_H values for all diodes tested to a given specification are nearly identical. Since these values may be different for different manufacturers, the use of different limits is likely to more accurately achieve the desired intent. (A lower limit does not indicate a better die bond when comparing different product sources.) The diode specifications would list the following test conditions and measurement parameters:

I_H (in A)

t_H (in ms)

I_M (in mA)

t_{MD} (in µs)

t_{SW} (in µs)

ΔV_F (maximum limit value, in mV)

5.3 ΔT_J limit. (Much more involved than ΔV , but useful for examining questionable devices.) Since ΔT_J is the product of K (in accordance with 6.) and ΔV_F, this approach is the same as defining a maximum acceptable junction temperature rise for a given set of test conditions.

5.4 CU limit. (Slightly more involved than ΔT_J.) The ΔT_J limit approach described above does not take into account potential power dissipation variations between devices. The V_H value can vary, depending on chip design and size, thus causing the power dissipation during the heating time to be different from device to device. This variation will be small within a lot of devices produced by a single manufacturer but may be large between manufacturers. A CU limit value takes into account variations in power dissipation due to differences in V_H by dividing the ΔV_F value by V_H.

5.5 (K•CU) limit. (Slightly more involved but provides greater detail.) This is a combinational approach that takes into account both K factor and power dissipation variations between devices.

5.6 $Z_{\theta JX}$ limit. (For full characterization; not required for screening purposes, but preferred if the proper ATE is available.) The thermal impedance approach uses an absolute magnitude value specification that overcomes the problems associated with the other approaches. Thermal impedance is time dependent and is calculated as follows:

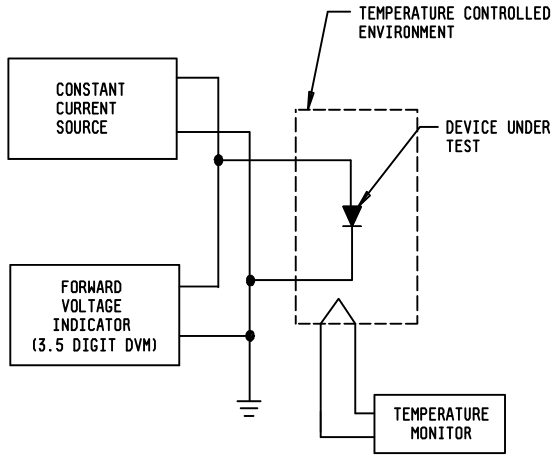
$$Z_{\Theta JX} = \frac{\Delta T_J}{P_D} = \left| \frac{(K)(\Delta V_F)}{(I_H)(V_H)} \right| {}^{o}\mathrm{C/W}$$

5.7 $R_{\theta JX}$ limit. (For thermal resistance specification testing.) The thermal resistance to some defined point, such as the case, is an absolute magnitude value specification used for equilibrium conditions. The t_H heating time must therefore be extended to appreciably longer times (typically 20 to 50 seconds). In the example of $R_{\theta JC}$ measurements, the case must be carefully stabilized and monitored in temperature which requires an infinite heat sink for optimum results. The ΔT_J is the difference in junction temperature to the case temperature for the example of $R_{\theta JC}$.

$$R_{\Theta JX} = \frac{\Delta T_J}{P_D} = \left| \frac{(K)(\Delta V_F)}{(I_H)(V_H)} \right| {}^{o}\mathrm{C/W}$$

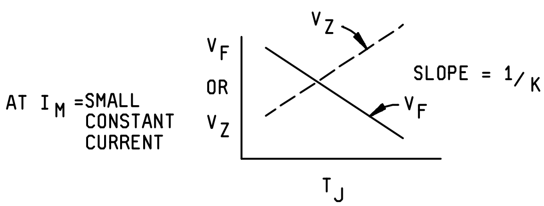
5.8 General comment for thermal transient testing. One potential problem in using the thermal transient testing approach lies in trying to make accurate enough measurements with sufficient resolution to distinguish between acceptable and nonacceptable diodes. As the diode-under-test current handling capability increases, the thermal impedance under transient conditions will become a very small value. This raises the potential for rejecting good devices and accepting bad ones. Higher I_H values must be used in this case.

*6. Measurement of the TSP V_F (or V_Z). The calibration of V_F versus T_J is accomplished by monitoring V_F for the required value of I_M as the environmental temperature (and thus the DUT temperature), and is varied by external heating. It is not required if the acceptance limit is ΔV_F (see 5.2), but is relevant to the other acceptance criteria (see 5.3 through 5.6). The magnitude of I_M shall be chosen so that V_F is a linearly decreasing function over the normal T_J range of the device. I_M must be large enough to ensure that the diode junction is turned on but not large enough to cause significant self-heating. An example of the measurement method and resulting calibration curve is shown on figure 3101-3.



Step 1: Measure V_{F1} at T_{J1} using I_M
Step 2: Measure V_{F2} at T_{J2} using I_M

Step 3: $$K = \left|\frac{T_{J2} - T_{J1}}{V_{F2} - V_{F1}}\right| \,^\circ C / mV$$



I_M: must be large enough to overcome surface leakage effects but small enough not to cause significant self-heating.
*When using the zener direction, the I_M may also require adjustment to avoid a near zero TSP where the avalanche breakdown effects are offset by tunneling or field emission. (See 4.2, note d.)

T_J: is externally applied: (e.g., via oven, liquid) environment.

FIGURE 3101-3. Example curve of V_F versus T_J.

A calibration factor K (which is the reciprocal of the slope of the curve on figure 3101-3) can be defined as:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{F2} - V_{F1}} \right| \ °C/mV$$

*It has been found experimentally that the K-factor variation for all devices within a given device type class is small. The usual procedure is to perform a K factor calibration on a 10 to 12 piece sample from a device lot and determine the average K and standard deviation (σ). If σ is less than or equal to three percent of the average value of K, then the average value of K can be used for all devices within the lot. If σ is greater than three percent of the average value of K, then all the devices in the lot shall be calibrated and the individual values of K shall be used in determining device acceptance. As an alternative to using individual values of K, the manufacture may establish internal limits unique to their product that ensures atypical product removal from the population (lot-to-lot and within-the-lot). The manufacture shall use statistic techniques to establish the limits to the satisfaction of the government.

7. Establishment of test conditions and acceptance limits. Thermal resistance measurements require that I_H be equal to the required value stated in the device specifications, typically at rated current or higher. Values for t_H, t_{MD}, and heat sink conditions are also taken from the device specifications. The steps shown below are primarily for thermal transient testing and thermal characterization purposes.

The following steps describe how to set up the test conditions and determine the acceptance limits for implementing the transient thermal test for die attachment evaluation using the apparatus and definitions stated above.

7.1 Initial device testing procedure. The following steps describe in detail how to set up the apparatus described previously for proper testing of various diodes. Since this procedure thermally characterizes the diode out to a point in heating time required to ensure heat propagation into the case (i.e., the $R_{\theta JX}$ condition), an appropriate heat sink should be used or the case temperature should be monitored.

Step 1: From a 20 to 25 piece sample, pick any one diode to start the setup process. Set up the test apparatus as follows:

I_H = 1.0 A	(Or some other desired value near the DUTs normal operating current: typically higher for power diodes, and lower for zener diodes, when measured in the zener direction.)
t_H = 10-50 ms	Unless otherwise specified, for most devices rated up to 15 W power dissipation.
50 - 100 ms	Unless otherwise specified, for most devices rated up to 200 W power dissipation.
≥ 250 ms	For steady state thermal resistance measurement. The pulse must be shown to correlate to steady state conditions before it can be substituted for steady state condition.
*t_{MD} = 100 µs max	A larger value may be required on power devices with inductive package elements which generate nonthermal electrical transients; unless otherwise specified, this would be observed in the t_3 region of figure 3101-2.
I_M = 10 mA	(Or some nominal value approximately two percent, or less, of I_H.)

Step 2: Insert device into the apparatus test fixture and initiate a test. (For best results, a test fixture that offers some form of heat sinking would be desirable. Heat sinking is not needed if either the power dissipation during the test is well within the diode's free-air rating or the maximum heating time is limited to less than that required for the heat to propagate through the case.)

*Step 3: If ΔV_F is in the 15 to 80 mV range, or ΔV_{ZL} is equivalent to the same ΔT_J, then proceed to the next step. This range approximately corresponds to a junction temperature change of roughly +10°C to +50°C and is sufficient for initial comparison purposes.

If ΔV_F is less than 15 mV, return to step 1 and increase heating power into device by increasing I_H.

If ΔV_F is greater than 80 mV, approximately corresponding to a junction temperature change greater than +50°C, it would probably be desirable to reduce the heating power by returning to step 1 and reducing I_H.

NOTE: The test equipment shall be capable of resolving ΔV_F to within five percent. If not, the higher value of ΔV_F must be selected until the five percent tolerance is met. Two different devices can have the same junction temperature rise even when P_H is different, due to widely differing V_H. Within a given lot, however, a higher V_H is more likely to result in a higher junction temperature rise. For such examples, this screen can be more accurately accomplished using the CU value. As defined in 2., CU provides a comparison unit that takes into account different device V_H values for a given I_H test condition.

*Step 4: Test each of the sample devices and record the data detailed in 8.1.

*Step 5: Select out the devices with the highest and lowest values of CU or $Z_{\underline{\theta JX}}$ and put the remaining devices aside.

The ΔV_F values can be used instead of CU or $Z_{\theta JX}$ if the measured values of V_H are very tightly grouped around the average value.

Step 6: Using the devices from step 5, collect and plot the heating curve data for the two devices in a manner similar to the examples shown on figure 3101-4.

*Step 7: Interpretation of the heating curves is the next step. Realizing that the thermal characteristics of identical chips should be the same if the heating time (t_H) is less than or equal to the thermal time constant of the chip, the two curves should start out the same for the low values of t_H. Non identical chips (thinner or smaller in cross section) will have completely different curves, even at the smaller values of t_H. As the value of t_H is increased, thereby exceeding the chip thermal constant, heat will have propagated through the chip into the die attachment region. Since the heating curve devices of step 5 were specifically chosen for their difference, the curves of figure 3101-4 diverge after t_H reaches a value where the die attachment variance has an affect on the device junction temperature. Increasing t_H further will probably result in a flattening of the curve as the heating propagates in the device package. If the device package has little thermal mass and is not well mounted to a good heat sink, the curve will not flatten very much, but will show a definite change in slope.

Step 8: Using the heating curve, select the appropriate value of t_H to correspond to the inflection point in the transition region between heat in the chip and heat in the package.

If there are several different elements in the heat flow path: Chip, die attachment, substrate, substrate attach, and package for example in a hybrid, there will be several plateaus and transitions in the heating curve. Appropriate selection of t_H will optimize evaluation sensitivity to other attachment areas.

Step 9: Return to the apparatus and set t_H equal to the value determined from step 8.

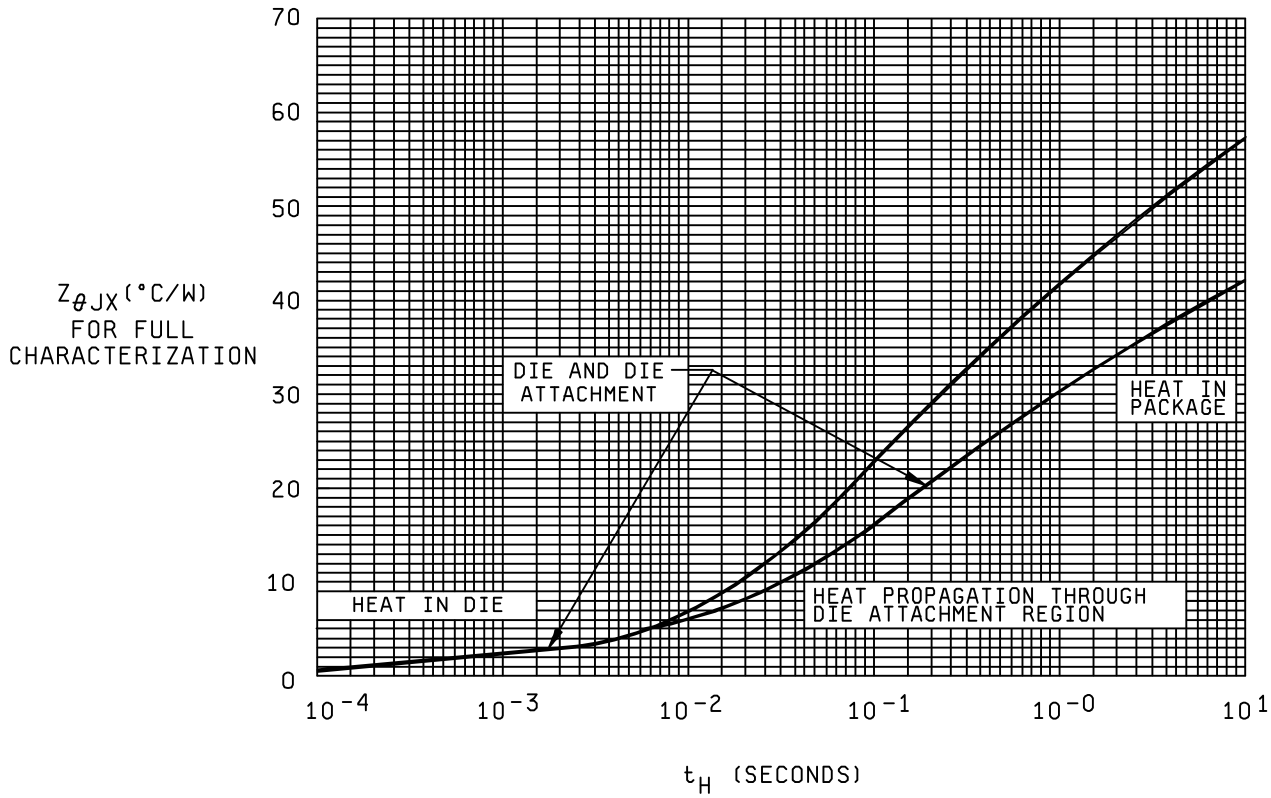


FIGURE 3101-4. Heating curves for two extreme devices.

Step 10: Because the selected value of t_H is much less than that for thermal equilibrium, it is possible to significantly increase the heating power without degrading or destroying the device. The increased power dissipation within the DUT will result in higher ΔV_F or CU values that will make determination of acceptable and nonacceptable devices much easier.

Step 11: The pass/fail limit, the cut-off point between acceptable and nonacceptable devices, can be established in a variety of ways:

a. Correlation to other die attachment evaluation methods, such as die shear and x-ray, while these two methods have little actual value from a thermal point of view, they do represent standardization methods as described in various military standards.

*b. Maximum allowable junction temperature variations between devices, since the relationship between ΔT_J and ΔV_F is about 0.5°C/mV for forward bias testing, or a measurable equivalent for zener direction testing, the junction temperature spread between devices can be easily determined. The T_J predicts reliability. Conversely, the T_J spread necessary to meet the reliability projections can be translated to a ΔV_F or CU value for pass/fail criteria.

To fully utilize this approach, it will be necessary to calibrate the devices for the exact value of the T_J to V_F characteristic. The characteristic's slope, commonly referred to as K factor, is easily measured on a sample basis using a voltmeter, environmental chamber, temperature indicator, and a power supply setup as described in 6. A simple set of equations yield the junction temperature once K and ΔV_F are known:

$$\Delta T_J = (K)\ (\Delta V_F)$$

$$T_J = T_A + \Delta T_J$$

Where T_A is the ambient or reference temperature. For thermal transient test conditions, this temperature is usually equivalent to lead temperature (T_L) for axial lead devices or case temperature (T_C) for case mounted devices.

*c. Statistically from a 20 to 25 device sample the distribution of ΔV_F or CU values should be a normal one with defective devices out of the normal range. Figure 3101-5 shows a ΔV_F distribution for a sample lot of diodes. NOTE: The left-hand side of the histogram envelope is fairly well defined but the other side is greatly skewed to the right. This comes about because the left-hand side is constrained by the absolutely best heat flow that can be obtained with a given chip assembly material and process unless a test method error is introduced. The other side has no such constraints because there is no limit as to how poorly a chip is mounted.

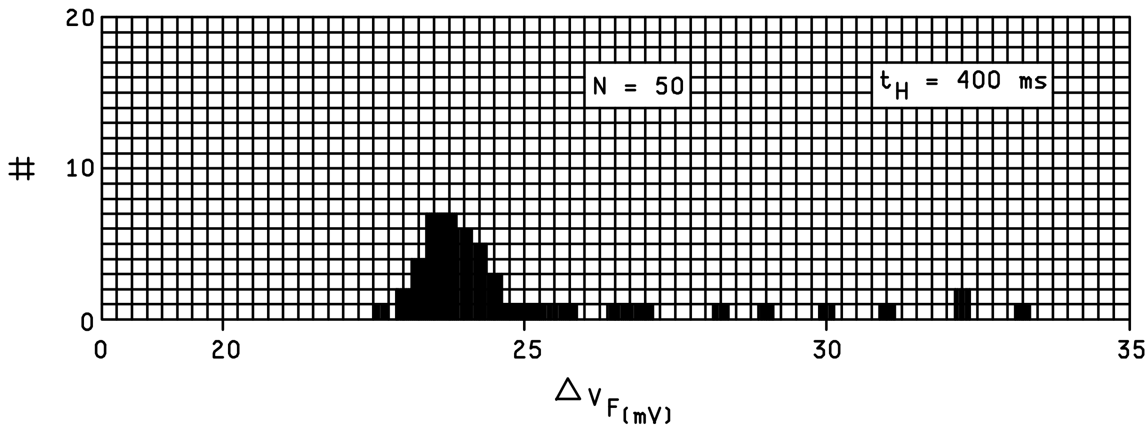


FIGURE 3101-5. Typical ΔV_F distribution.

The usual rule of thumb in setting the maximum limit for ΔV_F , CU, or $Z_{\theta JX}$ is to use the distribution average value and three standard deviations (σ). For example:

$| (\Delta V_F) | = \overline{\Delta V_F} + X\, \sigma$

high
limit

$| (CU) | = \overline{CU} + X\, \sigma$

high
limit

$| (Z_{\theta JX}) | = \overline{Z_{\theta JX}} + X\, \sigma$

high
limit

Where X = 3 in most cases and $\overline{\Delta V_F}$, $\overline{\Delta CU}$, and $\overline{\Delta Z_{\theta JX}}$ are the average distribution values.

The statistical data required is obtained by testing 25 or more devices under the conditions of step 11.

The maximum limit determined from this approach should be correlated to the diode's specified thermal resistance. This will ensure that the ΔV_F or CU limits do not pass diodes that would fail the thermal resistance or transient thermal impedance requirements.

*Step 12: Once the test conditions and pass/fail limit have been determined, it is necessary only to record this information for future testing requirements of the same device in the same package. It is also recommended that a minimum limit is established to ensure a test method error or other anomaly is investigated.

*Step 13: After the pass/fail limits are established, there shall be verification they correlate to good and bad bonded devices or the electrical properties such as surge.

The steps listed hereto are conveniently summarized in table 3101-I.

*TABLE 3101-I. Summary of test procedure steps.

General description		Steps	Comments
A	Initial setup	1 through 4	Approximate instrument settings to find variations among devices in 10 to 15 piece sample.
B	Heating curve generation	5 through 6	Using highest and lowest reading devices, generate heating curves.
C	Heating curve interpretation	7 through 9	Heating curve is used to find more appropriate value for t_H corresponding to heat in the die attachment area (for some other desired interface in the heat flow path).
D	Final setup	10	Heating power applied during t_H is increased in order to improve measurement sensitivity to variations among devices.
E	Pass-fail determination	11 through 12	A variety of methods is available such as JESD 34 for setting the fail limit; the statistical approach is the fastest and easiest to implement.
F	Verification	13	Mechanical / Electrical Correllation

7.2 Routine device thermal transient testing procedure. Once the proper control settings have been determined for a particular device type from a given manufacturing process or vendor, repeated testing of that device type simply requires that the same test conditions be used as previously determined.

New device types or the same devices manufactured with a different process will require a repeat of 7.1 for proper thermal transient test conditions.

8. Test conditions and measurements to be specified and recorded.

8.1 Thermal transient and equilibrium measurements.

8.1.1 Test conditions. Specify the following test conditions:

a. I_M measuring current ___ mA

b. I_H heating current ___ A

c. t_H heating time ___ ms

d. t_{MD} measurement time delay ___µs

e. t_{SW} sample window time __ µs

8.1.2 Data. Record the following data:

a. V_{Fi} initial forward voltage ___V

b. V_H heating voltage ___V

c. V_{Ff} final forward voltage ___V

(NOTE: Some test equipment may provide a ΔV_F instead of V_{Fi} and V_{Ff}; this is an acceptable alternative. Record the value of ΔV_F.

Some test equipment may provide direct display of calculated CU or $Z_{\theta JX}$ this is an acceptable alternative. Record the value of CU or $Z_{\theta JX}$.

8.2 K factor calibration. (Optional for criteria 8.3a or 8.3b, mandatory for 8.3c, 8.3d, or 8.3e.)

8.3 Test conditions. Specify the following test conditions:

a. I_M current magnitude ___mA

b. Initial junction temperature ___°C

c. Initial V_F voltage ___mV

d. Final junction temperature ___°C

e. Final V_F voltage ___mV

8.4 K factor. Calculate K factor in accordance with the following equation:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{F2} - V_{F1}} \right| \; °C/mV$$

K factor ___°C/mV

8.5 Specification limit calculations. One or more of the following should be measured or calculated, as called for on the device specification (see 5.1):

ΔV_F ___mV

CU ___mV/V

ΔT_J ___°C

K•CU ___°C/V

$Z_{\theta JX}$ ___°C/W

$R_{\theta JX}$ ___°C/W

METHOD 3103

THERMAL IMPEDANCE MEASUREMENTS FOR INSULATED GATE BIPOLAR TRANSISTORS

(DELTA GATE-EMITTER ON VOLTAGE METHOD)

1. Purpose. The purpose of this test method is to measure the thermal impedance of the IGBT under the specified conditions of applied voltage, current, and pulse duration. The temperature sensitivity of the gate-emitter ON voltage, under conditions of applied collector-emitter voltage and low emitter current, is used as the junction temperature indicator. This method is particularly suitable to enhancement mode, power IGBTs having relatively long thermal response times. This test method is used to measure the thermal response of the junction to a heating pulse. Specifically, the test may be used to measure dc thermal resistance and to ensure proper die mountdown to its case. This is accomplished through the appropriate choice of pulse duration and heat power magnitude. The appropriate test conditions and limits are detailed in 6.

2. Definitions. The following symbols and terms shall apply for the purpose of this test method:

a. I_M: Emitter current applied during measurement of the gate-emitter ON voltage.

b. I_H: Heating current through the collector or emitter lead.

c. V_H: Heating voltage between the collector and emitter.

d. P_H Magnitude of the heating power pulse applied to DUT in watts; the product of I_H and V_H.

e. t_H: Heating time during which P_H is applied.

f. VTC: Voltage-temperature coefficient of $V_{GE(ON)}$ with respect to T_J; in mV/°C.

g. K: Thermal calibration factor equal to reciprocal of VTC; in °C/mV.

h. T_J: Junction temperature in degrees Celsius.

T_{Ji}: Junction temperature in degrees Celsius before start of the power pulse.

T_{Jf}: Junction temperature in degrees Celsius at the end of the power pulse.

i. T_X: Reference temperature in degrees Celsius.

T_{Xi}: Initial reference temperature in degrees Celsius.

T_{Xf}: Final reference temperature in degrees Celsius.

j. $V_{GE(ON)}$: Gate-emitter ON voltage in millivolts.

$V_{GE(ON)i}$: Initial gate-emitter ON voltage in millivolts.

$V_{GE(ON)f}$: Final gate-emitter ON in millivolts.

k. $V_{GE(M)}$: Gate-emitter voltage during measurement periods.

$V_{GE(H)}$: Gate-emitter voltage during heating periods.

l. $V_{CE(M)}$: Collector-emitter voltage during measurement periods.

$V_{CE(H)}$: Collector-emitter voltage during heating periods.

m. V_{CG}: Collector-gate voltage, adjusted to provide appropriate V_{CE}.

n. t_{MD}: Measurement delay time is defined as the time from the removal of heating power P_H to the start of the $V_{GE(ON)}$ measurement.

o. t_{SW}: Sample window time during which final $V_{GE(ON)}$ measurement is made.

p. $Z_{\Theta JX}$: Transient junction-to-reference point thermal impedance in °C/W. $Z_{\Theta JX}$ or specified power pulse duration is:

$$Z_{\theta JX} = \left(T_{jf} - T_{ji} - \frac{\Delta T_x}{P_H} \right)$$

Where: ΔT_X = change in reference point temperature during the heating pulse (see 5.2 and 5.4 for short heating pulses, e.g., die attach evaluation, this term is normally negligible.)

3. Apparatus. The apparatus required for this test shall include the following as applicable to the specified test procedure.

3.1 Case temperature measurement. A thermocouple for measuring the case temperature at a specified reference point. The recommended reference point shall be located on the case under the heat source. Thermocouple material shall be copper- constantan (type T) or equivalent. The wire size shall be no larger than AWG size 30. The junction of the thermocouple shall be welded, rather than soldered or twisted, to form a bead. The accuracy of the thermocouple and its associated measuring system shall be ±0.5°C. Proper mounting of the thermocouple to ensure intimate contact to the reference point is critical for system accuracy.

3.2 Controlled temperature environment. A controlled temperature environment capable of maintaining the case temperature during the device calibration procedure to within ±1°C over the temperature range of +23°C to +100°C, the recommended temperatures for measuring K-factor.

3.3 K factor calibration. A K factor calibration setup, as shown on figure 3103-1, that measures $V_{GE(ON)}$ for the specified values of V_{CE} and I_M in an environment where temperature is both controlled and measured. A temperature controlled circulating fluid bath is recommended. The current source must be capable of supplying I_M with an accuracy of ±2 percent. The voltage source V_{CG} is adjusted to supply V_{CE} with an accuracy of ±2 percent. The voltage measurement of $V_{GE(ON)}$ shall be made with a voltmeter capable of 1 mV resolution. The device-to-current source wire size shall be sufficient to handle the measurement current (AWG size 22 stranded is typically used for up to 100 mA).

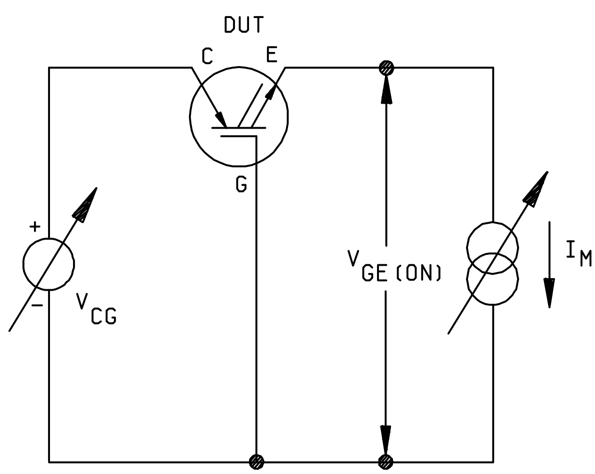


FIGURE 3103-1. K factor calibration setup.

3.4 Thermal testing. There are two approaches to the actual thermal testing, either the common-gate or the common-source method. Both methods work equally well, although the common-source method may be more reliable and less potentially damaging to the DUT. The figures and description below describe the thermal measurement for n-channel enhancement mode devices. Opposite polarity devices can be tested by appropriately reversing the various supplies. Depletion mode devices can be tested by applying the gate-emitter voltage (V_{GE}) in the appropriate manner.

3.4.1 Common-gate thermal test circuit. A common-gate configuration test circuit used to control the device and to measure the temperature using the gate-emitter ON voltage as the temperature sensing parameter as shown on figure 3103-2. Polarities shown are for n-channel devices but the circuit may be used for p-channel types by reversing the polarities of the voltage and current sources.

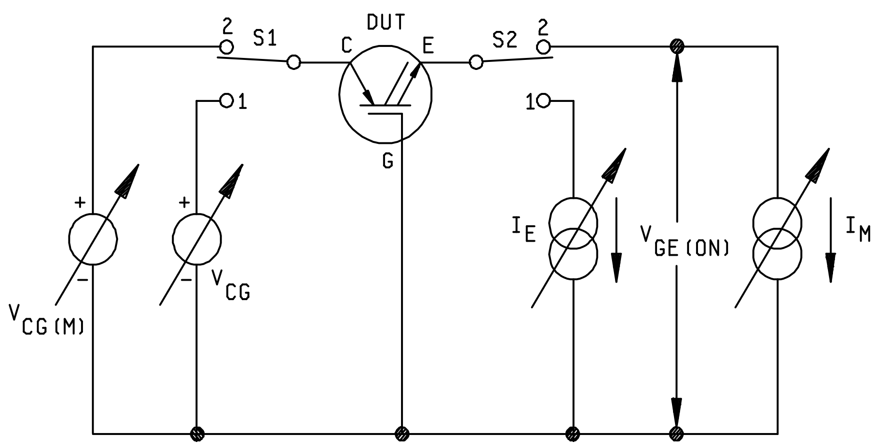
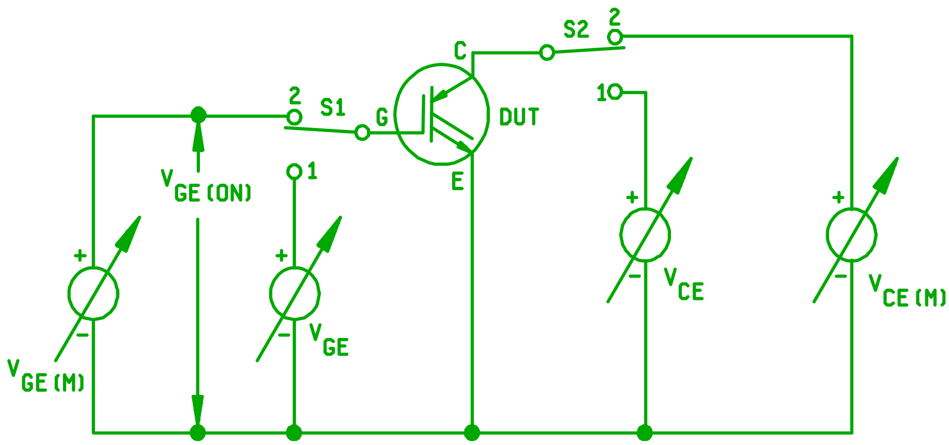


FIGURE 3103-2. Common-gate thermal impedance measurement circuit (gate-emitter on voltage method).

The circuit consists of the DUT, two voltage sources, two current sources, and two electronic switches. During the heating phase of the measurement, switches S1 and S2 are in position 1. The values of V_{CG} and I_E are adjusted to achieve the desired values of I_C and V_{CE} for the P_H "heating" condition.

To measure the initial and post heating pulse junction temperatures of the DUT, switches S1 and S2 are each switched to position 2. This puts the gate at the measurement voltage level $V_{CG(M)}$ and connects the current source I_M to supply measurement current to the emitter. The values of $V_{CG(M)}$ and I_M must be the same as used in the K factor calibration if actual junction temperature rise data is required. Figures 3103-4 and 3103-5 show the waveforms associated with the three segments of the test.

3.4.2 Common-source thermal test circuit. A common-source configuration test circuit used to control the device and to measure the temperature using the gate-emitter ON voltage as the temperature sensing parameter as shown on figure 3103-3. Polarities shown are for n-channel devices but the circuit may be used for p-channel types by reversing the polarities of the voltage and current sources.



NOTE: The circuit consists of the DUT, four voltage sources, and two electronic switches. During the heating phase of the measurement, switches S1 and S2 are in position 1. The values of V_{CE} and V_{GE} are adjusted to achieve the desired values of I_C and V_{CE} for the P_H "heating" condition.

FIGURE 3103-3. Common-source thermal impedance measurement circuit (gate-emitter on voltage method).

To measure the initial and post heating pulse junction temperatures of the DUT, switches S1 and S2 are each switched to position 2. This puts the collector at the measurement voltage level $V_{CE(M)}$ and the gate at $V_{GE(M)}$, which must be adjusted to obtain I_M. The values of $V_{CE(M)}$ and I_M must be the same as used in the K factor calibration if actual junction temperature rise data is required. Figures 3103-4 and 3103-5 show the waveforms associated with the three segments of the test.

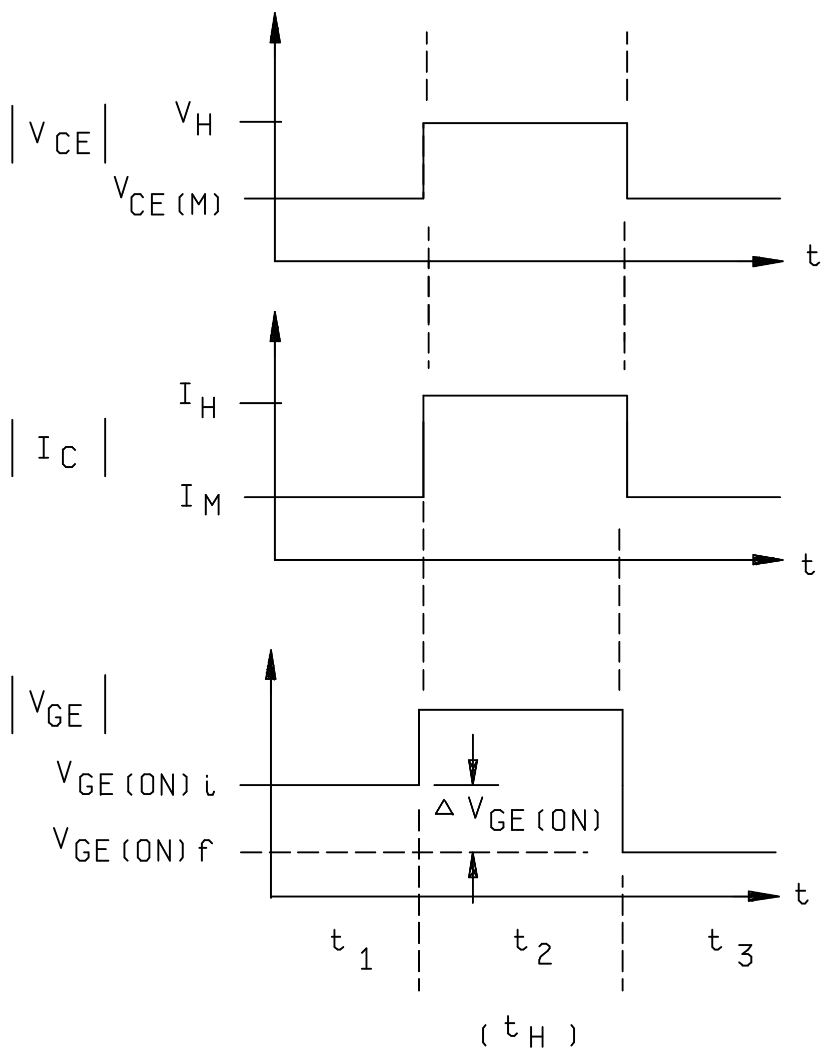


FIGURE 3103-4. Device waveforms during the three segments of the thermal transient test.

The value of t_{MD} is critical to the accuracy of the measurement and must be properly specified in order to ensure measurement repeatability. Note that some test equipment manufacturers include the sample and hold window time t_{SW} within their t_{MD} specification.

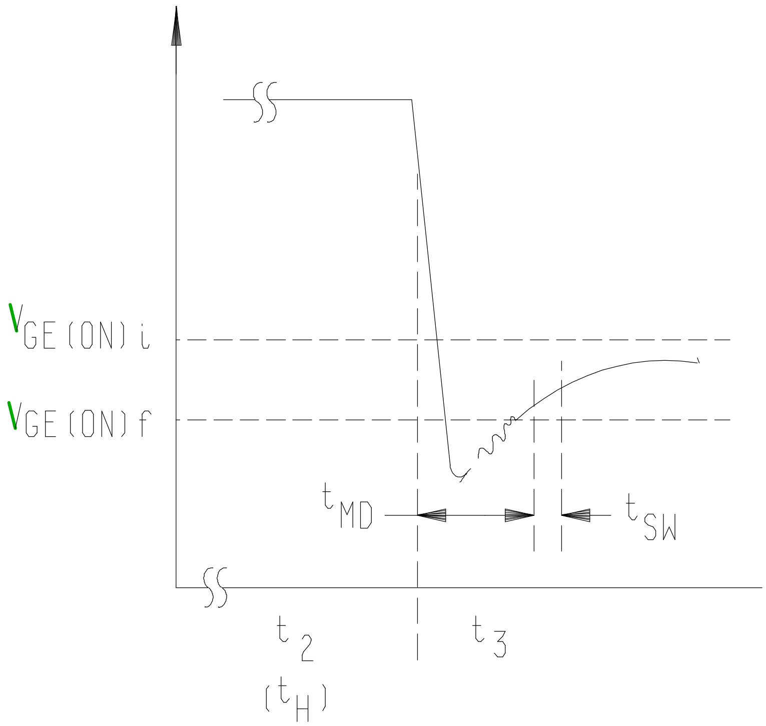


FIGURE 3103-5. Second V_{GE} measurement waveform.

NOTE: The circuits for both common-gate and common-source thermal measurements can be modified so that V_{CE} is applied during both measurement and heating periods if the value of V_{CE} is at least ten times the value of $V_{GE(ON)}$. Further, the common-gate circuit can be modified so that I_M is continually applied as long as the I_E current source can be adjusted for the desired value of heating current.

3.5 Source-drain forward voltage. Suitable sample-and-hold voltmeter or oscilloscope to measure source-drain forward voltage at specified times. $V_{GE(ON)}$ shall be measured to within 5 mV, or within 5 percent of ($V_{GE(ON)i}$ - $V_{GE(ON)f}$), whichever is less.

4. Measurement of the TSP. The required calibration of $V_{GE(ON)}$ versus T_J is accomplished by monitoring $V_{GE(ON)}$ for the required values of V_{CE} and I_M as the heat sink temperature (and thus the DUT temperature) is varied by external heating. The magnitudes of V_{CE} and I_M shall be chosen so that $V_{GE(ON)}$ is a linearly decreasing function over the expected range of T_J during the power pulse. For this condition, V_{CE} must be at least three times $V_{GE(ON)}$. I_M must be large enough to ensure that the device is turned on but not so large as to cause any significant self-heating. (This will normally be 1 mA for low power devices and up to 100 mA for high power ones.) An example calibration curve is shown on figure 3103-6.

4.1 K factor calibration. A calibration factor K (which is the reciprocal of VTC or the slope of the curve on figure 3103-4) can be defined as:

$$K = \frac{1}{VTC} = \left| \frac{T_J1 - T_J2}{V_{GE(ON)1} - V_{GE(ON)2}} \right| \ {}^{\circ}C / mV$$

It has been found experimentally that the K-factor variation for all devices within a given device type class is small. The usual procedure is to perform a K factor calibration on a 10 to 12 piece sample from a device lot and determine the average K and standard deviation (σK). If σK is less than or equal to three percent of the average value of K, then the average value of K can be used for all devices within the lot. If σK is greater than three percent of the average value of K, then all the devices in the lot shall be calibrated and the individual values of K shall be used in thermal impedance calculations or in correcting $\Delta V_{GE(ON)}$ values for comparison purposes.

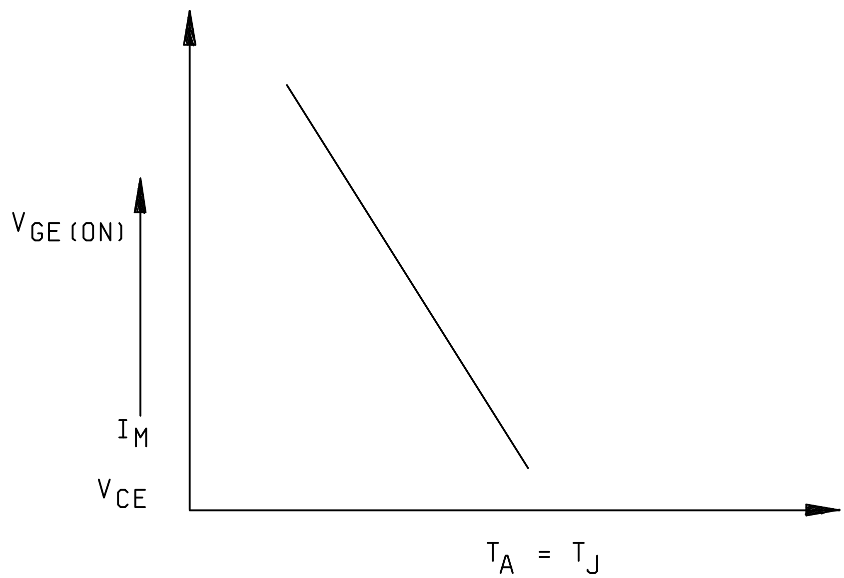


FIGURE 3103-6. Example curve of $V_{GE(ON)}$ versus T_J.

When screening to ensure proper die attachment within a given lot, this calibration step is not required, (e.g., devices of a single manufacturer with identical PIN and case style). In such cases, the measure of thermal response may be $\Delta V_{GE(ON)}$ for a short heating pulse, and the computation of ΔT_J or $Z_{\Theta JX}$ is not necessary. (For this purpose, t_H shall be 10 ms for TO-39 size packages and 100 ms for TO-3 packages.)

5. Calibration. K factor must be determined according to the procedure outlined in 4, except as noted in 4.1.

5.1 Reference point temperature. The reference point is usually chosen to be on the bottom of the transistor case directly below the semiconductor chip in a TO-204 metal can or in close proximity to the chip in other styles of packages. Reference temperature point location must be specified and its temperature shall be monitored using the thermocouple mentioned in 3.1 during the preliminary testing. If it is ascertained that T_X increases by more than five percent of measured junction temperature rise during the power pulse, then either the heating power pulse magnitude must be decreased, the DUT must be mounted in a temperature controlled heat sink, or the calculated value of thermal impedance must be corrected to take into account the thermal impedance of the reference point to the cooling medium or heat sink.

Temperature measurements for monitoring, controlling or correcting reference point temperature changes are not required if the t_H value is low enough to ensure that the heat generated within the DUT has not had time to propagate through the package. Typical values of t_H for this case are in the 10 ms to 500 ms range, depending on DUT package type and material.

5.2 Thermal measurements. The following sequence of tests and measurements must be made.

a. Prior to the power pulse:

(1) Establish reference point temperature T_{Xi}.

(2) Apply measurement voltage V_{CE}.

(3) Apply measurement current I_M.

(4) Measure gate-emitter ON voltage $V_{GE(ON)i}$ (a measurement of the initial junction temperature).

b. Heating pulse parameters:

(1) Apply collector-emitter heating voltage V_H.

(2) Apply collector heating current I_H as required by adjustment of gate-emitter voltage.

(3) Allow heating condition to exist for the required heating pulse duration t_H.

(4) Measure reference point temperature T_{Xf} at the end of heating pulse duration.

NOTE: T_X measurements are not required if the t_H value meets the requirements stated in 5.2.

c. Post power pulse measurements:

(1) Apply measurement current I_M.

(2) Apply measurement voltage V_{GE}.

(3) Measure gate-emitter ON voltage $V_{GE(ON)f}$ (a measurement of the final junction temperature).

(4) Time delay between the end of the power pulse and the completion of the $V_{GE(ON)f}$ measurement as defined by the waveform of figure 3103-4 in terms of t_{MD} plus t_{SW}.

d. The value of thermal impedance, $Z_{\Theta JX}$, is calculated from the following formula:

$$Z_{\theta JX} = \frac{\Delta T_J}{P_H} = \left| \frac{K (V_{GE(ON)f} - V_{GE(ON)i})}{(I_H)(V_H)} \right| \circ C / W$$

This value of thermal impedance will have to be corrected if T_{Xf} is greater than T_{Xi} by +5°C. The correction consists of subtracting the component of thermal impedance due to the thermal impedance from the reference point (typically the device case) to the cooling medium or heat sink. T_X measurements are not required if the t_H value meets the requirements stated in 5.2.

This thermal impedance component has a value calculated as follows:

$$Z_{\theta X-HS} = \frac{\Delta T_X}{P_H} = \frac{(T_{Xf} - T_{Xi})}{(I_H)(V_H)}$$

Where: HS = cooling medium or heat sink (if used).
Then:

$$\underbrace{Z_{\Theta JX}}_{\text{Corrected}} = \underbrace{Z_{\Theta JX}}_{\text{Calculated}} - Z_{\Theta X\text{-}HS}$$

NOTE: This last step is not necessary for die attach evaluation (see 4.1).

6. Test conditions and measurements to be specified and recorded.

6.1 K factor calibration.

6.1.1 Test conditions. Specify the following test conditions:

a. I_M current magnitude ___mA
(See detail specification for current value)

b. V_{CE} voltage magnitude ___V
(See detail specification for voltage value)

c. Initial junction temperature ___°C
(Normally +25°C ±5°C)

d. Final junction temperature ___°C
(Normally +100°C ±10°C)

6.1.2 Data. Record the following data:

a. Initial $V_{GE(ON)}$ voltage ___mV

b. Final $V_{GE(ON)}$ voltage ___mV

6.1.3 K factor. Calculate K factor in accordance with the following equation:

$$K = \left| \frac{T_J 1 - T_J 2}{V_{GE(ON)1} - V_{GE(ON)2}} \right| \; ^{\circ}C / mV$$

6.1.4 For die attachment evaluation, this step may not be necessary (see 4.1).

6.2 Thermal impedance measurements.

6.2.1 Test conditions. Specify the following test conditions:

a. I_M measuring current ___mA
(Must be same as used for K factor calibration)

b. V_{CE} measuring voltage ___V
(Must be same as used for K factor calibration)

c. I_H heating current ___A

d. V_H collector-emitter heating voltage ___V

e. t_H heating time ___s

f. t_{MD} measurement time delay ___μs

g. t_{SW} sample window time ___μs

(NOTE: I_H and V_H are usually chosen so that P_H is approximately two-thirds of device rated power dissipation.)

6.2.2 Data. Record the following data:

a. T_{Xi} initial reference temperature ___°C

b. T_{Xf} final reference temperature ___°C

6.2.2.1 $\Delta V_{GE(ON)}$ data:

$\Delta V_{GE(ON)}$ ___mV

6.2.2.2 $V_{GE(ON)}$ data:

a. $V_{GE(ON)i}$ initial source-drain voltage ___V

b. $V_{GE(ON)f}$ final source-drain voltage ___V

T_X measurements are not required if the t_H value meets the requirements stated in 5.2.

6.2.3 Thermal impedance. Calculate thermal impedance using the procedure and equations shown in 5.4.

6.3 $\Delta V_{GE(ON)}$ measurements for screening. These measurements are made for t_H values that meet the intent of 4.1 and the requirements stated in 5.2.

6.3.1 Test conditions. Specify the following test conditions:

a. I_M measuring current ___mA

b. V_{GE} measuring voltage ___V

c. I_H heating current ___A

d. V_H collector-emitter heating voltage ___V

e. t_H heating time ___s

f. t_{MD} measurement time delay ___μs

g. t_{SW} sample window time ___μs

(The values of I_H and V_H are usually chosen equal to or greater than the values used for thermal impedance measurements.)

6.3.2 Specified limits. The following data is compared to the specified limits:

6.3.2.1 $\Delta V_{GE(ON)}$ data:

$\Delta V_{GE(ON)}$ __mV

6.3.2.2 $V_{GE(ON)}$ data:

a. $V_{GE(ON)i}$ initial source-drain voltage ___V

b. $V_{GE(ON)f}$ final source-drain voltage ___V

Compute $\Delta V_{GE(ON)}$ ___mV

6.3.2.3 ΔT_J calculation. Optionally calculate ΔT_J if the K factor results produce a σ greater than three percent of the average value of K.

$$\Delta T_J = K(\Delta V_{GE(ON)})\ ^\circ C$$

METHOD 3104

THERMAL RESISTANCE MEASUREMENTS OF GaAs MOSFET's (CONSTANT CURRENT FORWARD-BIASED GATE VOLTAGE METHOD)

1. Purpose. The purpose of this test method is to measure the thermal resistance of the MESFET under the specified conditions of applied voltage, current, and pulse width. The temperature sensitivity of the forward voltage drop of the gate-source diode is used as the junction temperature indicator. This method is particularly suitable for completely packaged devices.

2. Definitions. The following symbols and terms shall apply for the purpose of this test method:

a. I_M: Measuring current in the gate-source diode.

b. I_H: Heating current through the drain.

c. V_H: Heating voltage between the drain and source.

d. P_H Magnitude of the heating power pulse applied to DUT in watts; the product of I_H and V_H.

e. t_H: Heating time during which P_H is applied.

f. K: Thermal calibration factor (°C/mV).

g. T_J: Junction temperature in degrees Celsius.

T_{Ji}: Junction temperature in degrees Celsius before start of the power pulse.

T_{Jf}: Junction temperature in degrees Celsius at the end of the power pulse.

h. T_X: Reference temperature in degrees Celsius.

T_{Xi}: Initial reference temperature in degrees Celsius.

T_{Xf}: Final reference temperature in degrees Celsius.

i. V_{GSf}: Forward-biased gate-source junction diode voltage drop in volts.

$V_{GSf(i)}$: Initial gate-source voltage.

$V_{GSf(f)}$: Final gate-source voltage.

j. t_{MD}: The time from the start of heating power (P_H) removal to the completion of the final V_{GSf} measurement.

k. Θ_{JX} Junction-to-reference point thermal resistance in degrees Celsius/watt. Θ_{JX} for specified heating power conditions is:

$$\theta_{JX} = \frac{(T_{Jf} - T_{Ji})}{P_H}$$

l. CU: Comparison unit for screening devices against specification limits. Defined as the change in forward biased gate-source voltage divided by heating current in mV/A.

3. Apparatus. The apparatus required for this test shall include the following as applicable to the specified test procedure.

3.1 Case reference point temperature. The case reference point temperature shall be measured using a thermocouple. The recommended reference point should be located immediately outside the case under the heat source. Thermocouple material shall be copper-constantan (type T) or equivalent. The wire size shall be no larger than AWG size 30. The junction of the thermocouple shall be welded to form a bead rather than soldered or twisted. The accuracy of the thermocouple and associated measuring system shall be ±0.5°C.

3.2 Controlled temperature environment. A controlled temperature environment capable of maintaining the case temperature during the device calibration procedure to within ±1°C over the temperature range of room temperature (approximately +23°C) to +100°C.

3.3 K factor calibration setup. A K factor calibration setup, as shown on figure 3104-1, that measures V_{GSf} for a specified value of I_M in an environment that is both temperature controlled and measured. The current source must be capable of supplying I_M with an accuracy of ±1 percent and have a compliance of at least 1 volt and not more than 2 volts. The voltage measurement of V_{GSf} should be made to 1 mV resolution. The device-to-current source wire size shall be sufficient to handle the measurement current (AWG size 26 stranded is typically used for up to 10 mA).

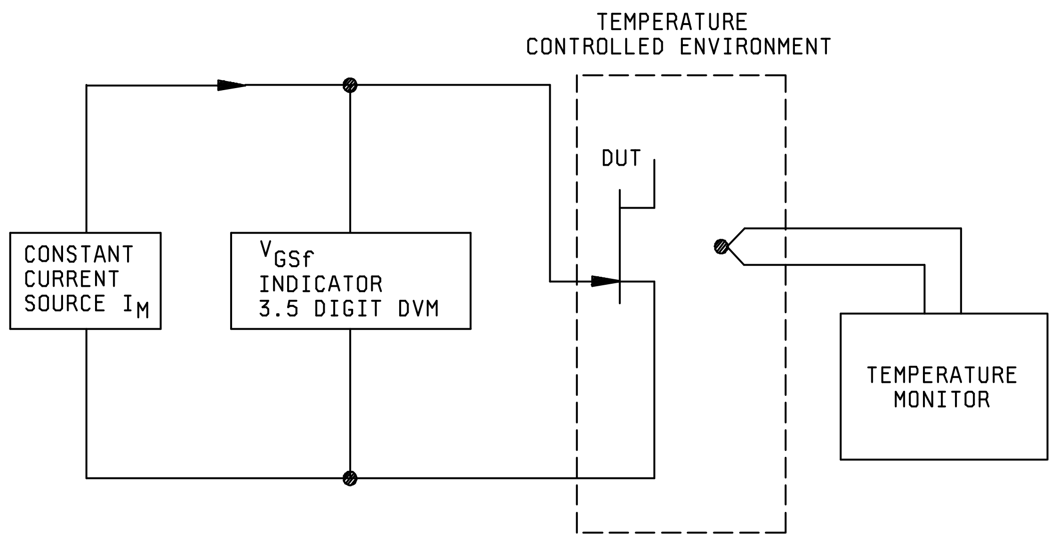
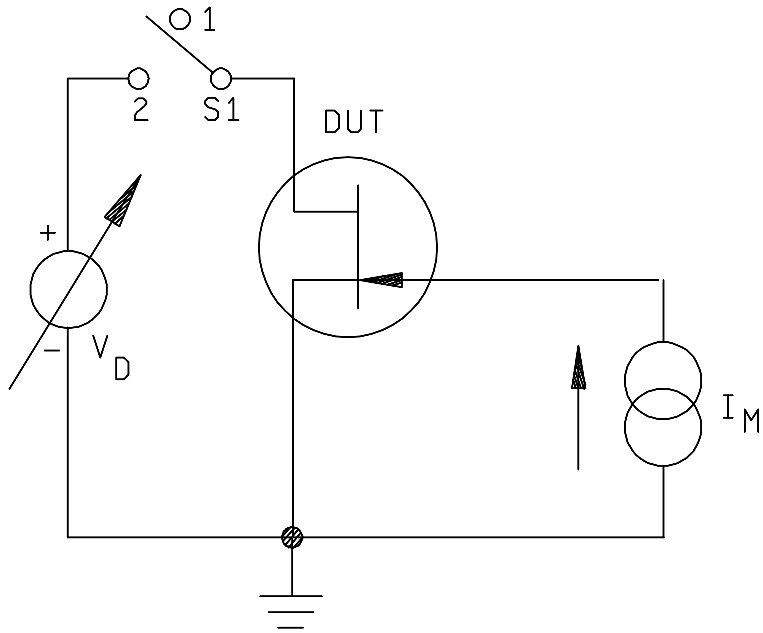


FIGURE 3104-1. K factor calibration setup.

3.4 Controlled temperature heat sink. Controlled temperature heat sink capable of maintaining the specified reference point temperature to within ±5 of the preset (measured) value.

3.5 Test circuit. The circuit used to control the device and to measure the temperature using the forward voltage of the gate-source diode as the temperature sensing parameter is shown on figure 3104-2. Polarities shown are for n-channel devices but the circuit may be used for p-channel types by reversing the polarities of the voltage and current sources.



NOTE: The circuit consists of the DUT, one voltage source, one current source, and one electronic switch. During the heating phase of the measurement, switch S1 is in position 2. The value of V_D is adjusted to achieve the desired values of I_D and V_{DS} for the P_H "heating" condition.

FIGURE 3104-2. Thermal resistance measurement circuit (constant current forward-biased gate voltage method).

To measure the initial and post heating pulse junction temperature of the DUT, switch S1 is switched to position 1. This disconnects the V_D source during the measurement time and allows for the measurement of $V_{GSf(i)}$ and $V_{GSf(f)}$ before and after the heating time, respectively. Figure 3104-3 shows the waveforms associated with the three segments of the test.

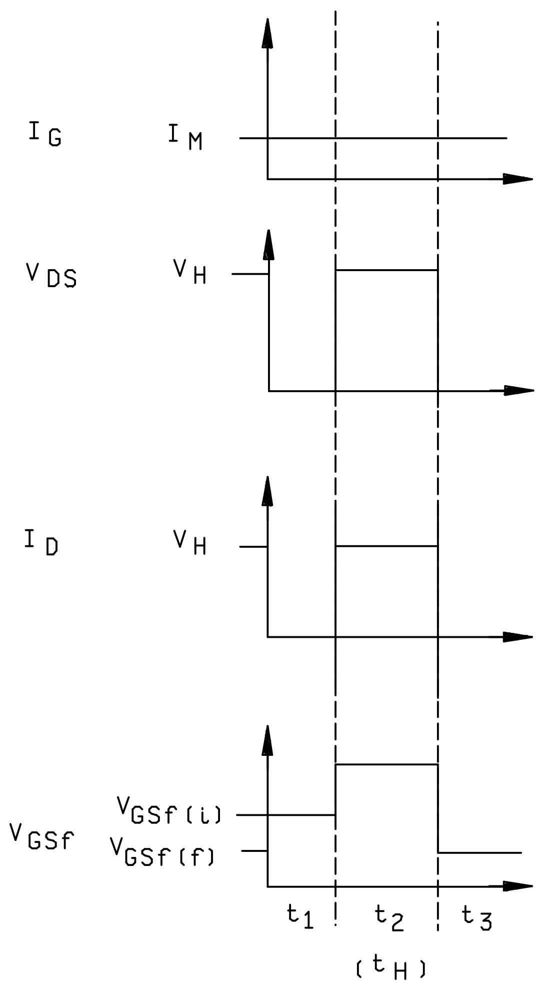


FIGURE 3104-3. Device waveforms during the three segments of the thermal resistance test.

The time required to make the second V_{GSf} reading is critical to the accuracy of the measurement and must be properly specified in order to ensure measurement repeatability. The definition of measurement delay time (t_{MD}) are described by the waveform on figure 3104-4.

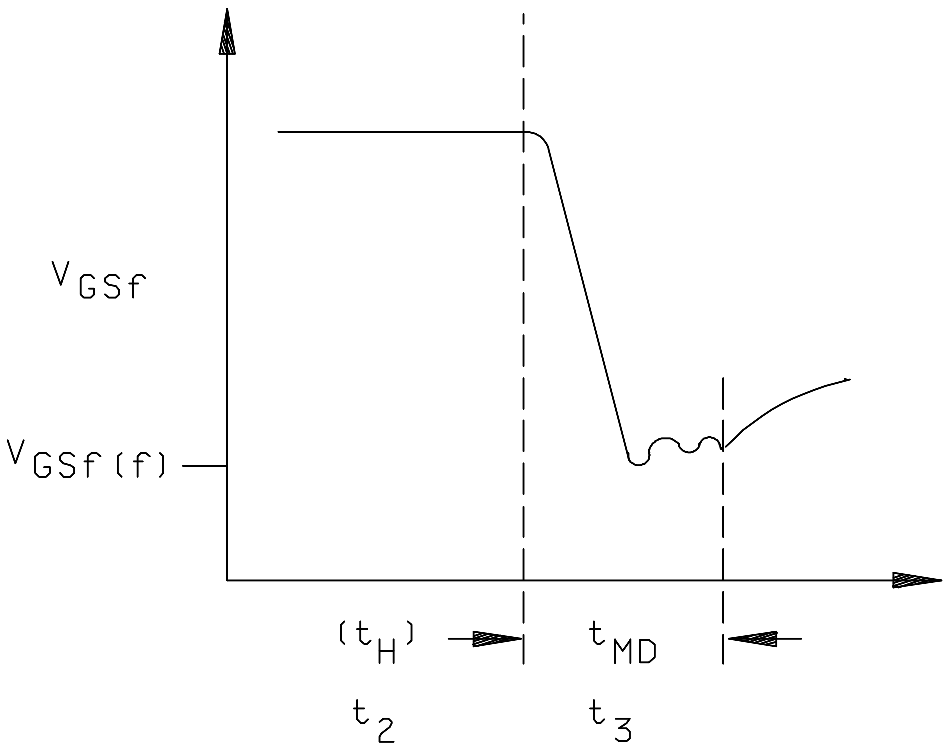


FIGURE 3104-4. Second V_{GSf} measurement waveform.

3.6 Source-drain forward voltage. Suitable sample-and-hold voltmeter or oscilloscope to measure source-drain forward voltage at specified times. V_{GSf} should be measured with 1 mV resolutions.

4. Measurement of the TSP V_{GSf}. The required calibration of V_{GSf} versus T_J is accomplished by monitoring V_{GSf} for the required value of I_M without any connection to the drain as the heat sink temperature (and thus the DUT temperature) is varied by external heating. The magnitude of I_M should be chosen so that V_{GSf} is a linearly decreasing function over the expected T_J range during the power pulse. I_M must be large enough to ensure that the gate-source junction is turned on but not large enough to cause significant self-heating or device destruction. An example calibration curve is shown on figure 3104-5.

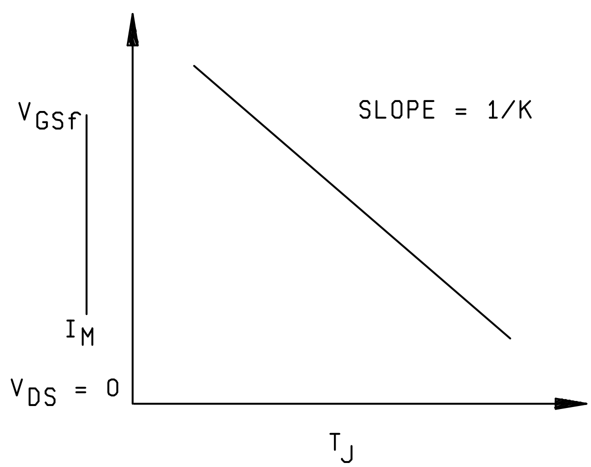


FIGURE 3104-5. Calibration curve.

A calibration factor K (which is the reciprocal of the slope of the curve on figure 3104-5) can be defined as:

$$K = \left| \frac{T_J 1 - T_J 2}{V_{GSf} 1 - V_{GSf} 2} \right| \ {}^\circ C / mV$$

It has been found experimentally that the K factor should vary less than several percent for all devices within a given device type class. The usual procedure is to perform a K factor calibration on a 10 to 12 piece sample from a device lot and determine the average K and standard deviation (σ). If σ is less than or equal to three percent of the average value of K, then the average value of K can be used for all devices within the lot. If σ is greater than the average value of K, then all the devices in the lot should be calibrated and the individual values of K should be used in thermal resistance calculations.

5. Test procedure.

5.1 Calibration. K factor must be determined according to the procedure outlined in 4.

5.2 Reference point temperature. The reference point is usually chosen to be on the bottom of the transistor case directly below the semiconductor chip. Reference temperature point location must be specified and its temperature should be monitored using the thermocouple mentioned in 3.1 during the preliminary testing. If it is ascertained that T_{Xf} increases by more than +5°C during the power pulse, then either the heating power pulse magnitude must be decreased, the DUT must be mounted in a temperature controlled heat sink, or the calculated value of thermal resistance must be corrected to take into account the thermal resistance associated with the temperature rise of the reference point.

5.3 Thermal measurements. The following sequence of tests and measurements must be made:

a. Prior to the power pulse:

(1) Establish reference point temperature: T_{Xi}.

(2) Apply measurement current: I_M.

(3) Measure gate-source voltage drop: $V_{GSf(i)}$ (A measurement of the initial junction temperature).

b. Heating pulse parameters:

(1) Maintain measurement current: I_M.

(2) Apply drain-source heating voltage: V_H.

(3) Measure drain heating current: I_H.

(4) Allow heating condition to exist for the required heating pulse width: t_H.

(5) Measure reference point temperature: T_{Xf}, at the end of heating pulse width.

c. Post power pulse measurements:

(1) Maintain measurement current: I_M.

(2) Measure gate-source voltage drop: V_{GSf}(f) (A measurement of the final junction temperature).

(3) Determine time delay between the end of the power pulse and the completion of the $V_{GSf(f)}$ measurement as defined by the waveform of figure 3104-4.

5.4 Thermal resistance. The value of thermal resistance, θ_{JX}, is calculated from the following formula:

$$\theta_{JX} = \frac{\Delta T_J}{P_H} = \frac{K \left| V_{GSF(f)} - V_{GSf(i)} \right|}{(I_H)(V_H)}$$

This value of thermal resistance will have to be corrected if T_{Xf} is greater than TX_i. The correction consists of subtracting out the component of thermal resistance due to the heat flow path from the reference point (typically the device case) to the heat sink and the environment. This thermal resistance component has a value calculated as follows:

$$\theta_{X-HS} = \frac{\Delta T_X}{P_H} = \frac{(T_{Xf} - T_{Xi})}{(I_H)(V_H)}$$

Then:

$$\underbrace{\theta_{JX}}_{\text{Corrected}} = \underbrace{\theta_{JX}}_{\text{Calculated}} - \theta_{X\text{-}HS}$$

An additional correction may be required because of the fast cooling of a typical MESFET heat source area. This requires that the thermal resistance measurements be made for two different values of t_{MD}. Care must be taken to ensure that the shorter of the chosen t_{MD} values does not lie within the non-thermal (i.e, electrical) switching transient region. Similarly, if the longer t_{MD} value is too large, the resultant value of θ_{JX} will be too small for an accurate measurement due to device cooling. The correction for the calculated thermal resistance is given below for test conditions in which I_M, V_H, and t_H remain the same for both tests.

$$\theta_{JX} = \theta_{JX} = \theta_{JX} \mid = \left| \frac{\theta_{JX}2 - \theta_{JX}1}{t_{MD1}^{1/2} - t_{MD2}^{1/2}} \right|$$

calculated value

6. Test conditions and measurements to be specified and recorded.

6.1 K factor calibration.

a. Specify the following test conditions:

(1) I_M current magnitude ___mA
(See detail specification for current value.)

(2) Initial junction temperature ___°C
(Normally +25°C ±5°C.)

(3) Final junction temperature ___°C
(Normally +100°C ±10°C.)

b. Record the following data:

(1) Initial $V_{GSf(i)}$ voltage ___mV

(2) Final $V_{GSf(f)}$ voltage ___mV

c. Calculate K factor in accordance with the following equation:

$$K = \left| \frac{T_{J1} - T_{J2}}{V_{GSf1} - V_{GSf2}} \right| \,°C/mV$$

d. For die attachment evaluation, this step may not be necessary (see 4.1).

6.2 Thermal impedance measurements.

6.2.1 Test conditions. Specify the following test conditions:

a. I_M measuring current ___mA
(Must be same as used for K factor calibration)

b. V_H drain-source heating voltage ___V

c. t_H heating time ___s

d. t_{MD} measurement time delay ___µs

e. t_{SW} sample window time ___µs

(The value of V_H is usually chosen to produce an I_H value that results in a P_H approximately two-thirds of the device rated power dissipation.)

6.2.2 Record data. Record the following data:

a. T_{Xi} initial reference temperature ___°C

b. T_{Xf} final reference temperature ___°C

c. I_H current during heating time ___A

6.2.2.1 ΔV_{GSf} data:

ΔV_{GSf} ___mV

6.2.2.2 V_{GSf} data:

a. $V_{GSf(i)}$ initial gate-source voltage ___V

b. $V_{GSf(f)}$ final gate-source voltage ___V

6.2.2.3 θ_{JX} data:

θ_{JX} __°C/W

T_X measurements are not required if the t_H value meets the requirements stated in 5.2.

6.2.3 Thermal impedance calculations. Using the data collected in 6.2.2 and the procedure and equations shown in 5.4, calculate the thermal resistance.

6.3 ΔV_{GSF} measurements for screening. These measurements are made for t_H values that meet the intent of 4.1 and the requirements stated in 5.2.

6.3.1 Test conditions. Specify the following test conditions:

a. I_M measuring current __mA

b. V_H drain-source heating voltage __V

c. t_H heating time __s

d. t_{MD} measurement time delay __μs

e. t_{SW} sample window time __μs

(The value of V_H is usually chosen to produce an I_H value that results in a P_H equal to or greater than the values used for thermal impedance measurements.)

6.3.2 Specified limits. Data from one or more of the following is compared to the specified limits:

6.3.2.1 ΔV_{GSf} data:

ΔV_{GSf} __mV

6.3.2.2 V_{GSf} data:

a. $V_{GSf(i)}$ initial gate-source voltage __V

b. $V_{GSf(f)}$ final gate-source voltage __V

Compute ΔV_{SD} __mV

6.3.2.3 ΔT_J data. Optionally calculate ΔT_J if the K factor results (see 4. and 6.1) produce a σ greater than three percent of the average value of K and if the I_H variation between devices to be compared is relatively small.

$$\Delta T_J = K(\Delta V_{GSf}) \,^{\circ}C$$

NOTE: The test apparatus may be capable of directly providing a computed value of ΔT_J.

6.3.2.4 CU data. Optionally calculate CU for comparison purposes if the K factor results (see 4. and 6.1) produce a σ less than three percent of the average value of K and if the I_H variation between devices to be compared is relatively large.

CU = comparison unit

CU = $\Delta V_{GSf}/I_H$ mV/A

NOTE: The test apparatus may be capable of directly providing a computed value of CU.

METHOD 3105.1

MEASUREMENT METHOD FOR THERMAL RESISTANCE
OF A BRIDGE RECTIFIER ASSEMBLY

1. Purpose. This method describes a means to cause current to flow alternately through the legs of a single-phase or three-phase bridge assembly under condition to make it feasible determines its effective thermal resistance. The bridge is operated under steady-state I_O conditions and the current in each leg is interrupted while readings are taken from which to calculate thermal resistance.

2. Definitions. The following symbols and terminology shall apply for the purposes of this test method:

a. V_F: The forward-biased junction voltage of the DUT used for junction temperature sensing. For bridge, this applies to individual legs (i.e., one ac to one dc terminal).

b. V_{F1}: The forward voltage at room temperature at I_{ref}.

c. V_{F2}: The forward voltage at I_{ref} and +100°C above that at V_{F1}.

d. $V_{F2}A$: The computed forward voltage at I_{ref} and at maximum rated T_J.

e. V_{F3}: The initial V_F value at I_{ref} before the application of heating power, with the device at rated case temperature.

f. V_{F4}: The final V_F value at I_{ref} after stabilization of temperatures due to the application of rated current at rated case temperature.

g. ΔV_F: The change in the TSP V_F, due to the application of heating power to the DUT in volts.

h. V_{FH}: The maximum forward voltage resulting from the application of I_O to the DUT.

i. I_O: The rated average current applied to the DUT.

j. I_{ref}: The measurement current used to forward-bias the temperature sensing diode junction for measurement of V_F.

k. TCVF: Voltage-temperature coefficient of V_F with respect to T_J at a fixed value of I_{ref} in V/°C.

l. T_J: The DUT junction temperature.

m. ΔT_J: The change in T_J caused by the application of I_O.

n. TSP: The temperature-sensitive parameter (V_F).

o. t_{F4}: Step trace time.

p. T_N: Reference case temperature for measuring V_N, when N = 1, 2, 3, or 4.

q. $R_{\theta JX}$: Thermal resistance from device junction to a defined reference point (e.g., lead or ambient) in units of °C/W.

r. $R_{\theta JC}$: Thermal resistance from device junction to a defined reference point on the outside surface of the case in units of °C/W.

3. Test circuit. The apparatus required for this test shall include the following, configured as shown on figures 3105-1 and 3105-2.

a. A source of 60 Hz, single or three phase sine wave (AC) capable of being adjusted to the desired value of I_O and able to supply the V_{FH} value required by the DUT. The current source should be able to maintain the desired current to within ±2 percent during the entire time needed for temperature stabilization and measurements.

b. A constant-current source to supply I_{REF} with sufficient compliance voltage range to turn on fully the junction of the diode leg being measured.

c. Anti-parallel fast recovery rectifier diodes with ratings exceeding I_O, to provide isolation of the high-current source from I_{REF} during commutation of I_O between legs.

d. A voltage measurement circuit capable of accurately making the V_F measurements within the available time interval (when the anti-parallel diodes are not conducting), with millivolt resolution.

4. Procedure. Refer to figures 3105-1 and 3105-2, test circuits for single- and three-phase bridges.

a. With S1 open, and DUT at +20°C to +30°C (temperature T_1), read V_{F1} of each leg at current I_{REF}. Elevate the device temperature to +100°C above temperature T_1 (temperature T_2). Allow the device to stabilize until the junction temperature is at T_2. Read V_{F2} of each leg at I_{REF} current. Compute the TCVF of each leg as follows:

$$TCVF = (V_{F1} - V_{F2}) / +100°C$$

Compute the expected V_{F2A} at T_J = maximum rated as follows:

$$V_{F2A} = V_{F1} - [(TCVF) \times (T_{Jmax} - T_1)]$$

Determine the average TCVF and the standard deviation of the TCVF from the readings on each leg. If the standard deviation is less than or equal to three percent of the average value of TCVF, TCVF may be used for all devices. If the standard deviation is greater than three percent of the average value of TCVF, then the individual values of TCVF shall be used in determining the performance of the bridge.

b. With the device held at T_3, at or below rated case temperature of I_O, close S1 and read V_{F3} for each leg.

c. After closing S1, adjust the power source, the load resistor, or both to obtain the maximum rated I_O (either I_{O1} or I_{O2}, depending on the rated T_C selected) and readjust the case temperature to the chosen rated value. Allow the device to achieve stable junction temperatures (see note 1).

d. Measure V_{F4} (see figure 3105-2) for each leg at the same reference current (±1 percent) as in steps a. and b. (The instrumentation used to measure V_{F4} must have sufficient resolution to read it within 2 mV or 2 percent).

NOTE: If V_{F3} for the leg is greater than V_{F2}, T_J is less than T_{Jmax}.

e. Measure V_{FH} for each leg.

f. Compute thermal resistance as follows:

(1) Compute $\Delta V_F = V_{F4} - V_{F3}$ for each leg.

(2) Compute $\Delta T_J = \frac{\Delta V_F}{TCVF}$ 1/

(3) Compute $R_{\theta JC}$ of the full bridge: $R_{\theta JC} = \frac{\Delta T_{JC}}{I_o \times 2V_{FH}}$

Where: ΔT_J is the average of all legs. V_{FH} is the average of all legs and I_O is the rectified output current of the full bridge. 2/ 3/ 4/

5. Test condition to be specified.

I_O ____________________

T_C ____________________

I_{REF} ____________________

Frequency____________________
(if other than 60 Hz)

6. Characteristics to be determined:

Steady state thermal resistance. Unless otherwise specified, junction to care: ______°C/W.

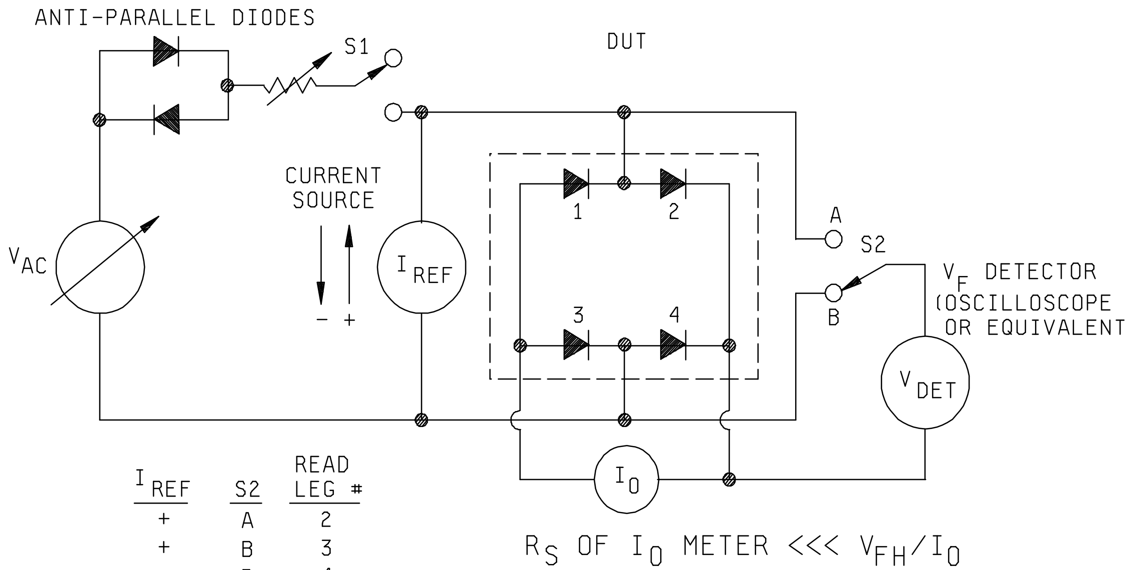
______

1/ If, under power, the case is held to T_4, slightly above T_3, a corrected ΔT_J ($\Delta T_{J(corr)} = \Delta T_{JC} - (T_4 - T_3)$) should be used for step f(2).

2/ Step f(3) gives R_{th} for the bridge. The average per-leg R_{th} for a single-phase bridge is four times the value; six times for a three-phase bridge (see 3/).

3/ If desired, R_{th} of individual legs may be computed from the individual values of ΔT_{JC} and V_{FH}.

4/ The power dissipated $I_O \times 2V_{FH}$ is a reasonable approximation.

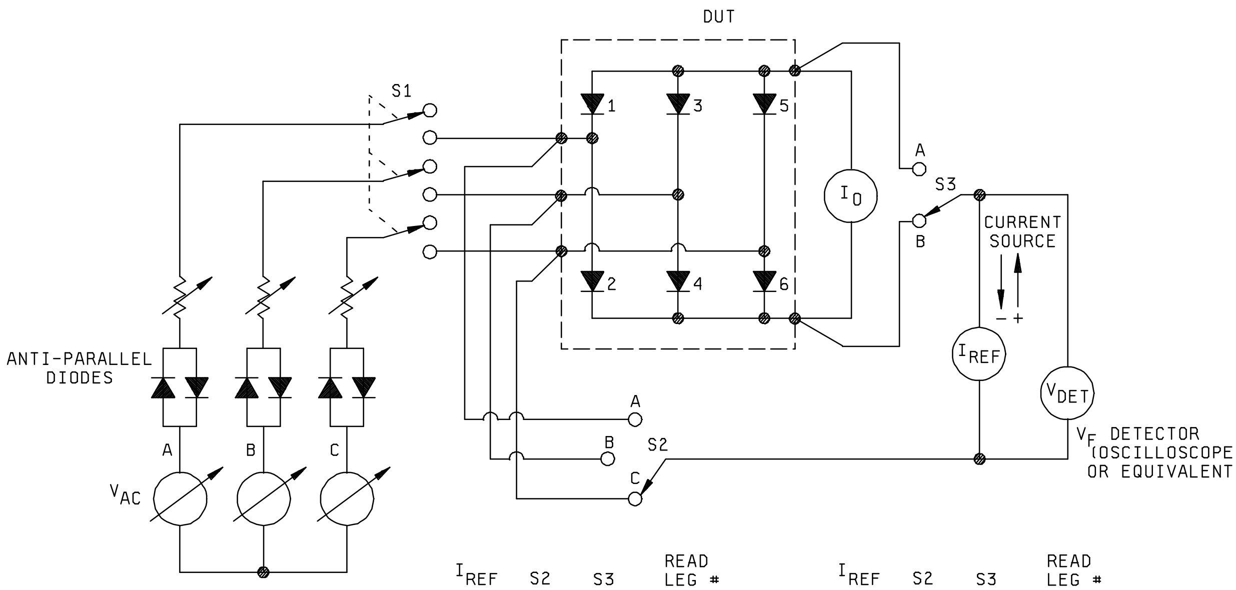


I_{REF}	S2	READ LEG #
+	A	2
+	B	3
−	B	4
−	A	1

NOTES:

1. All voltage measurements shall be made using leads Kelvin-connected directly to the bridge terminals.
2. V_{AC} is adjusted so that the V_{F4} step (t_{F4}) shown on figure 3105-3 is 100 µs ±50 µs and is clearly defined. A typical V_{AC} might be 10 volts peak. Bridges with parasitic inductive components must adjust V_{AC} so that after the inductive ringing settles, the V_{F4} step on figure 3105-3 (t_{F4}) is 100 µs ±50 µs.

FIGURE 3105-1. Single phase bridge.



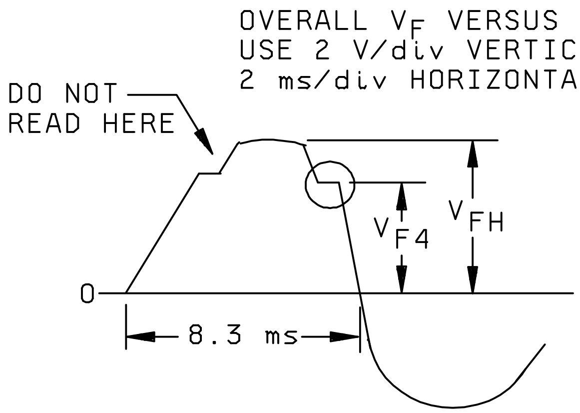
I_{REF}	S2	S3	READ LEG #
+	A	A	1
+	B	A	3
+	C	A	5

I_{REF}	S2	S3	READ LEG #
–	A	B	2
–	B	B	4
–	C	B	6

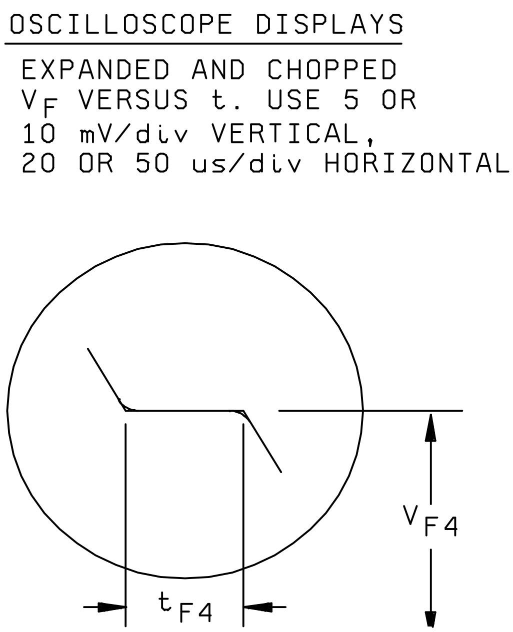
NOTES:

1. All voltage measurements shall be made using leads Kelvin-connected directly to the bridge terminals.
2. V_{AC} is adjusted so that the V_{F4} step (t_{F4}) shown on figure 3105-3 is 100 μs ±50 μs and is clearly defined. A typical V_{AC} might be 10 volts peak. Bridges with parasitic inductive components must adjust V_{AC} so that after the inductive ringing settles, the V_{F4} step on figure 3105-3 (t_{F4}) is 100 μs ±50 μs.

FIGURE 3105-2. Three phase bridge.



NOTE: V_{F4} "step trace" is provided when anti-parallel diodes in circuit briefly commutate off (the ac current passes through zero during each cooling cycle of individual bridge legs under ac test conditions.)



NOTES:

1. Polarity shown applies when I_{REF} is positive. The trace in inverted when I_{REF} is negative.
2. V_{AC} is adjusted so that the V_{F4} step (t_{F4}) shown on figure 3105-3 is 100 µs ±50 µs and is clearly defined. A typical V_{AC} might be 10 volts peak. Bridges with parasitic inductive components must adjust V_{AC} so that after the inductive ringing settles, the V_{F4} step on figure 3105-3 (t_{F4}) is 100 µs ±50 µs.

FIGURE 3105-3. Oscilloscope displays.

METHOD 3126

THERMAL RESISTANCE
(COLLECTOR-CUTOFF-CURRENT METHOD)

1. Purpose. The purpose of this test is to measure the thermal resistance of the device under the specified conditions. This method is particularly applicable to the measurement of germanium devices having relatively large thermal response times.

2. Test circuit. See figure 3126-1.

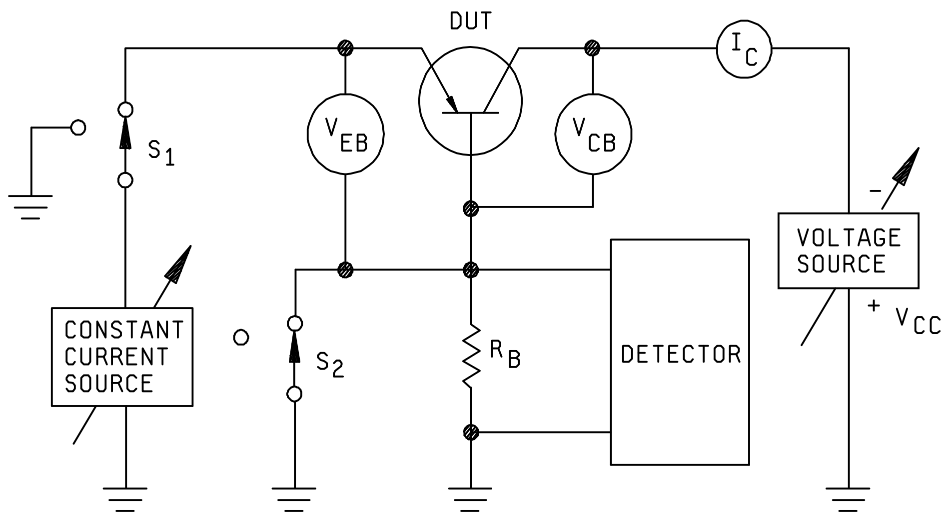


FIGURE 3126-1. Test circuit for thermal resistance (collector-cutoff-current method).

3. Procedure. Switches S1 and S2 are ganged and are operated such that the time they are closed (heat interval) is much larger than the time they are open (measurement interval). S1 is arranged to open slightly before S2 opens, and the interval between the opening of S1 and S2 is adjusted to be short compared to the thermal time constant of the device being measured. The length of the measurement interval should be short compared to the thermal response time of the transistor being measured. When both switches are open, the value of I_{CBO} is read as the drop across R_B. If the I_{CBO} varies during the measurement interval, the value immediately following the opening of S2 should be read. A calibrated oscilloscope makes a convenient detector. Care should be taken that the collector voltage stays constant.

3.1 Measurement interval. The measurement is made in the following manner: The case, ambient, or other reference point is elevated to a high temperature T_2, not exceeding the maximum junction temperature, and the cutoff current, I_{CBO}, read with the constant-current source supplying no current. The reference temperature is then reduced to a lower temperature T_1, and power, P_1, is applied to heat the transistor, by increasing the current from the constant current source, until the same value of I_{CBO} is read as was read above.

$$\text{Then: } \theta = \frac{T_2 - T_1}{P_1}$$

$$\text{Where: } P_1 = (n)(I_C V_{CC} + I_E V_{EB})$$

$$n = \text{duty cycle} \left(\frac{t_{on}}{t_{total}}\right)$$

4. Summary. The following conditions shall be specified in the detail specification:

a. Test temperature (see 3.).

b. Test voltages or currents (see 3.).

METHOD 3131.4

*STEADY-STATE THERMAL IMPEDANCE AND TRANSIENT THERMAL IMPEDANCE TESTING OF TRANSISTORS (DELTA BASE – EMITTER VOLTAGE METHOD)

* 1. Purpose. The purpose of this test is to determine the thermal performance of transistor devices. This can be done in two ways, steady-state thermal impedance or thermal transient testing. Steady-state thermal impedance (referred to as thermal resistance) determines the overall thermal performance of devices. A production-oriented screening process, referred to as transient thermal impedance testing, is a subset of steady-state thermal impedance testing and determines the ability of the transistor chip-to-header interface to transfer heat from the chip to the header, and is a measure of the thermal quality of the die attachment. It is relevant to designs which use headers, or heat conducting plugs, with mass and thermal conductivity allowing effective discrimination of poor die attachments. This is particularly true with power devices. The method can be applied to small signal, power, switching and Darlington transistors. This method is intended for production monitoring, incoming inspection, and pre-burn in screening applications. The measurement current (IM) must be large enough to ensure that the Darlington output transistor is biased into the linear conduction mode of the temperature sensing measurement periods of the thermal test.

* 1.1 Background and scope for transient thermal impedance testing. Transient thermal impedance of semiconductor devices are sensitive to the presence of voids in the die attachment material between the semiconductor chip and package since voids impede the flow of heat from the chip to the substrate (package). Due to the difference in the thermal time constants of the chip and package, the measurement of transient thermal impedance can be made more sensitive to the presence of voids than can the measurement of steady-state thermal impedance. This is because the chip thermal time constant is generally several orders of magnitude shorter than that of the package. Thus, the heating power pulse width can be selected so that only the chip and the chip-to-substrate interface are heated during the pulse by using a pulse width somewhat greater than the chip thermal time constant but less than that of the substrate. Heating power pulse widths ranging from 1 to 400 ms for various package designs have been found to satisfy this criterion. This enables the detection of voids to be greatly enhanced, with the added advantage of not having to heat sink the device under test (DUT). Thus, the transient thermal impedance techniques are less time consuming than the measurement of thermal resistance for use as a manufacturing screen, process control, or incoming inspection measure for die attachment integrity evaluation.

* 2. Definitions. The following symbols and terminology shall apply for the purpose of this test method:

a. V_{BE}: The forward biased base-emitter junction voltage of the DUT used for junction temperature sensing.

V_{BEi}: The initial V_{BE} value during application of measurement current (IM) and before application of heating power.

V_{BEf}: The final V_{BE} value during the sample window time (t_{SW}) after application and subsequent removal of heating power.

b. ΔV_{BE}: The change in, V_{BE}, (VBEi-VBEf) due to the application of heating power to the DUT.

c. I_H: The collector current applied to the DUT during the heating period.

d. V_{CE}: The voltage between the collector and emitter. V_{CE} is constant throughout the test.

e. P_H: The heating power applied the DFUT. $P_H = I_H . x\ V_{CE}$.

f. t_H: The duration of the heating power pulse P_H.

g. ti: The time after application of the measurement current (IM) and before application of the heating power pulse.

h. I_M: The measurement current applied to forward bias the junction for measurement of V_{BE}.

i. t_{MD}: Measurement delay time is the time from the end of the heating power pulse to the beginning of the sample window time (t_{SW}). Delay must be sufficient in length to allow for attenuation of switching transients to occur. The delay time will vary according to the length of the cable to test fixture and associated fixture inductances.

j. t_{SW}: Sample window time during which final V_{BE} measurement is made. The value of t_{SW} should be small; and occur at precisely the conclusion of tMD. It can approach zero if an oscilloscope is used for manual measurements and no transient effects are present.

k. VTC: Voltage-temperature coefficient of V_{BE} with respect to T_J at a fixed value of I_M; in mV/°C.

l. K: Thermal calibration factor equal to the reciprocal of VTC; in °C/mV.

* m. CU: The comparison unit, consisting of ΔV_{BE} divided by V_{BE}, that is used to normalize the transient thermal impedance for variations in power dissipation; in units of mV/V.

n. T_J: The DUT junction temperature.

o. ΔT_J: The change in T_J caused by the application of P_H for a time equal to t_H.

* p. $Z_{\theta JX}$: Transient. Thermal impedance from device junction to a time defined reference point; in units of °C/W.

* q. $Z_{\theta JC}$: Transient. Thermal impedance from device junction to a point on the outside surface of the case immediately adjacent to the device chip measured using time equal time constant of device; in units of °C/W.

* r. $R_{\theta JX}$: Steady-state. Thermal resistance from device junction to a defined reference point; in units of °C/W.

* s. $R_{\theta JC}$: Steady-state. Thermal resistance from device junction to a point on the outside surface of the case immediately adjacent to the device chip; in units of °C/W.

* t. $R_{\theta JA}$: Steady-state. Thermal resistance from device junction to an ambient (world); in units of °C/W.

u. TSP: The temperature sensitive parameter; V_{BE}.

3. Apparatus. The apparatus required for this test shall include the following, configured as shown on figure 3131-1, as applicable to the specified test procedure:

a. A constant current source capable of adjustment to the desired value of I_H and able to supply the V_{BE} value required by the DUT. The current source should be able to maintain the desired current to within ±2 percent during the entire length of heating time.

b. A constant current source to supply I_M with sufficient voltage compliance to turn the TSP junction fully on.

c. An electronic switch capable of switching between the heating period conditions and measurement conditions in a time frame short enough to avoid DUT cooling during the transition; this typically requires switching in the microsecond or tens of microseconds range.

d. A voltage measurement circuit capable of accurately making the V_{BEf} measurement within the time frame with millivolt resolution.

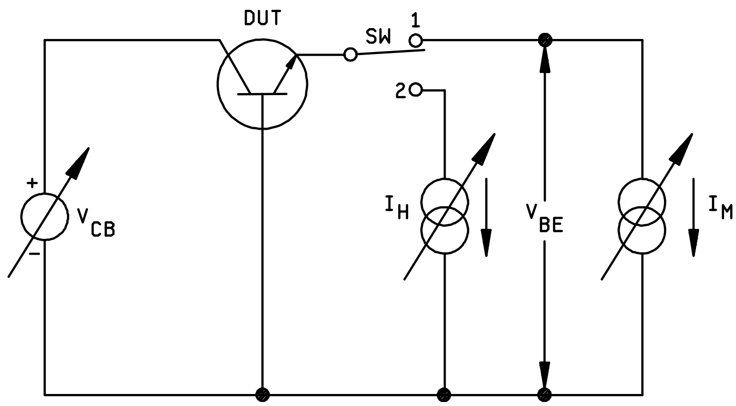


FIGURE 3131-1. Thermal impedance testing setup for transistors.

4. Test operation.

4.1 General description. The test begins with the adjustment of I_M and I_H to the desired values. The value of I_H is usually at least 50 times greater than the value of I_M. Then with the electronic switch in position 1, the value of V_{BEi} is measured. The switch is then moved to position 2 for a length of time equal to t_H and the value of V_{BE} is measured. Finally, at the conclusion of t_H, the switch is again moved to position 1 and the V_{BEf} value is measured within a time period defined by t_{MD} (or t_{MD} + t_{SW}, depending on the definitions stated previously). The two current sources are then turned off at the completion of the test.

4.2 Notes.

a. Some test equipment may provide a ΔVBE directly instead of V_{BEi} and V_{BEf}; this is an acceptable alternative. Record the value of ΔV_{BE}.

b. Some test equipment may provide $Z_{\theta JX}$ directly instead of V_{BEi} and V_{BEf} for thermal resistance calculations; this is an acceptable alternative. Record the value of $Z_{\theta JX}$.

c. Alternative waveforms, as may be generated by ATE using the general principles of this method, may be used upon approval of the qualifying activity.

5. Acceptance limit.

5.1 General discussion. Variations in transistor characteristics from one manufacturer to another cause difficulty in establishing a single acceptance limit for all transistors tested to a given specification. Ideally, a single acceptance limit value for ΔV_{BE} would be the simplest approach. However, different design, materials, and processes can alter the resultant ΔV_{BE} value for a given set of test conditions. Listed below are several different approaches to defining acceptance limits. The ΔV_{BE} limit is the simplest approach and is usually selected for screening purposes. Paragraphs 5.3 through 5.6 require increasingly greater detail or effort.

5.2 ΔV_{BE} limit. A single ΔV_{BE} limit is practical if the K factor and V_{BE} values for all transistors tested to a given specification are nearly identical. Since these values may be different for different manufacturers, the use of different limits is likely to more accurately achieve the desired intent. (A lower limit does not indicate a better die bond when comparing different product sources.) The transistor specifications would list the following test conditions and measurement parameters:

a. I_H (in A).

b. t_H (in ms).

c. I_M (in mA).

d. t_{MD} (in µs).

e. t_{SW} (in µs).

f. ΔV_{BE} (maximum limit value, in mV).

5.3 ΔT_J limit. (Much more involved than ΔVBE , but useful for examining questionable devices.) Since ΔT_J is the product of K (in accordance with 6.) and ΔV_{BE}, this approach is the same as defining a maximum acceptable junction temperature rise for a given set of test conditions.

5.4 CU limit. (Slightly more involved than ΔT_J.) The ΔT_J limit approach described above does not take into account potential power dissipation variations between devices. The V_{BE} value can vary, depending on chip design and size, thus causing the power dissipation during the heating time to be different from device to device. This variation will be small within a lot of devices produced by a single manufacturer but may be large between manufacturers. A CU limit value takes into account variations in power dissipation due to differences in V_{BE} by dividing the ΔV_{BE} value by V_{BE}.

5.5 (K•CU) limit. (Slightly more involved but provides greater detail.) This is a combinational approach that takes into account both K factor and power dissipation variations between devices.

* 5.6 $Z_{\theta JX}$ limit. (For full characterization; not required for screening purposes, but preferred if the proper ATE is available.) The transient thermal impedance approach uses an absolute magnitude value specification that overcomes the problems associated with the other approaches. transient Thermal impedance is time dependent and is calculated as follows:

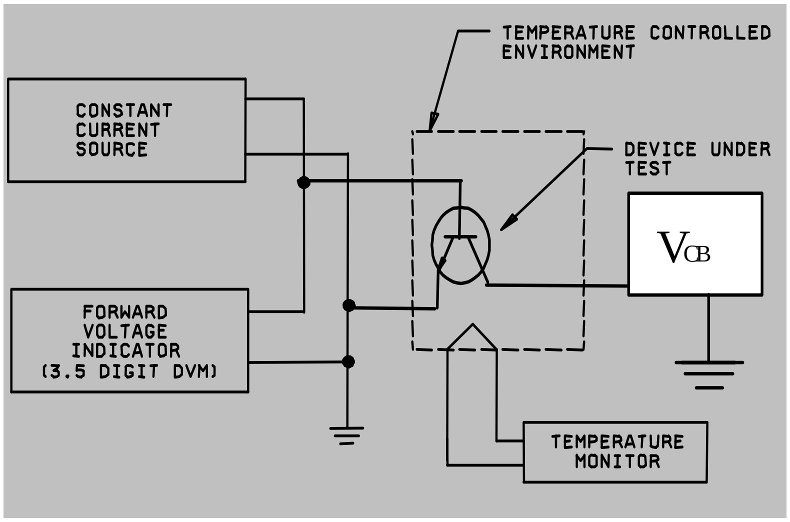
$$Z_{\Theta JX} = \frac{\Delta T_J}{P_D} = \left| \frac{(K)(\Delta V_{BE})}{(I_H)(V_H)} \right| {}^{o}\mathrm{C/W}$$

5.7 $R_{\theta JX}$ limit. (For thermal resistance specification testing.) The thermal resistance to some defined point, such as the case, is an absolute magnitude value specification used for equilibrium conditions. The t_H heating time must therefore be extended to appreciably longer times (typically 20 to 50 seconds). In the example of $R_{\theta JC}$ measurements, the case must be carefully stabilized and monitored in temperature which requires an infinite heat sink for optimum results. The ΔT_J is the difference in junction temperature to the case temperature for the example of $R_{\theta JC}$.

$$R_{\Theta JX} = \frac{\Delta T_J}{P_D} = \left| \frac{(K)(\Delta V_{BE})}{(I_H)(V_H)} \right| {}^{o}\mathrm{C/W}$$

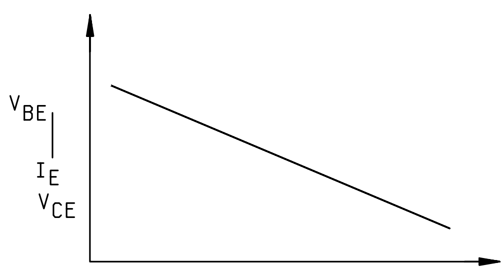
* 5.8 General comment for transient thermal impedance testing. One potential problem in using the transient thermal impedance testing approach lies in trying to make accurate enough measurements with sufficient resolution to distinguish between acceptable and nonacceptable transistors. As the DUT current handling capability increases, the thermal impedance under transient conditions will become a very small value. This raises the potential for rejecting good devices and accepting bad ones. Higher I_H values must be used in this case.

6. Measurement of the TSP V_{BE}. The calibration of V_{BE} versus T_J is accomplished by monitoring V_{BE} for the required value of I_M as the environmental temperature (and thus the DUT temperature), and is varied by external heating. It is not required if the acceptance limit is ΔV_{BE} (see 5.2), but is relevant to the other acceptance criteria (see 5.3 through 5.6). The magnitude of I_M shall be chosen so that V_{BE} is a linearly decreasing function over the normal T_J range of the device. I_M must be large enough to ensure that the base-emitter junction is turned on but not large enough to cause significant self-heating. An example of the measurement method and resulting calibration curve is shown on figure 3131-2.



Step 1: Measure V_{BE1} at T_{J1} using I_M
Step 2: Measure V_{BE2} at T_{J2} using I_M

Step 3: $K = \left| \frac{T_{J2} - T_{J1}}{V_{BE2} - V_{BE1}} \right| °C/mV$



I_M: Must be large enough to overcome surface leakage effects but small enough not to cause significant self-heating.

T_J: Is externally applied (e.g., via oven, liquid) environment.

FIGURE 3131-2. Example curve of V_{BE} versus T_J.

A calibration factor K (which is the reciprocal of the slope of the curve on figure 3131-2) can be defined as:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{BE2} - V_{BE1}} \right| \; °C/mV$$

The K factor is used to calibrate the DUT such that the measured forward voltage drop corresponds to the temperature of the junction at a given bias condition. In order to ensure accurate results, the bias conditions used to determine the K factor must be chosen such that the application is duplicated. Therefore, the results will be unique for each particular biasing condition and should be reestablished for different values of base and/or collector currents (IF for diodes). This method should be used for each of the following conditions: Transient thermal impedance, burn-in, and life tests. Verify actual TJ seen by a device in field applications.

It has been found experimentally that the K-factor variation for all devices within a given device type class is small. The usual procedure is to perform a K factor calibration on a 10 piece to 12 piece sample from a device lot and determine the average K and standard deviation (σ). If σ is less than or equal to three percent of the average value of K, then the average value of K can be used for all devices within the lot. If σ is greater than three percent of the average value of K, then all the devices in the lot shall be calibrated and the individual values of K shall be used in determining device acceptance. As an alternative to using individual values of K, the manufacture may establish internal limits unique to their product that ensures atypical product removal from the population (lot-to-lot and within-the-lot). The manufacturer shall use statistic techniques to establish the limits to the satisfaction of the government.

7. Establishment of test conditions and acceptance limits. Thermal resistance measurements require that I_H be equal to the required value stated in the device specifications, typically at rated current or higher. Values for t_H, t_{MD}, and heat sink conditions are also taken from the device specifications. The steps shown below are primarily for transient thermal impedance testing and thermal characterization purposes.

The following steps describe how to set up the test conditions and determine the acceptance limits for implementing the transient thermal test for die attachment evaluation using the apparatus and definitions stated above.

7.1 Initial device testing procedure. The following steps describe in detail how to set up the apparatus described previously for proper testing of various transistors. Since this procedure thermally characterizes the transistor out to a point in heating time required to ensure heat propagation into the case (i.e., the $R_{\theta JX}$ condition), an appropriate heat sink should be used or the case temperature should be monitored.

* Step 1: From a 20 to 25 piece sample, pick any one diode to start the setup process. Set up the test apparatus as follows:

I_H = 1.0 A	(Or some other desired value near the DUTs normal operating current, typically higher for power transistors.
t_H = 10-50 ms	Unless otherwise specified, for most devices rated up to 15 W power dissipation.
50 - 100 ms	Unless otherwise specified, for most devices rated up to 200 W power dissipation.
* ≥ 250 ms	For steady-state thermal impedance measurement. The pulse must be shown to correlate to steady-state conditions before it can be substituted for steady-state condition.

t_{MD} = 100 µs max   A larger value may be required on power devices with inductive package elements which generate nonthermal electrical transients; unless otherwise specified, this would be observed in the t_3 region of figure 3131-3.

I_M = 10 mA   (Or some nominal value approximately two percent, or less, of I_H.)

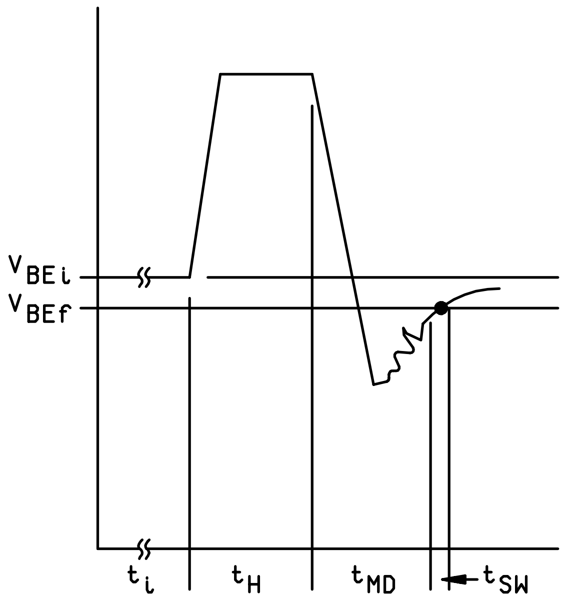


FIGURE 3131-3. Thermal impedance testing waveforms.

Step 2: Insert device into the apparatus test fixture and initiate a test. (For best results, a test fixture that offers some form of heat sinking would be desirable. Heat sinking is not needed if either the power dissipation during the test is well within the diode's free-air rating or the maximum heating time is limited to less than that required for the heat to propagate through the case.)

Step 3: If ΔV_{BE} is in the 15 to 80 mV range then proceed to the next step. This range approximately corresponds to a junction temperature change of roughly +10°C to +50°C and is sufficient for initial comparison purposes.

If ΔV_{BE} is less than 15 mV, return to 7.1, step 1 and increase heating power into device by increasing I_H.

If ΔV_{BE} is greater than 80 mV, approximately corresponding to a junction temperature change greater than +50°C, it would be desirable to reduce the heating power by returning to 7.1, step 1 and reducing I_H.

NOTE: The test equipment shall be capable of resolving ΔV_{BE} to within five percent. If not, the higher value of ΔV_{BE} must be selected until the five percent tolerance is met. Two different devices can have the same junction temperature rise even when P_H is different, due to widely differing V_{BE}. Within a given lot, however, a higher V_{BE} is more likely to result in a higher junction temperature rise. For such examples, this screen can be more accurately accomplished using the CU value. As defined in 2m., CU provides a comparison unit that takes into account different device V_{BE} values for a given I_H test condition.

Step 4: Test each of the sample devices and record the data detailed in 8.1.

Step 5: Select out the devices with the highest and lowest values of CU or $Z_{\theta JX}$ and put the remaining devices aside.

The ΔV_{BE} values can be used instead of CU or $Z_{\theta JX}$ if the measured values of V_{BE} are very tightly grouped around the average value.

Step 6: Using the devices from 7.1, step 5, collect and plot the heating curve data for the two devices in a manner similar to the examples shown on figure 3131-4.

Step 7: Interpretation of the heating curves is the next step. Realizing that the thermal characteristics of identical chips should be the same if the heating time (t_H) is less than or equal to the thermal time constant of the chip, the two curves should start out the same for the low values of t_H. Non-identical chips (thinner or smaller in cross section) will have completely different curves, even at the smaller values of t_H. As the value of t_H is increased, thereby exceeding the chip thermal constant, heat will have propagated through the chip into the die attachment region. Since the heating curve devices of 7.1, step 5 were specifically chosen for their difference, the curves of figure 3131-4 diverge after t_H reaches a value where the die attachment variance has an affect on the device junction temperature. Increasing t_H further will probably result in a flattening of the curve as the heating propagates in the device package. If the device package has little thermal mass and is not well mounted to a good heat sink, the curve will not flatten very much, but will show a definite change in slope.

Step 8: Using the heating curve, select the appropriate value of t_H to correspond to the inflection point in the transition region between heat in the chip and heat in the package.

If there are several different elements in the heat flow path: Chip, die attachment, substrate, substrate attach, and package, for example in a hybrid, there will be several plateaus and transitions in the heating curve. Appropriate selection of t_H will optimize evaluation sensitivity to other attachment areas.

Step 9: Return to the apparatus and set t_H equal to the value determined from 7.1, step 8.

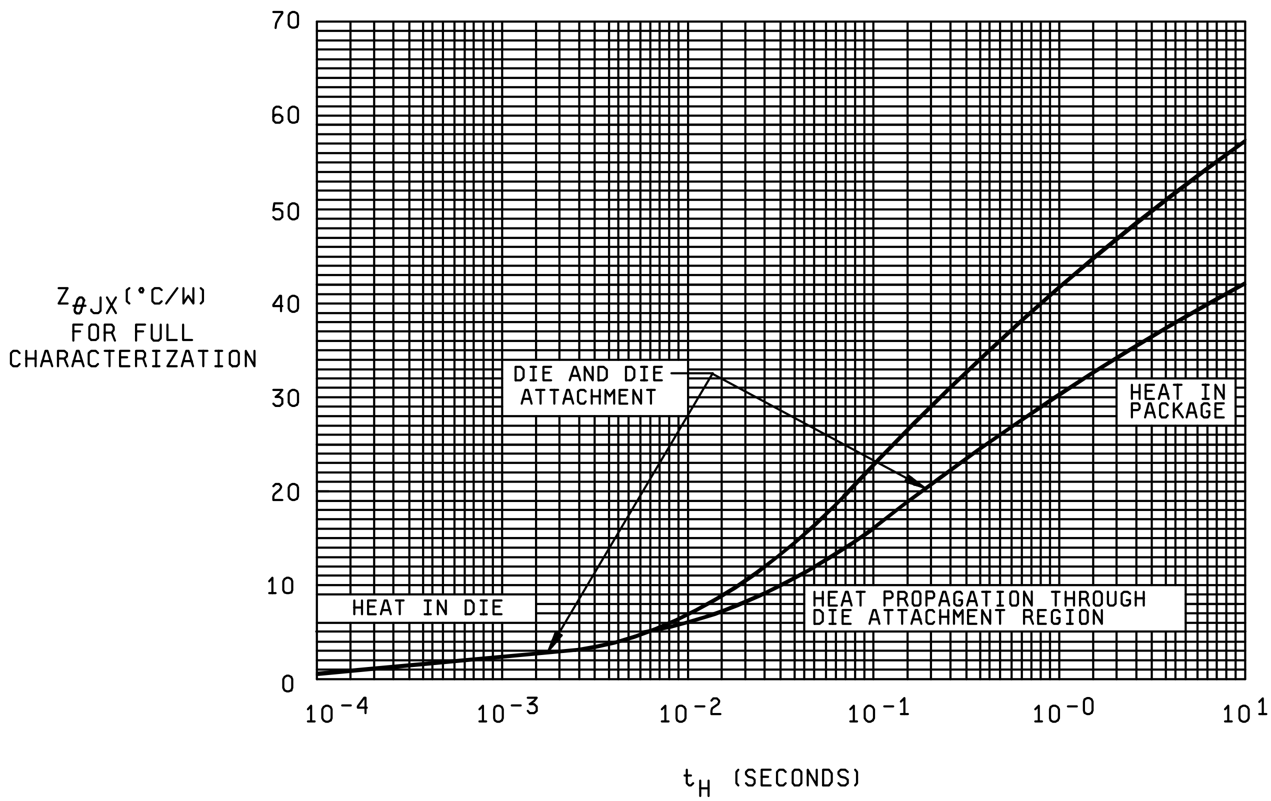


FIGURE 3131-4. Heating curves for two extreme devices.

Step 10: Because the selected value of t_H is much less than that for thermal equilibrium, it is possible to significantly increase the heating power without degrading or destroying the device. The increased power dissipation within the DUT will result in higher ΔV_{BE} or CU values that will make determination of acceptable and nonacceptable devices much easier.

Step 11: The pass/fail limit, the cut-off point between acceptable and nonacceptable devices, can be established in a variety of ways:

a. Correlation to other die attachment evaluation methods, such as die shear and x-ray, while these two methods have little actual value from a thermal point of view, they do represent standardization methods as described in various military standards.

b. Maximum allowable junction temperature variations between devices, since the relationship between ΔT_J and ΔV_{BE} is about 0.5°C/mV for forward bias testing, or 0.25C/mV for Darlington transistors, the junction temperature spread between devices can be easily determined. The T_J predicts reliability. Conversely, the T_J spread necessary to meet the reliability projections can be translated to a ΔV_{BE} or CU value for pass/fail criteria.

To fully utilize this approach, it will be necessary to calibrate the devices for the exact value of the T_J to V_{BE} characteristic. The characteristic's slope, commonly referred to as K factor, is easily measured on a sample basis using a voltmeter, environmental chamber, temperature indicator, and a power supply setup as described in 6. A simple set of equations yield the junction temperature once K and ΔV_{BE} are known:

$$\Delta T_J = (K)(\Delta VBE)$$

$$T_J = T_A + \Delta T_J$$

Where: T_A is the ambient or reference temperature. For thermal transient test conditions, this temperature is usually equivalent to case temperature (T_C) for case mounted devices.

c. Statistically from a 20 to 25 device sample, the distribution of ΔV_{BE} or CU values should be a normal one with defective devices out of the normal range. Figure 3131-5 shows a ΔV_{BE} distribution for a sample lot of transistors. NOTE: The left-hand side of the histogram envelope is fairly well defined but the other side is greatly skewed to the right. This comes about because the left-hand side is constrained by the absolutely best heat flow that can be obtained with a given chip assembly material and process unless a test method error is introduced. The other side has no such constraints because there is no limit as to how poorly a chip is mounted.

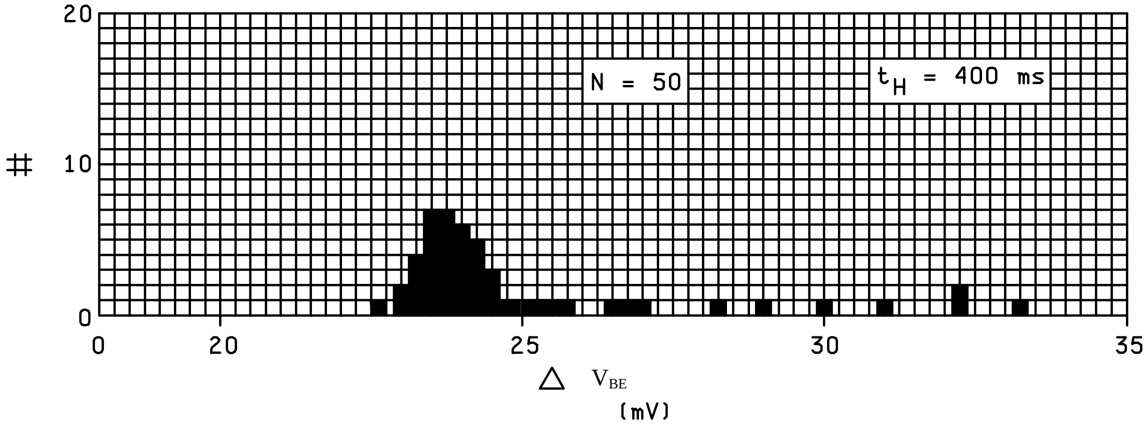


FIGURE 3131-5. Typical ΔV_{BE} distribution.

The usual rule of thumb in setting the maximum limit for ΔV_{BE} , CU, or $Z_{\theta JX}$ is to use the distribution average value and three standard deviations (σ). For example:

$| (\Delta V_{BE}) | = \overline{\Delta V_{BE}} + X \sigma$

high
limit

$| (CU) | = \overline{CU} + X \sigma$

high
limit

$| (Z_{\theta JX}) | = \overline{Z_{\theta JX}} + X \sigma$

high
limit

Where: X = 3 in most cases and $\overline{\Delta V_{BE}}$, $\overline{\Delta CU}$, and $\overline{\Delta Z_{\theta JX}}$ are the average distribution values.

The statistical data required is obtained by testing 25 or more devices under the conditions of 7.1, step 11.

The maximum limit determined from this approach should be correlated to the transistor's specified thermal resistance. This will ensure that the ΔV_{BE} or CU limits do not pass diodes that would fail the thermal resistance or transient thermal impedance requirements.

Step 12: Once the test conditions and pass/fail limit have been determined, it is necessary only to record this information for future testing requirements of the same device in the same package. It is also recommended that a minimum limit is established to ensure a test method error or other anomaly is investigated.

Step 13: After the pass/fail limits are established, there shall be verification they correllate to good and bad bonded devices or the electrical properties such as surge.

The steps listed hereto are conveniently summarized in table 3131-I.

TABLE 3131-I. Summary of test procedure steps.

General description		Steps	Comments
A	Initial setup	1 through 4	Approximate instrument settings to find variations among devices in 10 to 15 piece sample.
B	Heating curve generation	5 through 6	Using highest and lowest reading devices, generate heating curves.
C	Heating curve interpretation	7 through 9	Heating curve is used to find more appropriate value for t_H corresponding to heat in the die attachment area (for some other desired interface in the heat flow path).
D	Final setup	10	Heating power applied during t_H is increased in order to improve measurement sensitivity to variations among devices.
E	Pass-fail determination	11 through 12	A variety of methods is available such as JESD 34 for setting the fail limit; the statistical approach is the fastest and easiest to implement.
F	Verification	13	Mechanical / Electrical correlation

7.2 Routine device thermal transient testing procedure. Once the proper control settings have been determined for a particular device type from a given manufacturing process or vendor, repeated testing of that device type simply requires that the same test conditions be used as previously determined. New device types or the same devices manufactured with a different process will require a repeat of 7.1 for proper thermal transient test conditions.

8. Test conditions and measurements to be specified and recorded.

* 8.1 Transient thermal impedance-steady-state thermal impedance measurements.

8.1.1 Test conditions. Specify the following test conditions:

a. I_M measuring current ___ mA

b. I_H heating current ___ A

c. t_H heating time ___ ms

d. t_{MD} measurement time delay ___µs

e. t_{SW} sample window time __ µs

8.1.2 Data. Record the following data:

a. V_{BEi} initial forward voltage ___V

b. V_H heating voltage ___V

c. V_{BEf} final forward voltage ___V

(NOTE: Some test equipment may provide a ΔV_{BE} instead of V_{BEi} and V_{BEf}; this is an acceptable alternative. Record the value of ΔV_{BE}.

Some test equipment may provide direct display of calculated CU or $Z_{\theta JX}$; this is an acceptable alternative. Record the value of CU or $Z_{\theta JX}$.

8.2 K factor calibration. (Optional for criteria 8.3a or 8.3b, mandatory for 8.3c, 8.3d, or 8.3e.)

8.3 Test conditions. Specify the following test conditions:

a. I_M current magnitude ___mA

b. Initial junction temperature ___°C

c. Initial V_{BE} voltage ___mV

d. Final junction temperature ___°C

e. Final V_{BE} voltage ___mV

8.4 K factor. Calculate K factor in accordance with the following equation:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{BE2} - V_{BE1}} \right| \ °C/mV$$

K factor ___°C/mV

8.5 Specification limit calculations. One or more of the following should be measured or calculated, as called for on the device specification (see 5.1):

ΔV_{BE}	___mV
CU	___mV/V
ΔT_J	___°C
K•CU	___°C/V
$Z_{\theta JX}$	___°C/W
$R_{\theta JX}$	___°C/W

METHOD 3132

THERMAL RESISTANCE

(DC FORWARD VOLTAGE DROP, EMITTER BASE, CONTINUOUS METHOD)

1. Purpose. The purpose of this test is to measure the thermal resistance of the device under the specified conditions.

2. Test circuit. See figure 3132-1.

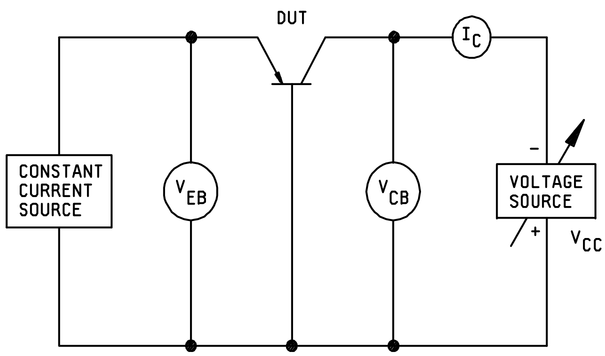


FIGURE 3132-1. Test circuit for thermal resistance (dc forward voltage drop, emitter base, continuous method).

3. Procedure. The measurement technique assumes that the forward emitter voltage drop varies with temperature. It further assumes that during the course of measurement, the variation in forward emitter voltage drop varies monotonically due to temperature and is much greater than that due to the variation with collector voltage.

3.1 Measurement. The measurement is made in the following manner: The case, ambient, or other reference point is elevated to a high temperature T_2, not exceeding the maximum junction temperature. Current I_C is set to a value and a voltage applied to the collector base diode, V_2. The value of V_2 applied shall be low yet high enough so that the device is operating in a normal manner. V_{1EB} is read under these conditions. The reference temperature is reduced to a lower temperature T_1 and V_{CC} varied until the same value of V_{1EB} is read as was read above. The thermal resistance is then

$$\theta = \frac{T_2 - T_1}{I_C\ (V_1 - V_2)}$$

Where: V_1 is the collector voltage applied at temperature T_1.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test temperatures.

b. I_C and V_2.

METHOD 3136

THERMAL RESISTANCE

(FORWARD VOLTAGE DROP, COLLECTOR TO BASE, DIODE METHOD)

1. Purpose. The purpose of this test is to measure the thermal resistance of the device under the specified conditions. This method is particularly applicable to the measurement of germanium and silicon devices having relatively long thermal response times.

2. Test circuit. See figure 3136-1.

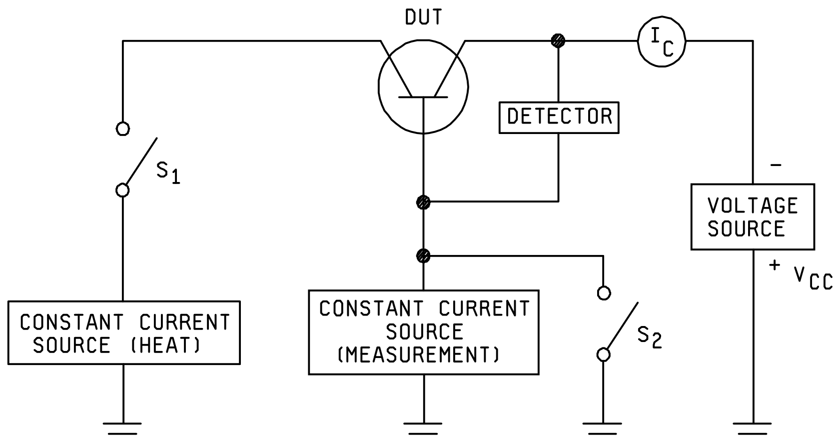


FIGURE 3136-1. Test circuit for thermal resistance (forward voltage drop, collector to base, diode method).

3. Procedure. Switches S1 and S2 are ganged switches and are so arranged that S2 opens very shortly after S1 opens and such that the delay between the openings is much shorter than the thermal response time of the device being measured. S1 and S2 should be closed (heat interval) for a much larger time than they are open (measurement interval) and the measurement interval should be short compared to the thermal response time of the device being measured.

3.1 Measurement. The measurement is made in the following manner: The case, ambient, or other reference point is elevated to a high temperature T_2, not exceeding the maximum junction temperature, and the collector-base voltage, V_{CB}, is read. This reading is made at the beginning of the measurement interval. An oscilloscope makes a convenient detector. The reference temperature is then reduced to a lower temperature, T_1. The heating power, P_1, is adjusted by adjusting the heating current source in the emitter circuit until the same value of V_{CB} is read as was read above. The value of Θ is calculated from the equation:

$$\theta = \frac{T_2 - T_1}{P_1}$$

Where: $P_1 = (n)\,(I_C V_{CC} + I_E V_{EB})$

$$and\ \ n = duty\ cycle\left[\frac{t_{on}}{t_{total}}\right]$$

4. Summary. The following conditions shall be specified in the detail specification:

a. Test temperature (see 3.1).

b. Test voltages and currents (see 3.).

METHOD 3141

THERMAL RESPONSE TIME

1. Purpose. The purpose of this test is to measure the time required for the junction to reach 90 percent of the final value of junction temperature change following application of a step function of power dissipation under specified conditions.

2. Apparatus. The apparatus used to determine the thermal response time shall be capable of demonstrating device conformance to the minimum requirements of the individual specification.

3. Procedure. The thermal response time shall be determined by measuring the time required for the junction temperature (as indicated by a precalibrated temperature sensitive electrical parameter) to reach 90 percent of the final value of junction temperature change caused by a step function in power dissipation when the device case or ambient temperature, as specified, is held constant.

4. Summary. The device case or ambient temperature shall be specified in the detail specification.

METHOD 3146.1

THERMAL TIME CONSTANT

1. Purpose. The purpose of this test is to measure the time required for the junction to reach 63.2 percent of the final value of junction temperature change following application of a step function of power dissipation under specified conditions.

2. Apparatus. The apparatus used to determine the thermal time constant shall be capable of demonstrating device conformance to the minimum requirements of the individual specification.

3. Procedure. The thermal time constant shall be determined by measuring the time required for the junction temperature (as indicated by a precalibrated temperature sensitive electrical parameter) to reach 63.2 percent of the final value of junction temperature change caused by a step function in power dissipation, when the device case or ambient temperature, as specified, is held constant.

4. Summary. The device case or ambient temperature shall be specified in the detail specification.

METHOD 3151

THERMAL RESISTANCE, GENERAL

1. Purpose. The purpose of this test is to measure the temperature rise per unit power dissipation of the designated junction above the case of the device or ambient temperature, under conditions of steady state operation.

2. Apparatus. The apparatus used to determine the thermal resistance shall be capable of demonstrating device conformance to the minimum requirements of the individual specification.

3. Procedure. The thermal resistance may be determined by:

a. Measuring the junction power required to maintain the junction temperature constant (as indicated by a precalibrated temperature sensitive electrical parameter) when the case of the device or ambient temperature, as specified, is changed by a known amount.

b. Measuring the junction temperature (as indicated by a precalibrated temperature sensitive electrical parameter) when the junction power is changed a known amount while the case of the device or ambient temperature, as specified, is held constant.

4. Summary. The characteristic being measured, $R_{\theta JC}$ or $R_{\theta JA}$ shall be specified in the detail specification.

METHOD 3161

THERMAL IMPEDANCE MEASUREMENTS FOR VERTICAL POWER MOSFET's (DELTA SOURCE-DRAIN VOLTAGE METHOD)

1. Purpose. The purpose of this test method is to measure the thermal impedance of the MOSFET under the specified conditions of applied voltage, current, and pulse duration. The temperature sensitivity of the forward voltage of the source-drain diode is used as the junction temperature indicator. This method is particularly suitable to enhancement mode, power MOSFET's having relatively long thermal response times. This test method may be used to measure the thermal response of the junction to a heating pulse, to ensure proper die mountdown to its case, or the dc thermal resistance, by the proper choice of the pulse duration and magnitude of the heating pulse. The appropriate test conditions and limits are detailed in 5.

1.1 Definitions. The following symbols shall apply for the purpose of this test method:

I_M: Current in the source-drain diode during measurement of the source-drain voltage.

I_H: Heating current through the drain.

V_H: Heating voltage between the drain and source.

P_H: Magnitude of the heating power pulse applied to DUT in watts; the product of I_H and V_H.

t_H: Heating time during which P_H is applied.

VTC: Voltage-temperature coefficient of V_{SD} with respect to T_J; in mV/°C.

K: Thermal calibration factor, equal to reciprocal of VTC; in °C/mV.

T_J: Junction temperature in degrees Celsius.

T_{Ji}: Junction temperature in degrees Celsius before start of the power pulse.

T_{Jf}: Junction temperature in degrees Celsius at the end of the power pulse.

T_X: Reference temperature in degrees Celsius.

T_{Xi}: Initial reference temperature in degrees Celsius.

T_{Xf}: Final reference temperature in degrees Celsius.

V_{SD}: Source-drain diode voltage in millivolts.

V_{SDi}: Initial source-drain voltage in millivolts.

V_{SDf}: Final source-drain voltage in millivolts.

t_{MD}: Measurement delay time is defined as the time from the removal of heating power P_H to the start of the V_{SD} measurement.

t_{SW}: Sample window time during which final V_{SD} measurement is made.

$V_{GS(M)}$: Gate-source voltage applied during the initial and final measurement periods.

$Z_{\theta JX}$: Transient junction-to-reference point thermal impedance in degrees Celsius/watt. $Z_{\theta JX}$ for specified power pulse duration is:

$$Z_{\theta JX} = \frac{(T_{jf} - T_{ji} - \Delta T_X)}{P_H}$$

Where: ΔT_X = Change in reference point temperature during the heating pulse (see 4.2 and 4.4). For short heating pulses, e.g., die attach evaluation, this term is normally negligible.)

2. Apparatus. The apparatus required for this test shall include the following as applicable to the specified test procedure:

a. A thermocouple for measuring the case temperature at a specified reference point. The recommended reference point shall be located on the case under the heat source. Thermocouple material shall be copper-constantan (type T) or equivalent. The wire size shall be no larger than AWG size 30. The junction of the thermocouple shall be welded to form a bead rather than soldered or twisted. The accuracy of the thermocouple and its associated measuring system shall be ±0.5°C. Proper mounting of the thermocouple to ensure intimate contact to the reference point is critical for system accuracy.

b. A controlled temperature environment capable of maintaining the case temperature during the device calibration procedure to within ±1°C over the temperature range of +23°C to +100°C, the recommended temperatures for measuring K factor.

c. A K factor calibration setup, as shown on figure 3161-1, that measures V_{SD} for a specified value of I_M in an environment in which temperature is both controlled and measured. A temperature controlled, circulating fluid bath may be used. The current source must be capable of supplying I_M with an accuracy of ±1 percent. The voltage source must be capable of supplying a stable $V_{GS(M)}$ in the range of -1 to -5 V (opposite polarity for p-channel devices). This voltage is applied in such a way as to turn the DUT off (i.e., gate negative with respect to source for n-channel device). The voltage measurement of V_{SD} shall be made using kelvin contacts and with voltmeters capable of 1 mV resolution. The device-to-current source wire size shall be sufficient to handle the measurement current (AWG size 22 stranded is typically used for up to 100 mA).

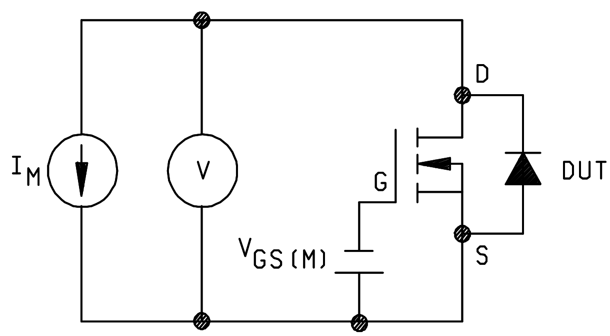
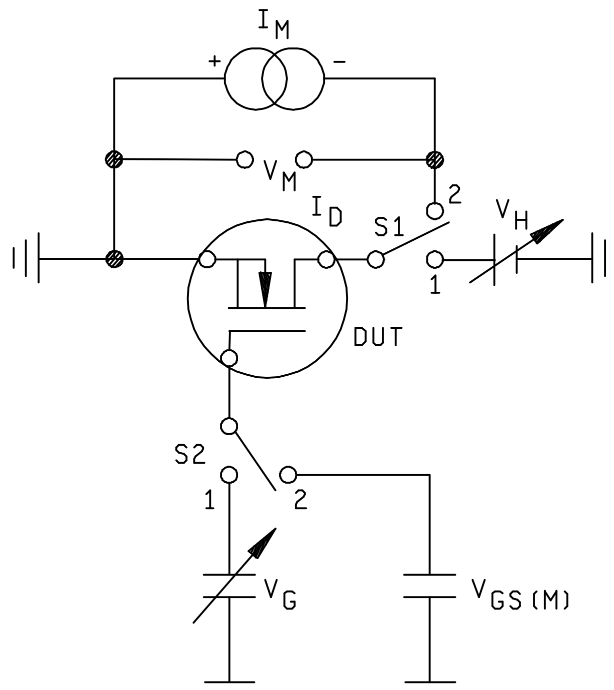


FIGURE 3161-1. K-factor calibration setup.

d. A test circuit used to control the device and to measure the temperature using the forward voltage of the source-drain diode as the temperature sensing parameter as shown on figure 3161-2. Polarities shown are for n-channel devices but the circuit may be used for p-channel types by reversing the polarities of the voltage and current sources.

e. Suitable sample-and-hold voltmeter or oscilloscope to measure source-drain forward voltage at specified times. V_{SD} shall be measured to within 5 mV, or within 5 percent of (V_{SDi} - V_{SDf}), whichever is less.



NOTES:

1. The circuit consists of the DUT, three voltage sources, a current source, and two electronic switches. During the heating phase of the measurement, switches S1 and S2 are in position 1. The values of V_G and V_D are adjusted to achieve the desired values of I_D and V_{DS} for the P_H "heating" condition.
2. To measure the initial and post heating pulse junction temperatures of the DUT, switches S1 and S2 are each switched to position 2. This puts the gate at the measurement voltage level $V_{GS(M)}$ and connects the current source I_M to supply forward measurement current to the source-drain diode. The polarity of the current source is such that the voltage applied to the MOSFET source and drain are opposite to those employed during normal MOSFET operation. Figures 3161-3 and 3161-4 show the waveforms associated with the three segments of the test.

FIGURE 3161-2. Thermal impedance measurement circuit (source-drain diode method).

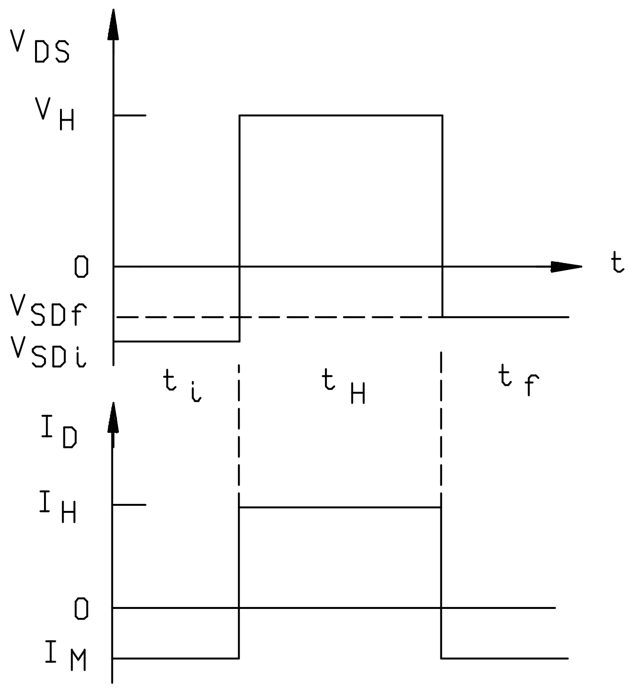


FIGURE 3161-3. Device waveforms during the three segments of the thermal transient test.

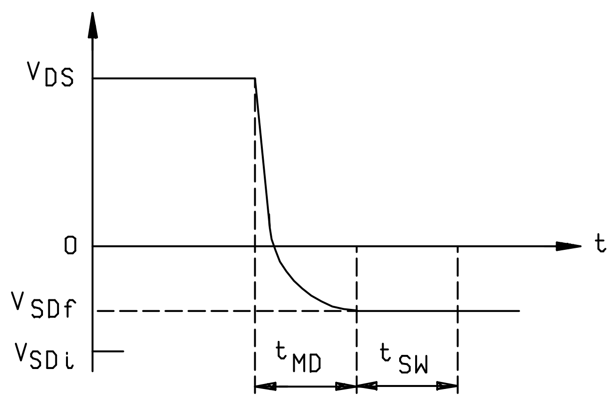


FIGURE 3161-4. Second V_{SD} measurement waveform.

NOTE: The value of t_{MD} is critical to the accuracy of the measurement and must be properly specified in order to ensure measurement repeatability. Note that some test equipment manufacturers include the sample and hold window time t_{SW} within their t_{MD} specification.

3. Measurement of the TSP. The required calibration of V_{SD} versus T_J is accomplished by monitoring V_{SD} for the required value of I_M as the heat sink temperature (and thus the DUT temperature) is varied by external heating. The magnitude of I_M shall be chosen so that V_{SD} is a linearly decreasing function over the expected range of T_J during the power pulse. I_M must be large enough to ensure that the source-drain junction is turned on but not so large as to cause any significant self-heating. (This will normally be 10 mA for small power devices and up to 100 mA for large ones.) The $V_{GS(M)}$ value must be large enough to decouple the gate from controlling the DUT; typical values are in the 1 to 5 V range. An example calibration curve is shown on figure 3161-5.

3.1 Measurement of die attachment integrity. When screening to ensure proper die attachment integrity within a given lot or in a group of same type number devices of one manufacturer, this calibration step is not required. In such cases, the measure of thermal response may be ΔV_{SD} for a short heating pulse, and the computation of ΔT_J or $Z_{\theta JX}$ is not necessary. (For this purpose, t_H shall be 10 ms for TO-39 size packages and 100 ms for TO-3 packages.)

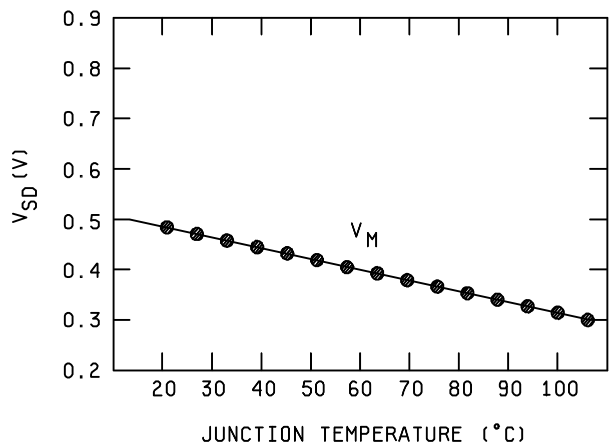


FIGURE 3161-5. Example curve of V_{SD} versus T_J.

3.2 K factor calibration. A K factor calibration (which is the reciprocal of VTC or the slope of the curve on figure 3161-4) can be defined as:

$$K = \frac{1}{VTC} = \left| \frac{T_{J1} - T_{J2}}{V_{SD1} - V_{SD2}} \right| \; °C / mV$$

It has been found experimentally that the K factor variation for all devices within a given device type class is small. The usual procedure is to perform a K factor calibration on a 10 to 12 piece sample from a device lot and determine the average K and standard deviation (σ). If σ is less than or equal to three percent of the average value of K, then the average value of K can be used for all devices within the lot. If σ is greater than three percent of the average value of K, then all the devices in the lot shall be calibrated and the individual values of K shall be used in thermal impedance calculations or in correcting ΔV_{SD} values for comparison purposes.

4. Test procedure.

4.1 Calibration. K factor must be determined according to the procedure outlined in 3., except as noted in 3.1.

4.2 Reference point temperature. The reference point is usually chosen to be on the bottom of the transistor case directly below the semiconductor chip in a TO-204 metal can or in close proximity to the chip in other styles of packages. Reference temperature point location must be specified and its temperature shall be monitored using the thermocouple mentioned in 2.a. during the preliminary testing. If it is ascertained that T_X increases by more than +5°C of measured junction temperature rise during the power pulse, then either the heating power pulse magnitude must be decreased, the DUT must be mounted in a temperature controlled heat sink, or the calculated value of thermal impedance must be corrected to take into account the thermal impedance of the reference point to the cooling medium or heat sink. Temperature measurements for monitoring, controlling, and correcting for reference point temperature changes are not required if the t_H value is low enough to ensure that the heat generated within the DUT has not had time to propagate through the package. Typical values of t_H for this case are in the 10 ms to 500 ms range, depending on DUT package type and material.

4.3 Thermal measurements. The following sequence of tests and measurements must be made:

a. Prior to the power pulse:

(1) Establish reference point temperature (T_{Xi}).

(2) Apply measurement current (I_M).

(3) Apply gate-source measurement voltage ($V_{GS(M)}$).

(4) Measure source-drain voltage drop (V_{SDi}) (a measurement of the initial junction temperature).

b. Heating pulse parameters:

(1) Apply drain-source heating voltage (V_H).

(2) Apply drain heating current (I_H) as required by adjustment of gate-source voltage.

(3) Allow heating condition to exist for the required heating pulse duration (t_H).

(4) Measure reference point temperature (T_{Xf}) at the end of heating pulse duration.

(NOTE: T_X measurements are not required if the t_H value meets the requirements stated in 4.2.)

c. Post power pulse measurements:

(1) Apply measurement current (I_M).

(2) Apply gate-source measurement voltage ($V_{GS(M)}$).

(3) Measurement source-drain voltage drop (V_{SDf}) (a measurement of the final junction temperature).

(4) Time delay between the end of the power pulse and the completion of the V_{SDf} measurement as defined by the waveform of figure 3161-4 in terms of $t_{MD} + t_{SW}$.

4.4 Thermal impedance. The value of thermal impedance ($Z_{\Theta JX}$) is calculated from the following formula:

$$Z_{\theta JX} = \frac{\Delta T_J}{P_H} = \left| \frac{K (V_{SDf} - V_{SDi})}{(I_H)(V_H)} \right| \,^{\circ}C/W$$

This value of thermal impedance will have to be corrected if T_{Xf} is greater than T_{Xi} by +5°C. The correction consists of subtracting out the component of thermal impedance due to the thermal impedance from the reference point (typically the device case) to the cooling medium or heat sink. T_X measurements are not required if the t_H value meets the requirements stated in 4.2. This thermal impedance component has a value calculated as follows:

$$Z_{\theta X\text{-}HS} = \frac{\Delta T_X}{P_H} = \frac{(T_{xf} - T_{xi})}{[(I_H)(V_H)]}$$

Where: HS = cooling medium or heat sink (if used).

Then: $\underbrace{Z_{\theta JX}|}_{\text{Corrected}} = \underbrace{Z_{\theta JX}|}_{\text{Calculated}} - Z_{\theta X\text{-}HS}$

Note: This last step is not necessary for die attach evaluation (see 3.1).

5. Test conditions and measurements to be specified and recorded.

5.1 K factor calibration.

5.1.1 Conditions data. Specify the following test conditions:

a. Measuring current (I_M) (see detail specification).

b. Gate-source voltage ($V_{GS(M)}$) (in the range of 0 V to -6 V).

c. Initial junction temperature (T_J): +25°C ±5°C.

d. Final junction temperature (T_{Jf}): +100°C ±10°C.

5.1.2 Record data. Record the following data:

a. Initial V_{SD} voltage.

b. Final V_{SD} voltage.

5.1.3 Calculation data. Calculate K factor in accordance with the following equation:

$$K = \left| \frac{T_J1 - T_J2}{V_{SD}1 - V_{SD}2} \right| °C / mV$$

5.1.4 Die attach procedure. K factor calibration (see 5.1) may not be necessary for die attachment evaluation (see 3.1).

5.2 Thermal impedance measurements.

5.2.1 Conditions data. Specify the following test conditions in the detail specification.

a. Measuring current (I_M) (must be same as used for K factor calibration).

b. Drain heating current (I_H).

c. Heating time (t_H).

d. Drain-source heating voltage (V_H).

e. Measurement time delay (t_{MD}).

f. Sample window time (t_{SW}).

g. Gate-source voltage ($V_{GS(M)}$) (must be same as used for K factor calibration).

(NOTE: I_H and V_H are usually chosen so that P_H is approximately two-thirds of device rated power dissipation).

5.2.2 Record data. Record the following data:

a. Initial reference temperature (T_{Xi}).

b. Final reference temperature (T_{Xf}).

c. T_X measurements are not required if the t_H value meets the requirements stated in 4.2.

d. Calculate thermal impedance using the procedure and equations shown in 4.4.

5.2.2.1 ΔV_{SD} data. This parameter can either be read directly from suitable test instrumentation or calculated by taking the difference between initial and final values of V_{SD} (i.e., $\Delta V_{SD} = |V_{SD(i)} - V_{SD(f)}|$.)

5.2.3 Thermal resistance measurements. This is a thermal impedance measurement for the condition in which the heating time (t_H) has been applied long enough to ensure that the temperature drop from the device junction to the case reference point in accordance with 2.a. has reached equilibrium and no longer increases for greater values of t_H. In practical measurements, this condition can be assumed to exist when the rate of junction temperature change matches the rate of case temperature change.

5.3 Thermal response ΔV_{DS} measurements for screening. These measurements are made for t_H values that meet the intent of 3.1 and the requirements stated in 4.2.

5.3.1 Conditions data. Specify the following test conditions in the detail specification:

a. Measuring current (I_M).

b. Drain heating current (I_H).

c. Heating time (t_H).

d. Drain-source heating voltage (V_H).

e. Measurement time delay (t_{MD}).

f. Sample window time (t_{SW}).

g. Gate-source voltage ($V_{GS(M)}$) (must be the same as used if and when K factor calibration is performed (see 5.3.2.1b)).

(The values of I_H and V_H are usually chosen equal to or greater than the values used for thermal impedance measurements.)

5.3.2 Specified limits. The following data is compared to the specified limits:

5.3.2.1 ΔV_{SD} data.

a. Same as 5.2.2.1.

b. Optionally calculate ΔT_J for comparison or screening purposes, or both, if the K factor results (see 3. and 5.1) produce a σ greater than three percent of the average value of K.

$$\Delta T_J = K\ (\Delta V_{SD})\ \text{in } ^\circ C$$

6. Summary. The following conditions shall be specified in the detail specification:

6.1 Thermal impedance.

a. I_M measuring current.

b. I_H drain heating current.

c. t_H heating time.

d. V_H drain-source heating voltage.

e. t_{MD} measurement time delay.

f. t_{SW} sample window time.

6.2 Thermal response ΔV_{SD} measurement.

a. I_M measuring current.

b. I_H drain heating current.

c. t_H heating time.

d. V_H drain-source heating voltage.

e. t_{MD} measurement time delay.

f. t_{SW} sample window time.

METHOD 3181

THERMAL RESISTANCE FOR THYRISTORS

1. Purpose. The purpose of this test is to measure the thermal resistance of thyristors under specified conditions.

2. Test circuit. See figure 3181-1.

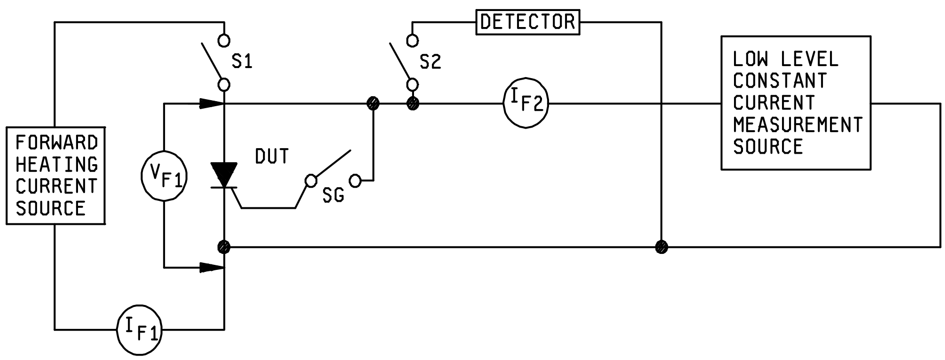


FIGURE 3181-1. Thermal resistance test circuit.

3. Procedure. S1 is closed for a much longer interval (heat) than it is opened (measurement). The measurement interval should be short compared to the thermal response time of the device being measured. The constant measurement current is a small current (of the order of a few milliamperes) and so selected that the magnitude of V_{F1} changes appropriately with the device material (silicon approximately 2 mV/°C) and junction temperature. The heating current source is adjustable.

3.1 Measurement. The measurement is made in the following manner. The case ambient or other reference point is elevated to a high temperature, T_2, not exceeding the maximum junction temperature and the forward voltage drop V_{F1} read with the heating source supplying no current (i.e., the forward voltage V_{F1} is to be read at the start of the measurement interval). An oscilloscope makes a convenient detector. At T_2 there will be a small power dissipated in the device due to the measurement current source. The reference is then reduced to a lower temperature T_1, and power P_1 is applied to heat the device by increasing the current from the constant current source until the same value of V_{F1} is read as was read above. However, if P_1 is calculated as the heating power contributed by the heating current source only the equation:

$$\theta = \frac{T_2 - T_1}{P_1} \text{ gives } \theta \text{ accurately}$$

Where: $P_1 = V_{F1} I_{F1}$

4. Summary. The following conditions shall be specified in the detail specification:

a. Test temperatures (see 3.1).

b. Test voltages and currents (see 3.1).

3200 Series

Low frequency tests

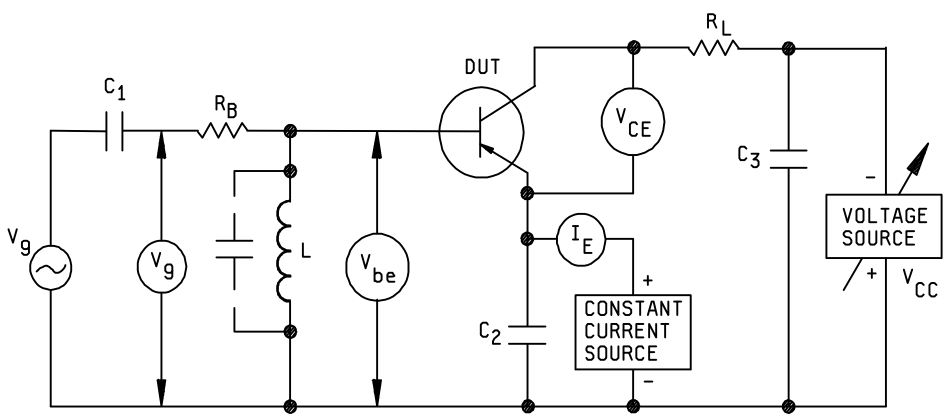
Unless otherwise specified, the measurements shall be made at the electrical test frequency, 1,000 ±25 Hz. At 1,000 Hz, the reactive components may not be negligible.

METHOD 3201.1

SMALL-SIGNAL SHORT-CIRCUIT INPUT IMPEDANCE

1. Purpose. The purpose of this test is to measure the input impedance of the device under the specified conditions.

2. Test circuit. The circuit and procedure shown are for common emitter configuration. For other parameters the circuit and procedure should be changed accordingly.



NOTE: The biasing circuit shown is for purposes of illustration only. Other stable biasing circuits may be used (see 4.3.4).

FIGURE 3201-1. Test circuit for small-signal short-circuit input impedance.

3. Procedure. The capacitors C_1, C_2, and C_3 shall present short-circuits at the test frequency in order to effectively couple and bypass the test signal. The inductance L shall be resonated with a capacitor and the combination shall have a large impedance compared with h_{ie} at the test frequency. R_L shall be a short circuit compared with the output impedance of the device. V_g and V_{be} are measured on high-impedance ac voltmeters after setting the specified values of I_E and V_{CE}.

$$\text{Then: } h_{ie} = \frac{V_{be}}{I_b}, \text{ where } I_b = \frac{V_g - V_{be}}{R_B}$$

4. Summary. The following conditions shall be specified in the detail specification:

a. Test frequency (see 3.).

b. Test voltages and currents (see 3.).

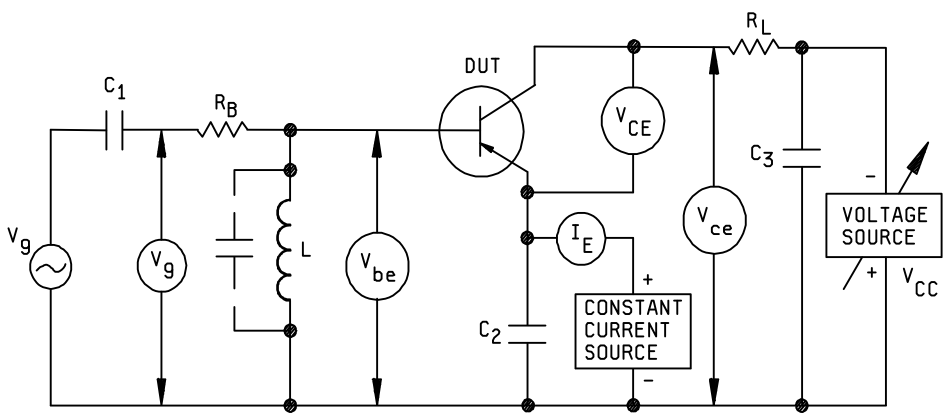
c. Parameter to be measured.

METHOD 3206.1

SMALL-SIGNAL SHORT-CIRCUIT FORWARD-CURRENT TRANSFER RATIO

1. Purpose. The purpose of this test is to measure the forward-current transfer ratio of the device under the specified conditions.

2. Test circuit. The circuit and procedure shown are for common emitter configuration. For other parameters the circuit and procedure should be changed accordingly.



NOTE: The biasing circuit shown is for purposes of illustration only. Other stable biasing circuits may be used (see 4.3.4).

FIGURE 3206-1. Test circuit for small-signal short-circuit forward-current transfer ratio.

3. Procedure. The capacitors C_1, C_2, and C_3 shall present short circuits at the test frequency in order to effectively couple and bypass the test signal. The inductance L shall be resonated with a capacitor and the combination shall have a large impedance compared with h_{ie} at the test frequency. R_L shall be a short circuit compared with the output impedance of the device. V_g, V_{be}, and V_{ce} shall be measured on high-impedance ac voltmeters after setting the specified values of I_E and V_{CE}.

$$\text{Then: } h_{fe} = \frac{I_c}{I_b}, \text{ where: } I_c = \frac{V_{ce}}{R_L} \text{ and } I_b = \frac{V_g - V_{be}}{R_B}$$

4. Summary. The following conditions shall be specified in the detail specification:

a. Test frequency (see 3.).

b. Test voltage and currents (see 3.).

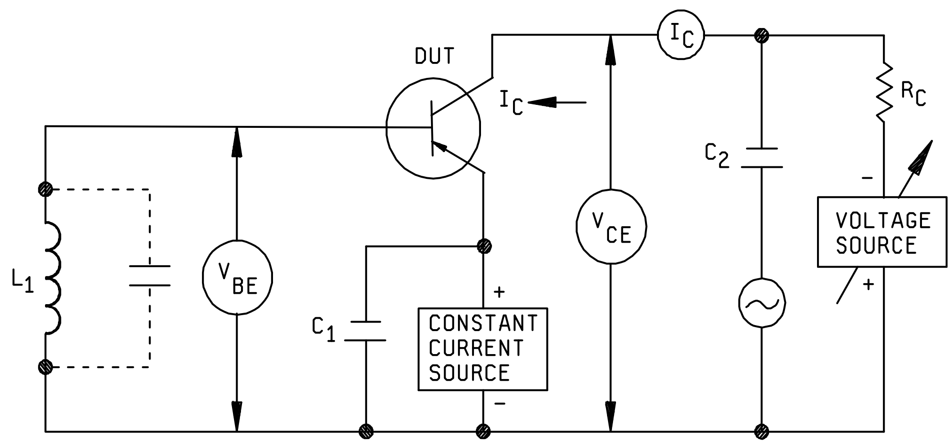
c. Parameter to be measured.

METHOD 3216

SMALL-SIGNAL OPEN-CIRCUIT OUTPUT ADMITTANCE

1. Purpose. The purpose of this test is to measure the output admittance of the device under the specified conditions.

2. Test circuit. The circuit and procedure shown are for common emitter configuration. For other parameters the circuit and procedure should be changed accordingly.



NOTE: The biasing circuit shown is for purposes of illustration only. Other stable biasing circuits may be used (see 4.3.4).

FIGURE 3216-1. Test circuit for small-signal open-circuit output admittance.

3. Procedure. Inductance L_1 shall be resonated with a capacitor and the combination shall have a large impedance compared with h_{ie} at the test frequency. The capacitors C_1 and C_2 shall present short circuits at the test frequency in order to effectively couple and bypass the test signal. Voltmeters V_{be} and V_{ce} shall be high impedance voltmeters. Then:

$$h_{oe} = \frac{I_c}{V_{ce}}$$

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltages and currents (see 3.).

b. Test frequency (see 3.).

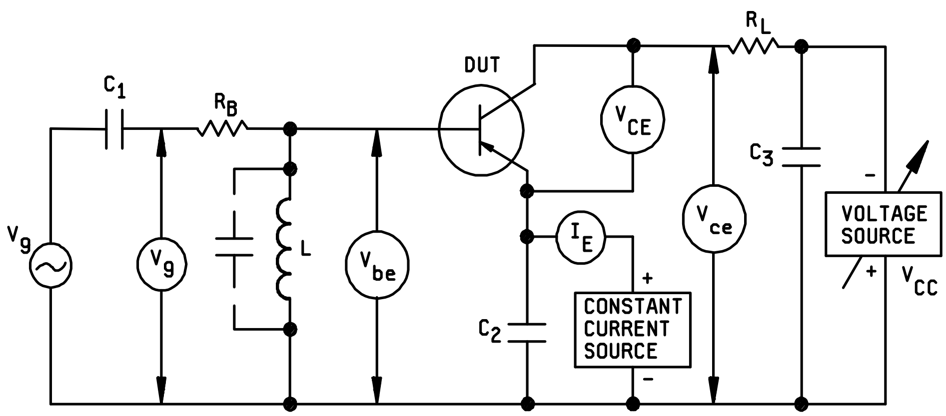
c. Parameter to be measured.

METHOD 3221

SMALL-SIGNAL SHORT-CIRCUIT INPUT ADMITTANCE

1. Purpose. The purpose of this test is to measure the input admittance of the device under the specified conditions.

2. Test circuit. The circuit and procedure shown are for common emitter. For other parameters the circuit and procedure should be changed accordingly.



NOTE: The biasing circuit shown is for purposes of illustration only. Other stable biasing circuits may be used (see 4.3.4).

FIGURE 3221-1. Test circuit for small-signal short-circuit input admittance.

3. Procedure. The capacitors C_1, C_2, and C_3 shall present short circuits at the test frequency in order to effectively couple and bypass the test signal. The inductance L shall be resonated with a capacitor and the combination shall have a large impedance compared with h_{ie} at the test frequency. R_L is optional and shall be a short circuit compared with the output impedance of the device. V_g and V_{be} are measured on high-impedance ac voltmeters.

$$\text{Then: } h_{ie} = \frac{V_{be}}{I_b}$$

$$\text{Thus: } Y_{ie} = \frac{1}{h_{ie}}$$

4. Summary. The following conditions shall be specified in the detail specification:

a. Test frequency (see 3.).

b. Test voltages and currents (see 3.).

c. Parameter to be measured.

METHOD 3231

SMALL-SIGNAL SHORT-CIRCUIT OUTPUT ADMITTANCE

1. Purpose. The purpose of this test is to measure the output admittance of the device under the specified conditions.

2. Test circuit. The circuit and procedure shown are for common emitter configuration. For other parameters the circuit and procedure should be changed accordingly.

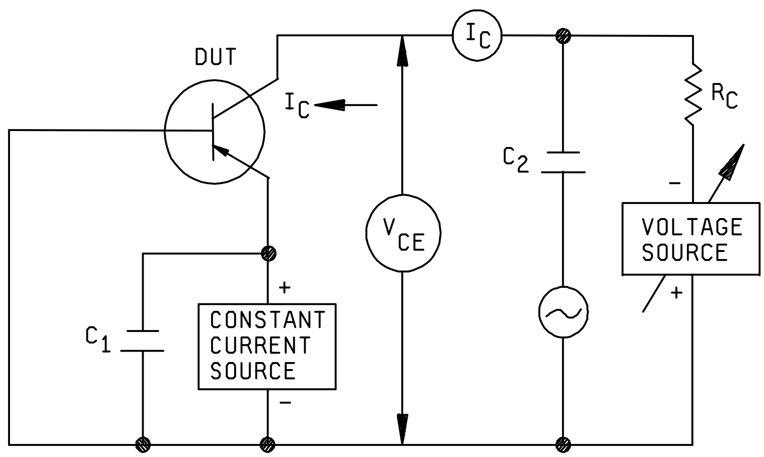


FIGURE 3231-1. Test circuit for small-signal short-circuit output admittance.

3. Procedure. The capacitors C_1 and C_2 shall present short circuits at the test frequency in order to effectively couple and bypass the test signal. Resistor R_C is not zero but chosen for any convenient value.

$$\text{Then: } y_{oe} = \frac{I_c}{V_{ce}}$$

4. Summary. The following conditions shall be specified in the detail specification:

a. Test frequency (see 3.).

b. Test voltages or currents.

c. Parameter to be measured.

METHOD 3236

OPEN CIRCUIT OUTPUT CAPACITANCE

1. Purpose. This test is designed to measure the open circuit output capacitance of the device under the specified conditions.

2. Test circuit. The circuit and procedure shown are for common base configuration. For other parameters the circuit and procedure should be changed accordingly.

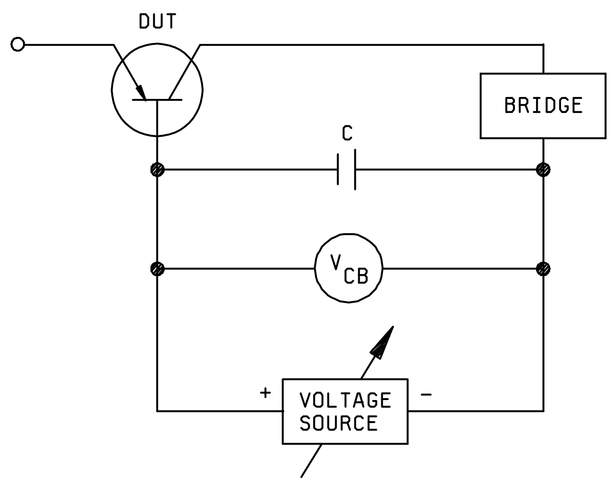


FIGURE 3236-1. Test circuit for open circuit output capacitance.

3. Procedure. The bridge should have low dc resistance between its output terminals and should be capable of carrying the specified collector current without affecting the desired accuracy of measurement. The emitter should be open-circuited to ac and the frequency of measurement shall be as specified. Capacitor C should be sufficiently large to provide a short circuit at the test frequency.

3.1 Measurement. The capacitance reading instrument is nulled with the circuitry connected, thereby eliminating errors due to the stray capacitances of the circuit wiring. The device to be measured is inserted into the test socket, is properly biased, and the output capacitance is measured.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltages or currents (see 3.).

b. Measurement frequency (see 3.).

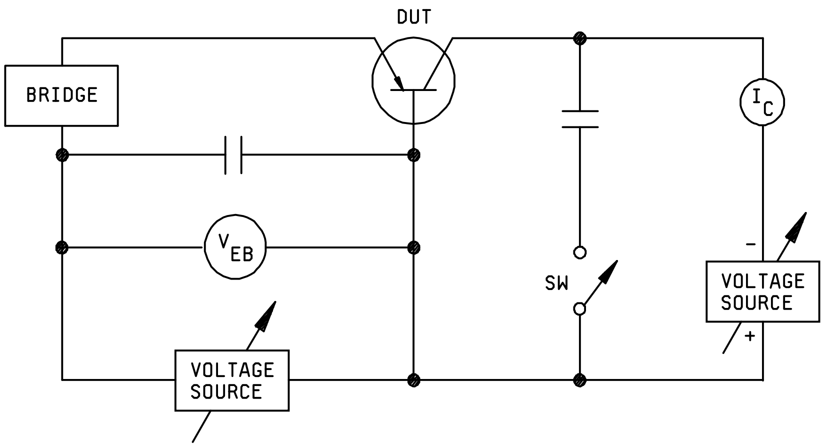
c. Parameter to be measured.

METHOD 3240.1

INPUT CAPACITANCE
(OUTPUT OPEN-CIRCUITED OR SHORT-CIRCUITED)

1. Purpose. The purpose of this test is to measure the shunt capacitance of the input terminals of the device under the specified conditions.

2. Test circuit. See figure 3240-1.



NOTE: For other configurations, the circuit may be modified in such a manner that it is capable of demonstrating device conformance to the minimum requirements of the individual specification.

FIGURE 3240-1. Test circuit for input capacitance (output open-circuited or short-circuited).

3. Procedure. The bridge should have a low dc resistance between the input terminals and should be capable of carrying the required emitter current without effecting the desired accuracy of measurement. The specified voltages or voltage and current shall be applied to the terminals; an ac small signal shall be applied to the input terminals. Switch SW shall be opened or closed depending upon whether the output is intended to be ac open-circuited or ac short-circuited. The input capacitance shall then be measured. The capacitance reading instrument is nulled with the circuitry connected, thereby eliminating errors due to stray capacitances and circuit wiring.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltages or currents (see 3.).

b. Test frequency (see 3.).

c. Whether output is to be open-circuited or short-circuited.

METHOD 3241

DIRECT INTERTERMINAL CAPACITANCE

1. Purpose. The purpose of this test is to measure the direct interterminal capacitance between specified terminals using specified electrical biases.

2. Apparatus. A direct capacitance bridge or resonance method may be used to determine the value of the direct interterminal capacitance.

3. Procedure. The direct interterminal capacitance can be determined by using method A or method B.

3.1 Method A. The specified voltage shall be applied between specified terminals: an ac small signal shall be applied to the terminals and the direct interterminal capacitance shall be measured. The lead capacitance beyond .5 inch (12.70 mm) from the body seat shall be effectively eliminated by suitable means such as test socket shielding. The abbreviations and symbols used are defined as follows:

C_{cb}(dir): Collector to base interterminal direct capacitance.

C_{eb}(dir): Emitter to base interterminal direct capacitance.

C_{ce}(dir): Collector to emitter interterminal direct capacitance.

3.2 Method B. A suitable resonance method can be utilized to measure the following two-terminal capacitances:

C_1: Capacitance between collector terminal and ground, with base and emitter terminals grounded.

C_2: Capacitance between the base terminal and ground, with collector and emitter terminals grounded.

C_3: Capacitance between the collector and base terminals strapped together and ground, with the emitter terminal grounded.

The direct interterminal capacitance can then be calculated from the following relationship:

$$C_{cb}(dir) = \frac{C_1 + C_2 - C_3}{2}$$

The direct interterminal capacitance for other configurations can be determined by suitable modifications of the above procedure. Such modifications shall be capable of demonstrating device conformance to the minimum requirements of the individual specification.

4. Summary. The following conditions shall be specified in the detail specification:

a. Terminal arrangement.

b. DC biasing conditions.

c. Test voltage or current.

d. Measurement frequency.

METHOD 3246.1

NOISE FIGURE

1. Purpose. The purpose of this test is to measure the noise figure of the device under the specified conditions.

2. Apparatus. An average responding rms calibrated indicator shall be used in addition to other suitable apparatus to measure the noise figure of the diode.

3. Procedure. The voltage and current specified in the individual specification shall be applied to the terminals, and the noise figure shall then be measured at the frequency specified in the individual specification (normally 1,000 Hz) with an input resistance of 1,000 A and as referred to a 1 Hz bandwidth.

4. Summary. The following conditions shall be specified in the detail specification:

   a. Test voltage or current.

   b. Test frequency.

   c. Load resistance.

METHOD 3251.1

PULSE RESPONSE

1. Purpose. The purpose of this test is to measure the pulse response (t_d, t_r, t_s, and t_f) of the device under the specified conditions.

2. Test circuit. See figures 3251-1 and 3251-2.

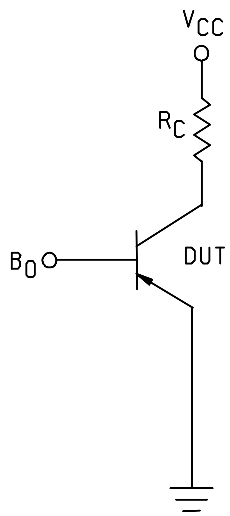


FIGURE 3251-1. Test circuit for pulse response, test condition A.

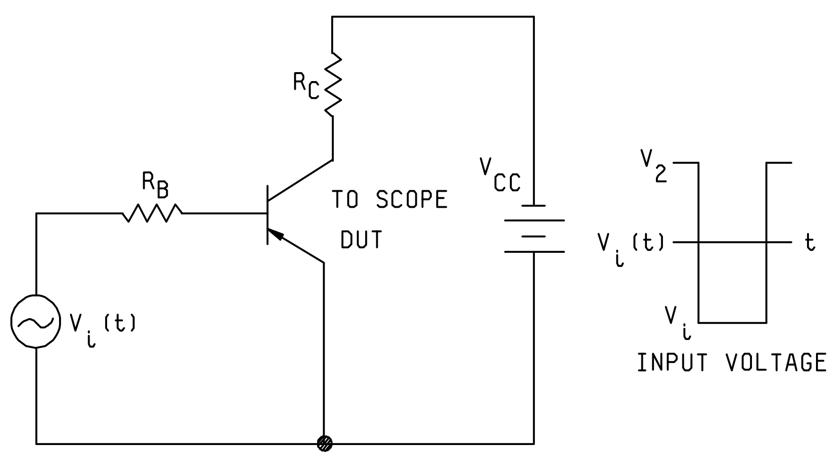


FIGURE 3251-2. Test circuit for pulse response, test condition B.

3. Procedure. The pulse response of the device shall be measured using test condition A or B.

3.1 Test condition A. The device shall be operated in the common emitter configuration as shown on figure 3251-1 with the collector load resistance (R_C) and collector supply voltage (V_{CC}) specified. When measuring delay or rise time, $I_{B(0)}$ and $I_{B(1)}$ or $V_{BE(1)}$ shall be specified. When measuring storage or fall time, $I_{B(1)}$ or $V_{BE(1)}$ and $I_{B(2)}$ or $V_{BE(2)}$ shall be specified. The input transition and the collector voltage response detector shall have rise and response fall times such that doubling these responses will not affect the results greater than the precision of measurement. The current and voltages specified shall be constant. Stray capacitance of the circuit shall be sufficiently small so that doubling it does not affect the test results greater than the precision of measurement.

$I_{B(0)}$ = prior off state base current.

$V_{BE(0)}$ = prior off state base to emitter voltage.

$I_{B(1)}$ = on state base current.

$V_{BE(1)}$ = on state base to emitter voltage.

$I_{B(2)}$ = post off state base current.

$V_{BE(2)}$ = post off state base to emitter voltage.

3.2 Test condition B. The device shall be operated in the test circuit shown on figure 3251-2 (constant current drive) with the voltages and component values as specified. The pulse or square-wave generator and scope shall have rise and fall response times such that doubling these responses will not affect the results greater than the precision of measurement.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test condition (A or B).

b. Collector load resistance (R_C) and collector supply voltage (V_{CC}) for A.

c. Base resistance (R_B) collector load resistance (R_C), and collector supply voltage (V_{CC}) for B.

d. Test voltages or currents (see 3.).

METHOD 3255

LARGE SIGNAL POWER GAIN

1. Purpose. The purpose of this test is to measure the ratio of ac output power to the ac input power (usually specified in dB) under specified large signal conditions.

2. Test circuit. The test circuit shall be as specified in the detail specification.

3. Procedure. The procedure shall be as specified in the detail specification.

4. Summary. The following conditions shall be specified in the detail specification.

a. Test voltages and currents.

b. Test frequency (if other than 1,000 Hz).

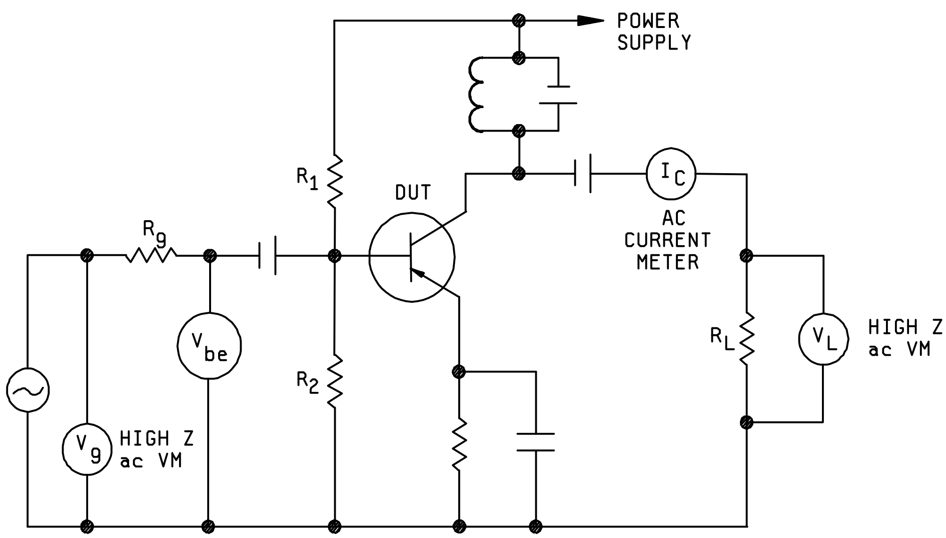
c. Test circuit.

METHOD 3256

SMALL SIGNAL POWER GAIN

1. Purpose. The purpose of this test is to measure the ratio of the ac output power to the ac input power under the specified conditions (usually specified in dB) for small signal power gain.

2. Test circuit. See figure 3256-1.



NOTE: For other configurations, the circuit should be modified in such a manner that the circuit is capable of demonstrating device conformance to the individual specification.

FIGURE 3256-1. Test circuit for small-signal power gain.

3. Procedure. The specified voltage(s) and current(s) should be applied to the terminals; an ac small signal should be applied to the input terminals of the specified circuit. The resistors R_1 and R_2 should have values larger than the h_{ie} of the device. The phase angle 1 between the input current and V_{be} shall be considered to be 0, if the specified test frequency is less than the extrapolated unity gain frequency (f_t) of the device.

Then, for common emitter:

$$P_{ge} = 10 \log \frac{P_{out}}{P_{in}}$$

$$Where,\ P_{in} = (V_{be})(i_b) \cos \theta$$

$$i_b = \frac{V_g - V_{be}}{R_g}$$

$$P_{out} = (i_c)^2 (R_L) \text{ or } \frac{(V_L^{\,2})}{R_L}$$

$$\text{Thus,} \quad P_{ge} = 10 \log \frac{(i_c)^2 \; (R_L)}{(V_{be}) \left(\dfrac{V_g - V_{be}}{R_g} \right)} \quad \text{or}$$

$$10 \log \frac{\dfrac{V_L^{\,2}}{R_L}}{V_{be} \left(\dfrac{V_g - V_{be}}{R_g} \right)}$$

For other configurations, modifications to the procedure should be made in such a manner that it is capable of demonstrating device conformance to the individual specification.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test circuit.

b. Test voltage(s) and current(s).

c. Test frequency (if other than 1,000 Hz).

METHOD 3261.1

EXTRAPOLATED UNITY GAIN FREQUENCY

1. Purpose. The purpose of this test is to determine the extrapolated unity gain frequency (gain band width product) of the device under the specified conditions.

2. Test circuit. The test circuit employed in determining the extrapolated unity gain frequency shall be that which is used for measuring the magnitude of the common emitter small-signal short-circuit current transfer ratio. (See method 3306.)

3. Procedure. The magnitude of the common emitter short-circuit current transfer ratio shall be determined at the specified frequency with the specified bias voltages and currents applied. The product of the specified signal frequency (f) and the measured common emitter small-signal short-circuit current transfer ratio (h_{fe}) is the extrapolated unity gain frequency (f_t).

4. Summary. The following conditions shall be specified in the detail specification:

a. Test current and voltage.

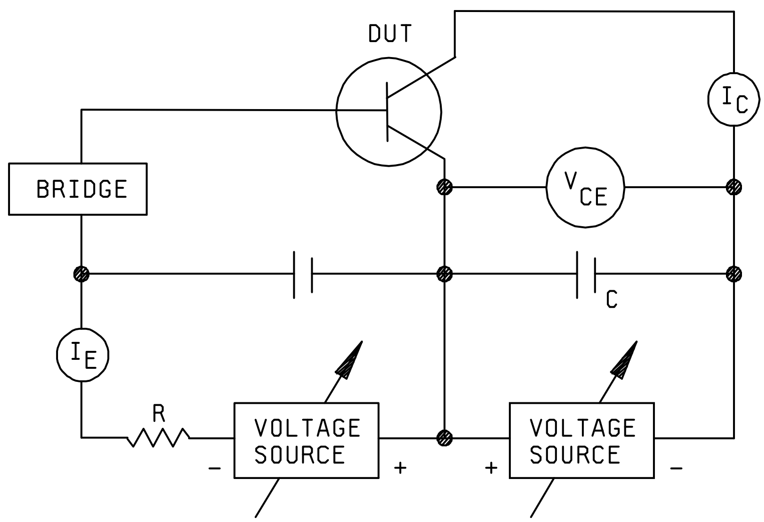
b. Test frequency.

METHOD 3266

REAL PART OF SMALL-SIGNAL SHORT-CIRCUIT INPUT IMPEDANCE

1. Purpose. The purpose of this test is to measure the resistive component of the small signal short-circuit input impedance of the device under the specified conditions.

2. Test circuit. See figure 3266-1.



NOTE: The circuit shown is used for measuring the common emitter real part of the small-signal short-circuit input impedance. For other device configurations, the above circuitry should be modified in such a manner that it is capable of demonstrating device conformance to the minimum requirements of the individual specification.

FIGURE 3166-1. Test circuit for real part of small-signal short-circuit input impedance.

3. Procedure. The voltage and current specified shall be applied to the terminals. An ac small signal of the frequency specified shall be applied to the input terminals and the output terminals shall be ac short-circuited. The real part of the input impedance shall then be measured.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltage and current.

b. Test frequency.

3300 Series

High frequency tests

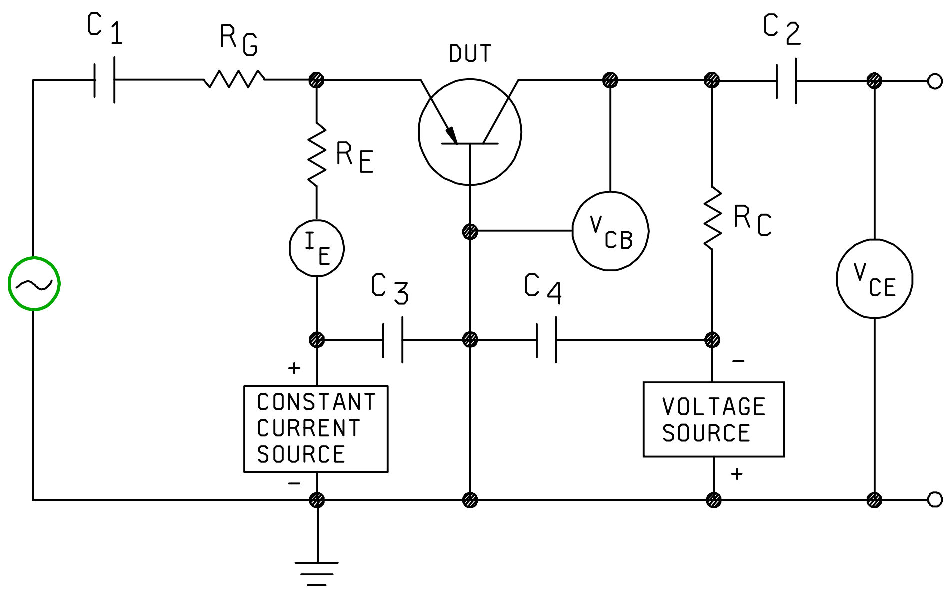
Care shall be taken that, in designing the circuit and transistor mounting, adequate shielding and decoupling are provided and that series inductances in circuits are negligible.

METHOD 3301

SMALL-SIGNAL SHORT-CIRCUIT FORWARD-CURRENT TRANSFER-RATIO CUTOFF FREQUENCY

1. Purpose. The purpose of this test is to measure the forward-current transfer-ratio cutoff frequency under the specified conditions.

2. Test circuit. The circuit and procedure shown are for common base configuration. For other parameters the circuit and procedure should be changed accordingly.



NOTE: Normal VHF circuit precautions should be taken. At frequencies higher than 10 MHz, the use of this circuit may lead to excessive errors. The biasing circuit shown is for the purposes of illustration only and any stable biasing circuit may be used.

FIGURE 3301-1. Test circuit for small-signal short-circuit forward-current transfer-ratio cutoff frequency.

3. Procedure. The voltages and currents shall be as specified. Resistors R_G and R_E shall be large to present open circuits to h_{ib}. Resistor R_C shall be small to present a short circuit to h_{ob}. Capacitors C_1, C_2, C_3, and C_4 shall present short circuits at the test frequency to effectively couple and bypass the test signal.

a. The circuitry shall be frequency independent. This can be checked by removing the device from the circuit and shorting between emitter and collector with no bias voltages applied. Care should be taken to ensure that the generator has a sufficiently pure waveform and that the high-impedance voltmeter is adequately sensitive to enable the measurement to be made at a low enough signal level to avoid the introduction of harmonics by the device.

b. The generator is set to a frequency at least 30 times lower than the lowest cutoff frequency limit and the low frequency h_{fb} is measured. The frequency is then increased until the magnitude of h_{fb} has fallen to $1/\sqrt{2}$ of its low frequency value. This is the cutoff frequency.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltages and currents (see 3.).

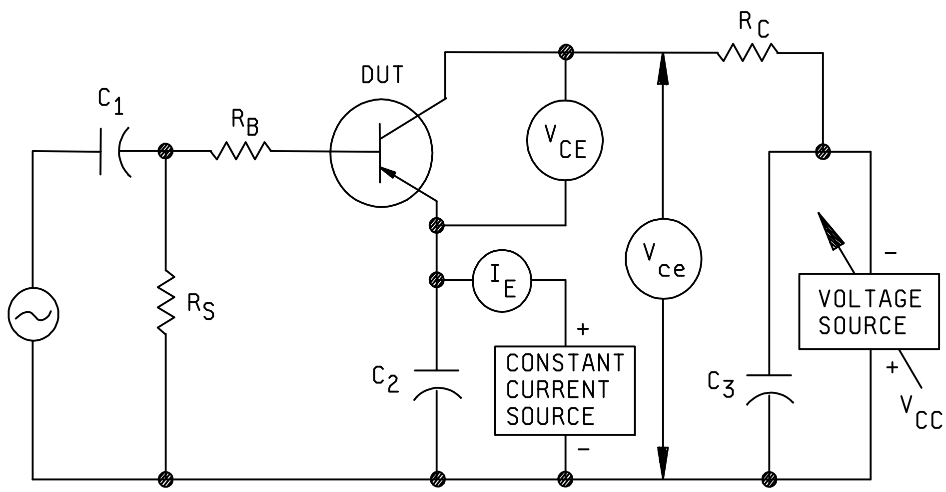
b. Parameter to be measured.

METHOD 3306.4

SMALL-SIGNAL SHORT-CIRCUIT FORWARD-CURRENT TRANSFER RATIO

1. Purpose. The purpose of this test is to measure the forward-current transfer ratio under the specified conditions.

2. Test circuit. The circuit (see figure 3306-1) and procedure shown are for common emitter configuration. For other parameters the circuit and procedure should be changed accordingly.



* NOTE: The biasing circuit shown is for purpose of illustration only. Other stable biasing circuits may be used.

FIGURE 3306-1. Test circuit for small-signal short-circuit forward-current transfer ratio.

* 3. Procedure. Capacitors C_1, C_2, and C_3 shall present short circuits in order to effectively couple and bypass the test signal at the frequency of measurement. The value of R_B shall be sufficiently large to provide a constant current source. Resistor R_C shall be a short circuit compared to the output impedance of the device. With the device removed from the circuit, a shorting link is placed between the base and collector and the output voltage of the signal generator is adjusted until a reading of one (in arbitrary units) is obtained on the high-impedance ac voltmeter, V_{ce}. With the device in the circuit and biased as specified, the reading on voltmeter V_{CE} is now equal to the magnitude of (h_{fe}). (NOTE: Care must be taken to assure that the output signal is not clipped.)

* 4. Summary. The following conditions shall be specified in the performance specification:

a. Measurement frequency.

b. Test voltages and currents.

c. Parameter to be measured.

METHOD 3311

MAXIMUM FREQUENCY OF OSCILLATION

1. Purpose. The purpose of this test is to measure the maximum frequency of oscillation for the device under the specified conditions.

2. Test circuit. The circuit utilized for the maximum frequency of oscillation test shall be as specified in the detail specification.

3. Procedure. The voltage(s) and current(s) specified shall be applied to the device in the circuit specified, and the circuit resonant frequency shall be increased until oscillation ceases. The frequency at which oscillation ceases is the maximum frequency of oscillation.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test circuit.

b. Test voltage(s) and current(s).

METHOD 3320

RF POWER OUTPUT, RF POWER GAIN, AND COLLECTOR EFFICIENCY

TEST CONDITION A

1. Purpose. The purpose of this test is to measure the RF power output, RF power gain, and collector efficiency of a transistor under actual operating conditions in a specific RF amplifier test circuit. Test condition A shall be valid for devices operating at RF power levels greater than 10 dBm when tested in the frequency range between 10 MHz and 2 GHz.

2 Apparatus. All referenced equipment may be replaced by equivalents suitable for the frequency of test. The equipment set up shall be as shown on figures 3320-1 and 3320-2.

3. Procedure. The test fixture shall be disconnected and directional couplers number 1 and number 2 shall be directly connected using a minimum number of connectors. The RF switch shall be set to the output position 'C' and the frequency and RF power source adjusted to the specific conditions by monitoring the frequency counter and RF power meter respectively. The RF switch shall be set to position 'A' and the variable attenuator adjusted to obtain the identical reading as power out in position 'C'. The test fixture shall be reconnected with the DUT inserted and the dc power supply adjusted to the specified voltage. The circuit output tuning shall be adjusted for maximum power gain and circuit input tuning for minimum reflected power. (The RF switch shall be alternated between power in, reflected power, and power out while tuning and this procedure shall be repeated as many times as necessary to obtain minimum reflected power and maximum power out.) The power in level shall be checked before taking the final measurement. If input reflected power calibration is required, the above procedure shall be repeated with directional coupler number 1 reversed and switch position 'A' changed to switch position 'B'.

NOTE: Minimum reflected power is defined as minimum reading obtained with switch in position 'B' and maintaining power in.

3.1 Measurements.

3.1.1 Power output. Power output (P_{out}) is measured by adjusting the RF power source to obtain the specified forward input power and reading the output power in watts.

3.1.2 Power input. Power input (P_{in}) is measured by adjusting the RF power source to obtain the specified forward output power and reading the input power in watts.

3.1.3 Power gain. Power gain (G_p) is measured by adjusting the RF power source to the value of P_{in} which produces the specified P_{out}. P_{in} and P_{out} shall be observed and the gain (in dB) determined as follows:

$$G_P = 10 \log \frac{P_{out}}{P_{in}}$$

3.1.4 Collector efficiency. Collector efficiency (O) is measured by adjusting the RF source to the specified P_{in} (or P_{out}) and reading P_{out}. The collector efficiency shall be computed as follows:

$$\eta (\%) = \frac{P_{out}\ (W)}{P_{in}\ (W)} X\ 100 = \frac{P_{out}\ (W)}{I_C\ X\ V_{CC}} X\ 100$$

Where: I_C = collector current

V_{CC} = collector supply voltage

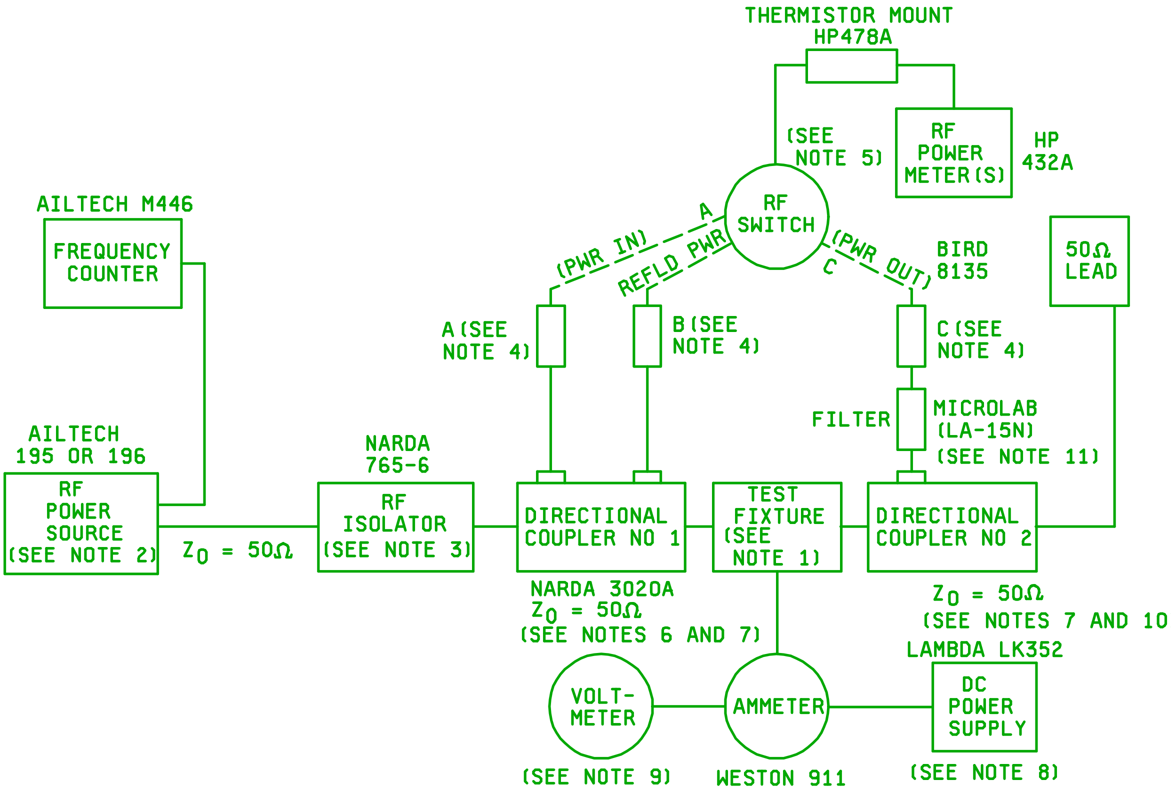


FIGURE 3320-1. Test equipment set-up.

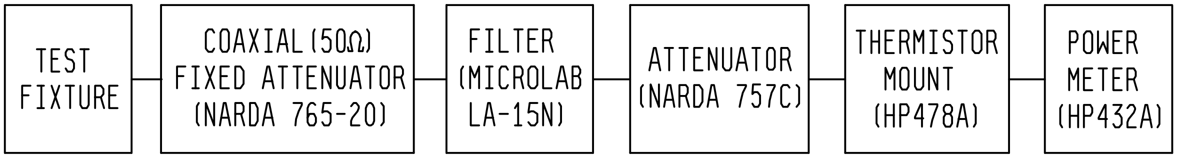


FIGURE 3320-2. Alternate test equipment set-up.

NOTES:

1. Test fixture is the circuit as described in the applicable detail specification (circuit layout and components quality are critical).

2. RF power source shall be a unit capable of generating desired power level at desired frequency with a harmonic and spurious content ≥ 20 dB below operating frequency level of 100 MHz to 1 GHz.

3. The RF isolator shall be a device (e.g., pad, circulator) capable of establishing ≥ 20 dB of isolation between RF power source and test fixture. (A resistive attenuator shall be used for out-of-band isolation.)

FIGURE 3320-2. Alternate test equipment set-up - Continued.

4. Variable attenuators (or fixed, if calibrated): Attenuators are set so that the actual power into and out of test fixture are known. Attenuation on directional coupler number 2 shall be calibrated against a known working standard either by means of a calibration chart or suitable adjustment if variable. Attenuation at position 'A' of directional coupler number 1 shall be calibrated or adjusted so that actual power at test fixture is known. Attenuation at position 'B' shall be adjusted to establish sensitivity needed to measure Reflected power (normally 10 dB less than the attenuation at position 'A').

5. RF switch may be eliminated if additional power meters are used.

6. More than one directional coupler may be used in place of coupler number 1. If more than one coupler is used, the Power In and Reflected power position may be interchanged.

7. The directional couplers shall have a minimum directivity of 30 dB and a nominal 20 dB coupling attenuation except where test level sensitivities require 10 dB or less attenuation.

8. The dc power supply shall be RF decoupled at the test fixture.

9. Voltmeter readings shall be sensed at test fixture, not at power supply.

10. Coupler number 2 and 50 Ω load may be replaced by coaxial fixed attenuators (Narda) and a power meter (HP 432A). Power meter may be separate or connected to the one shown on the other side through port C of the RF switch (see figure 3320-2).

11. If harmonic or subharmonic contents less than 20 dB down from the desired signal are present and could influence the measured output power, a suitable filter (low pass, band pass, or high pass) shall be employed between the attenuator(s) and power meter used for output power measurement.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltage (and current, if applicable).

b. Test frequency.

c. Power input (or output).

d. Test circuit with critical parts and layout specified.

e. Parameter to be measured.

TEST CONDITION B

1. Purpose. The purpose of this test is to measure the RF power output, RF power gain, and collector efficiency of a transistor under actual operating conditions in a specific RF amplifier test circuit. Test condition B shall be valid for devices operating at RF power levels greater than 0 dBm when tested in the frequency range between 100 MHz and 10 GHz.

2. Apparatus. All referenced equipment may be replaced by equipment of equal or superior capability. A typical equipment setup is as follows (see figure 3320-3). All components shall be suitable for the frequency range of measurement.

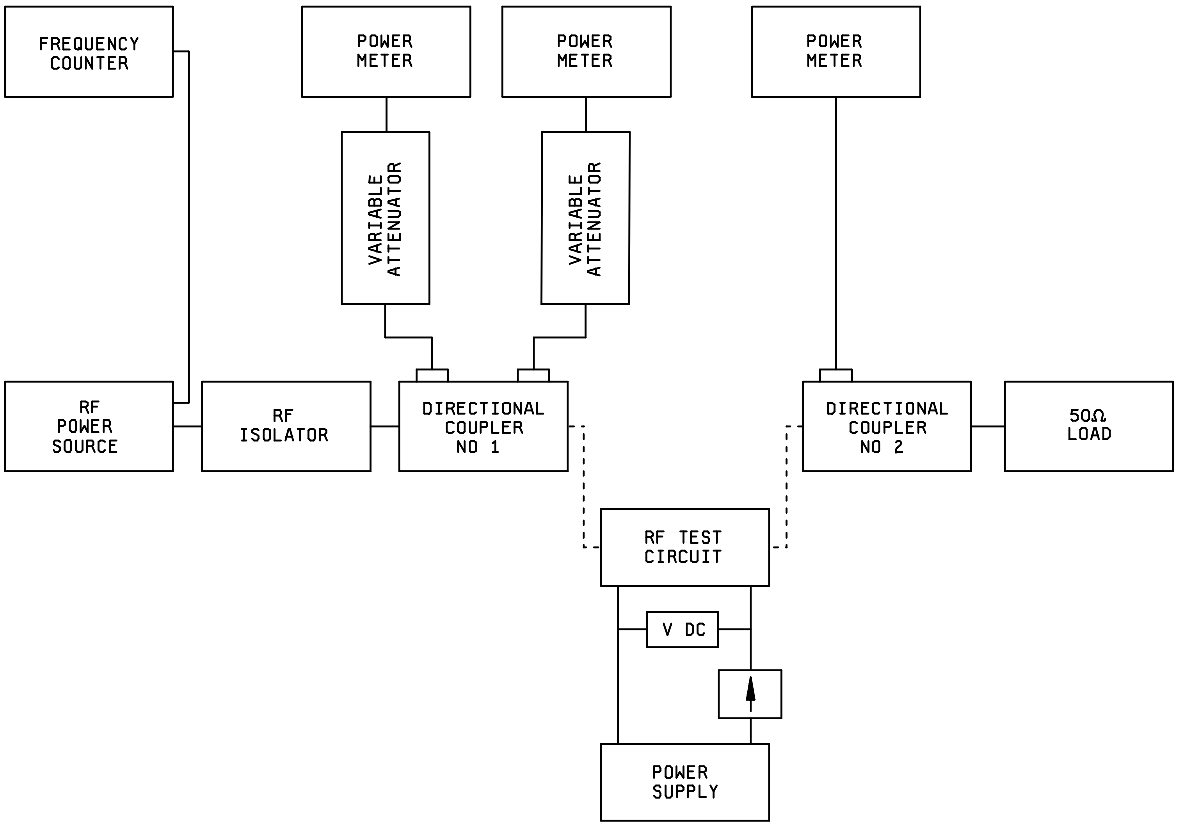


FIGURE 3320-3. RF test set-up.

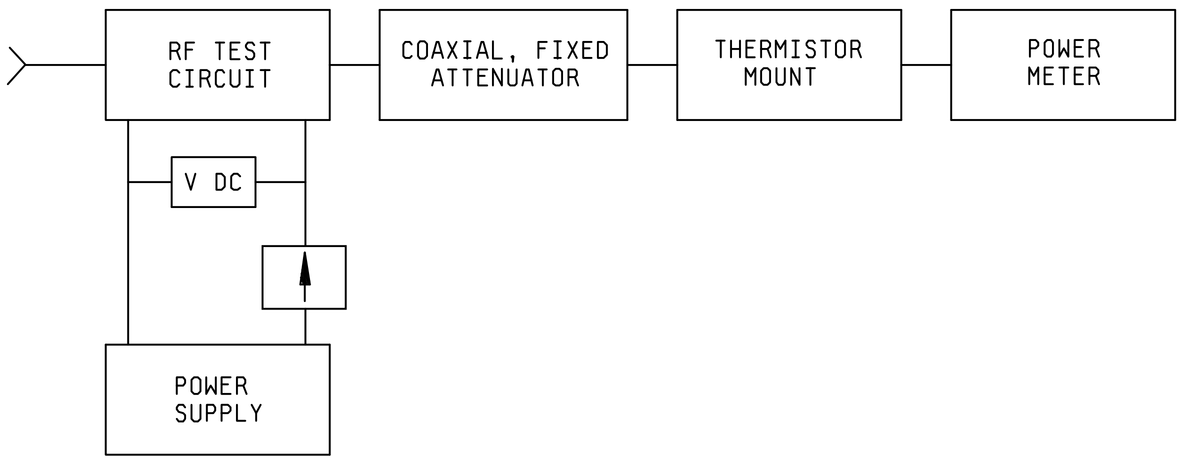
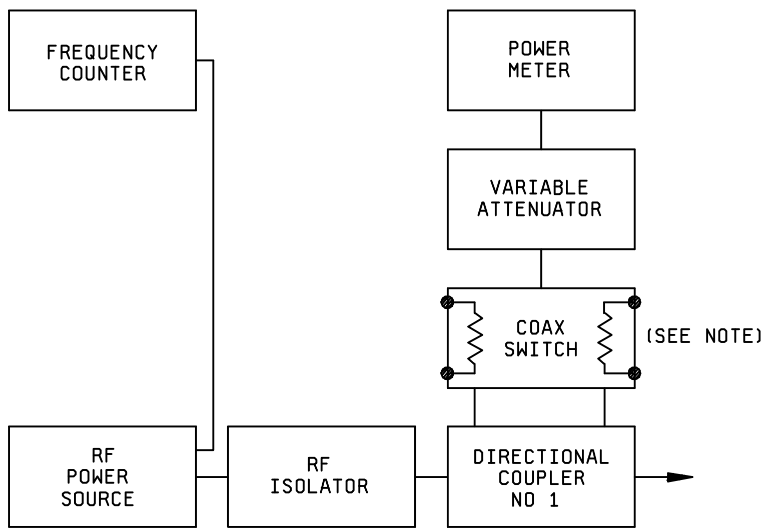


FIGURE 3320-4. Alternate output set-up.



NOTE: The unswitched port automatically terminates the alternate coupler port in 50 Ω when using the coax switch specified in the equipment list.

FIGURE 3320-5. Alternate input set-up.

NOTES:

1. The test fixture referred to in this document is the circuit which is described in the applicable detailed specification (circuit layout and component quality are critical).

2. The RF power source shall be a unit capable of generating desired power levels at the frequency of interest. All harmonics and spurious content shall be at least 26 dB below the output level. When necessary, a suitable filter (low pass or band pass) should be used between the RF source and the isolator to reduce the second harmonic. A similar filter should be used in the output circuit between the coupler and the power meter unless the harmonic levels of the DUT are less than 26 dB below the measurement level. If the filter is to be used, its insertion loss should be calibrated and accounted for at the measurement frequency.

3. Coupler number 2 and the 50 Ω load may be replaced by a coaxial fixed attenuator and a power meter (see figure 3320-4). If employed, the output low pass filter should be placed between the attenuator and power meter.

4. The two power meters connected to coupler number 1 may be replaced by one power meter and a good quality coaxial transfer switch. (The use of such switches is discouraged at frequencies above 4 GHz unless precautions are taken to account for RF losses (see figure 3320-5).) These switches are designed for use in 50 systems. The unswitched port is automatically terminated internally with 50 Ω and loads the alternate coupler port.

5. The RF isolator shall be a device (e.g., pad, circulator) capable of establishing ≥ 20 dB of isolation between RF power source and test fixture.

6. The directional couplers shall have a minimum directivity of 30 dB and a nominal 20 dB coupling attenuation except where test level sensitivities require 10 dB or less attenuation. (Greater accuracy results from using the highest coupling possible, consistent with the measurement.)

7. The dc power supply shall be RF decoupled at the test fixture.

8. Voltmeter readings shall be sensed at the test fixture, not at power supply.

9. A calibrated wavemeter may be used in lieu of the frequency counter specified on figure 3320-3.

1.2 Equipment list. (All referenced equipment may be replaced by equipment of equal or superior quality.)

Equipment	Manufacturer	Model
CW source	As desired	1/
Isolator	Addington Labs	1/
Dual directional coupler	NARDA	3022*
Variable attenuator	Merrimac	Au-25A5
Average power meter	Hewlett-Packard	432 A
Coax switch	Hewlett-Packard	33311 B/C
Fixed attenuator	NARDA	766-20
L.P. filter	Microlab FXR	1/
Power supply	Hewlett-Packard	6296 A
RF test fixture	(See individual specification)	
Voltmeter	Meter-mod Instruments	420 R
Ammeter	Meter-mod Instruments	420 R

2. Test procedure.

2.1 RF setup calibration procedure.

a. With the RF test setup as on figure 3320-3 and with the test fixture removed, hook up the output of coupler number 1 to the input of coupler number 2 (attenuation of directional coupler number 2 shall be calibrated against a known working standard either by means of calibration chart or suitable adjustment if variable).

b. Set the frequency of the source as indicated by the readout of the frequency counter or a dip in the power level when using an in-line wavemeter.

c. Adjust the variable attenuator on the source by decreasing the attenuator until the desired power level is observed on the output power meter (apply correction factor if necessary to correct for coupler number 2 or output attenuator error).

d. Observe the input power meter, and adjust the attenuator associated with this meter until it reads the same power output as the output power meter in 6.1c. (If using the alternate input setup on figure 3320-5, calibrate with coaxial switch in the forward position.)

e. Disconnect the output coupler and power meter from the circuit so that the output of coupler number 1 is open circuited. Adjust the attenuator associated with the reflected power meter until it reads the same as the forward meter. With a calibrated short on the input of the coupler observe the difference in reflected power between an open circuit condition and a short. Adjust the reflected power variable attenuator for an average between the open and short circuit readings. (If using the alternate input setup on figure 3320-5, the reflected power port is automatically calibrated when the forward power is calibrated if both ports of the coupler are balanced.)

1/ Model depends on frequency of test: See manufacturer's catalog for correct model number.

f. Increase the input attenuator until power output is zero (calibration completed).

g. If multiple frequency testing is required repeat 6.1a through 6.1f for each frequency, noting the variable attenuator and power source settings for each specified frequency. All equipment must be returned to the noted settings during test at each specified frequency point.

2.2 RF testing.

a. Make certain the dc power supply is off.

b. With the RF test setup on figure 3320-3 or with alternate circuits of figures 3320-4 and 3320-5, and with the test fixture in place, clamp a device in the test fixture.

c. Switch on the dc power supply. Precautions should be observed to prevent voltages exceeding the specified test level.

d. Adjust the attenuator at the source until the input power reads the appropriate power.

e. Observe the output power, reflected power, and collector current (record, if necessary).

f. Increase the attenuator at the source until the input power reads zero.

g. Repeat 6.2a through 6.2f as required with the previously noted power source and attenuator settings if other test frequencies are required.

h. Switch off the dc power supply.

i. Remove the device from the test fixture.

3. Data required (measurements).

a. Power output (P_{out}) is measured by adjusting the RF power source as outlined in 6.2 to obtain the specified forward input power and reading the output power in watts.

b. Power input (P_{in}) is measured by adjusting the RF power source to obtain the specified forward output power and reading the input power in watts.

c. Power gain (Gp) is calculated from the measured RF data. P_{in} and P_{out} shall be observed and the gain (in dB) determined as follows:

$$G_p = 10 \log \frac{P_{out}}{P_{in}}$$

d. Collector efficiency (η) is calculated from the measured RF and dc data. The collector efficiency shall be computed as follows:

$$\eta\,(\%) = \frac{P_{out}\ (W)}{P_{in}\ (dc - w)}\ X\ 100 = \frac{P_{out}\ (W)}{I_C\ X\ V_{CC}}\ X\ 100$$

Where: I_C = Collector current

V_{CC} = Collector supply voltage

e. Reflected power may be observed directly from the power meter if the setup is calibrated as specified in 6.1e. Even though reflected power may not be part of the RF specifications, it is included here because it is an indication as to how much of the input is actually reaching the device. Good practice dictates that, where possible, the external circuit should be adjusted from minimum reflected power.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltage (and current if applicable).

b. Test frequency.

c. Power input or power output.

d. Test circuit with critical parts and layout specified.

e. Parameter(s) to be measured.

f. Parameter(s) to be calculated.

g. RF test fixture.

3400 Series

Electrical characteristics tests for MOS field-effect transistors

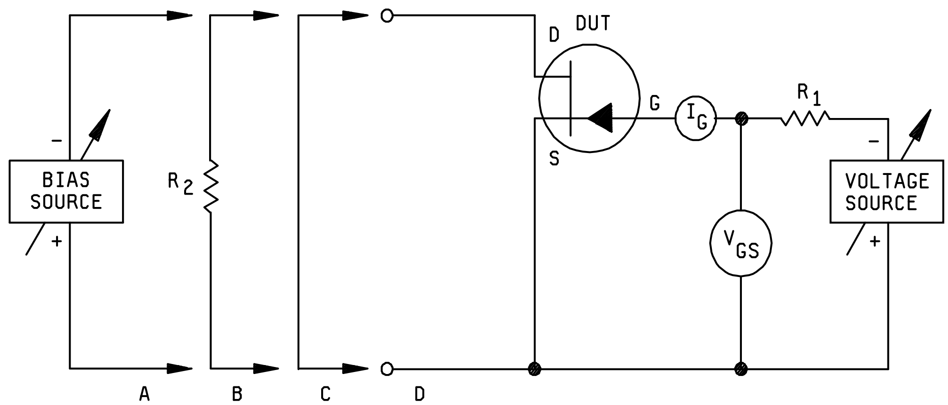
Circuits are shown for n-channel field-effect transistors in one circuit configuration only. They may readily be adapted for p-channel devices and for other circuit configurations.

METHOD 3401.1

BREAKDOWN VOLTAGE, GATE TO SOURCE

1. Purpose. The purpose of this test is to determine if the breakdown voltage of the field-effect transistor or IGBT under the specified conditions is greater than the specified minimum limit. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test circuit. See figure 3401-1.



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 3401-1. Test circuit for breakdown voltage, gate to source.

3. Procedure. The resistor R_1 is a current-limiting resistor and should be of sufficiently high resistance to avoid excessive current flowing through the device and current meter. The voltage shall be gradually increased, with the specified bias condition (condition A, B, C, or D) applied, from zero until either the minimum limit for $V_{(BR)GSX}$ 1/ or the specified test current is reached. The device is acceptable if the minimum limit for $V_{(BR)GSX}$ is reached before the test current reaches the specified value. If the specified test current is reached first, the device shall be considered a failure.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test current (see 3.).

b. Bias condition:

A: Drain to source: Reverse bias (specify bias voltage).

B: Drain to source: Resistance return (specify resistance of R_2).

C: Drain to source: Short circuit.

D: Drain to source: Open circuit.

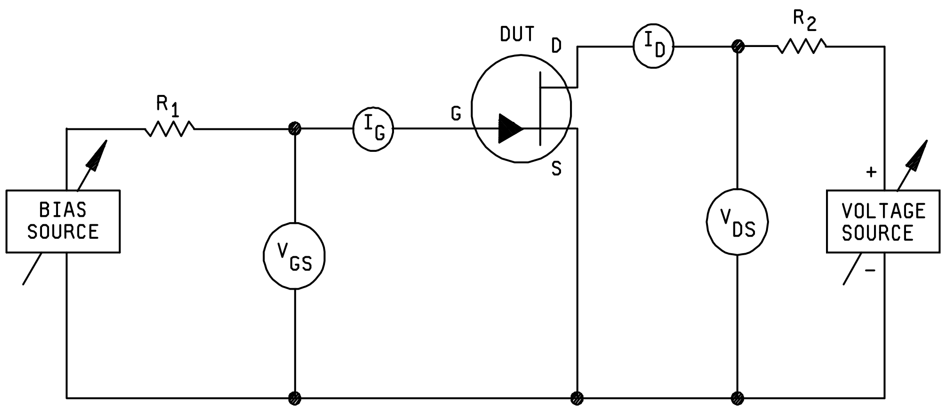
1/ $V_{(BR)GSX}$: Breakdown voltage, gate to source, with the specified bias condition applied from drain to source.

METHOD 3403.1

GATE TO SOURCE VOLTAGE OR CURRENT

1. Purpose. The purpose of this test is to measure the gate to source voltage or current of the field-effect transistor or IGBT under the specified conditions. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test circuit. See figure 3403-1.



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 3403-1. Test circuit for breakdown voltage, gate to source.

3. Procedure. The voltage source and bias source shall be adjusted to bring V_{DS} and I_D to their specified values. The voltage V_{GS} or current I_G may then be read.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltages and currents (see 3.).

b. Parameter to be measured.

METHOD 3404

MOSFET THRESHOLD VOLTAGE

1. Purpose. This method establishes the means for measuring MOSFET threshold voltage. This method applies to both enhancement-mode and depletion-mode MOSFETs, and for both silicon on sapphire and bulk-silicon MOSFETs. It is for use primarily in evaluating the response of MOSFETs to ionizing radiation, and for this reason the test differs from conventional methods for measuring threshold voltage.

1.1 Definition.

MOSFET threshold voltage, $V_{GS(TH)}$: The gate-to-source voltage at which the drain current is reduced to the leakage current, as determined by this method.

2. Apparatus. The apparatus shall consist of a suitable ammeter, voltmeters, and voltage sources. The apparatus may be manually adjusted or, alternatively, may be digitally programmed or controlled by a computer. Such alternative arrangements shall be capable of the same accuracy as specified below for manually adjusted apparatus.

2.1 Ammeter (A_1). The ammeter shall be capable of measuring current in the range specified with a full scale accuracy of ±0.5 percent or better.

2.2 Voltmeters (V_1 and V_2. The voltmeters shall have an input impedance of 10 mΩ or greater and have a capability of measuring 0 to 20 V with a full scale accuracy of ±0.5 percent or better.

2.3 Voltage sources (V_{GS} and V_{DS}). The voltage sources shall be adjustable over a nominal range of 0 V to 20 V, have a capability of supplying output currents at least equal to the maximum rated drain current of the device to be tested, and have noise and ripple outputs less than 0.5 percent of the output voltage.

3. Procedure.

WARNING: The absolute maximum values of power dissipation, drain-to-source voltage, drain current, or gate-to-source voltage specified is either the applicable acquisition document or the manufacturer's specifications shall not be exceeded under any circumstances.

3.1 N-channel devices.

3.1.1 Test circuit for n-channel devices. The test circuit shown on figure 3404-1 shall be assembled and the apparatus turned on. With the voltage sources V_{DS} and V_{GS} set to 0 volts, the MOSFET to be tested shall be inserted into the test circuit. The gate-to-source polarity switch shall be set to the appropriate position, and voltage source V_{GS} shall be set 1.0 V negative with respect to the anticipated value of threshold voltage $V_{GS(TH)}$. Voltage source V_{DS} shall be adjusted until voltmeter V_2 indicates the specified drain-to-source voltage V_{DS}. The current I_D, indicated by ammeter A_1, and the gate-to-source voltage V_{GS}, indicated by voltmeter V_1, shall be measured and recorded.

3.1.2 Measurement for n-channel devices. The measurement shall be repeated at gate-to-source voltages which are successively 0.25 volts more positive until either the maximum gate-to-source voltage or maximum drain current is reached. If the gate-to-source voltage reaches 0 volts before either of these limits has been reached, the gate-to source polarity switch shall be changed as necessary and measurements shall continue to be made at gate-to-source voltages which are successively 0.25 volts more positive until one of these limits has been reached.

3.2 P-channel devices.

3.2.1 Test circuit for p-channel devices. The test circuit shown on figure 3404-2 shall be assembled and the apparatus turned on. With the voltage sources V_{GS} and V_{DS} set to 0 volts, the MOSFET to be tested shall be inserted into the test circuit. The gate-to-source polarity switch shall be set to the appropriate position, and voltage source V_{GS} shall be set 1.0 V positive with respect to the anticipated value of threshold voltage $V_{GS(TH)}$. Voltage source V_{DS} shall be adjusted until voltmeter V_2 indicates the specified drain-to-source voltage V_{DS}. The current I_D, indicated by ammeter A_1, and the gate-to-source voltage V_{GS}, indicated by voltmeter V_1, shall be measured and recorded.

3.2.2 Measurement for p-channel devices. The measurement shall be repeated at gate-to-source voltages are successively 0.25 volts more negative until either the maximum gate-to-source voltage or maximum drain current is reached. If the gate-to-source voltage reaches 0 volts before either of these limits has been reached, the gate-to-source polarity switch shall be changed as necessary and measurements shall continue to be made at gate-to-source voltages which are successfully 0.25 volts more negative until one of these limits has been reached.

3.3 Leakage current measurement. Using method 3415, the leakage current shall be measured.

3.3.1 Drain-to-source voltage. The drain-to-source voltage shall be as specified in 4.b.

3.3.2 Gate-to-source voltage. The gate-to-source voltage shall be five volts different from the anticipated threshold voltage in the direction of reduced drain current.

3.4 Gate-to-source voltage graph. The gate-to-source voltage, V_{GS} shall be plotted versus the square-root of the drain current minus the leakage current, $\sqrt{I_D - I_L}$. At the point of maximum slope, a straight line shall be extrapolated downward. The threshold voltage $V_{GS(TH)}$ is the intersection of this line with the gate-to-source voltage axis. Examples are shown on figure 3404-3.

3.5 Report. As a minimum, the report shall include the device identification, the test date, the test operator, the test temperature, the drain-to-source voltage, the range of gate-to-source voltage, the leakage current, and the threshold voltage.

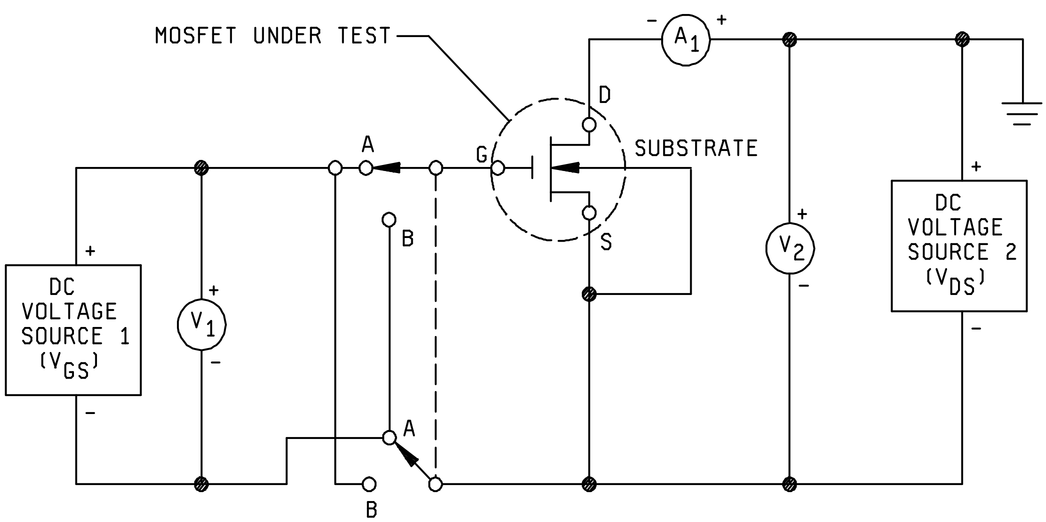
4. Summary. The following conditions shall be specified in the detail specification:

a. Test temperature. Unless otherwise specified, the test shall be performed at ambient.

b. Drain-to-source voltage.

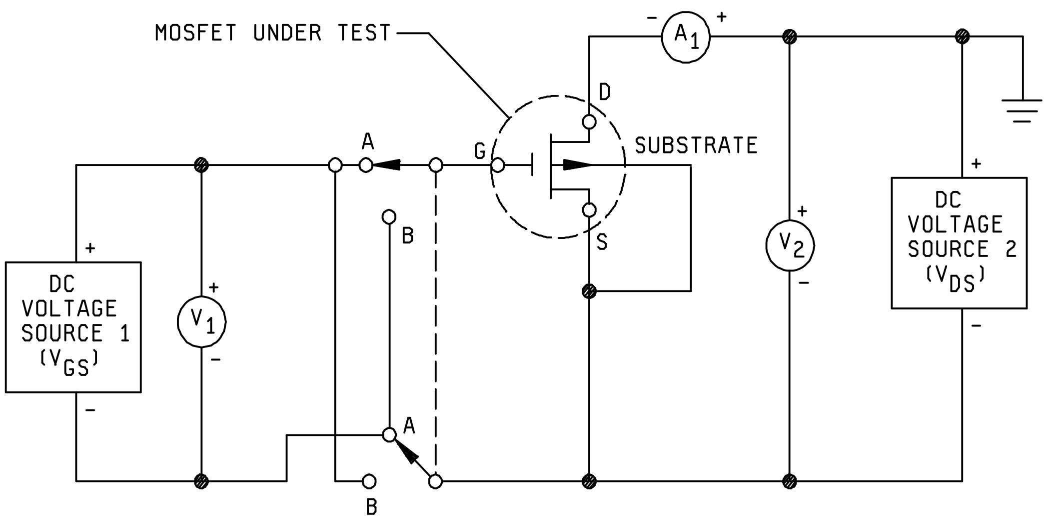
c. Maximum drain current.

d. Range of gate-to-source voltage.



NOTE: Gate-to-source polarity switch set at:
A for enhancement mode
B for depletion mode

FIGURE 3404-1. Test circuit for n-channel MOSFETs.



NOTE: Gate-to-source polarity switch set at:
A for enhancement mode
B for depletion mode

FIGURE 3404-2. Test circuit for p-channel MOSFETs.

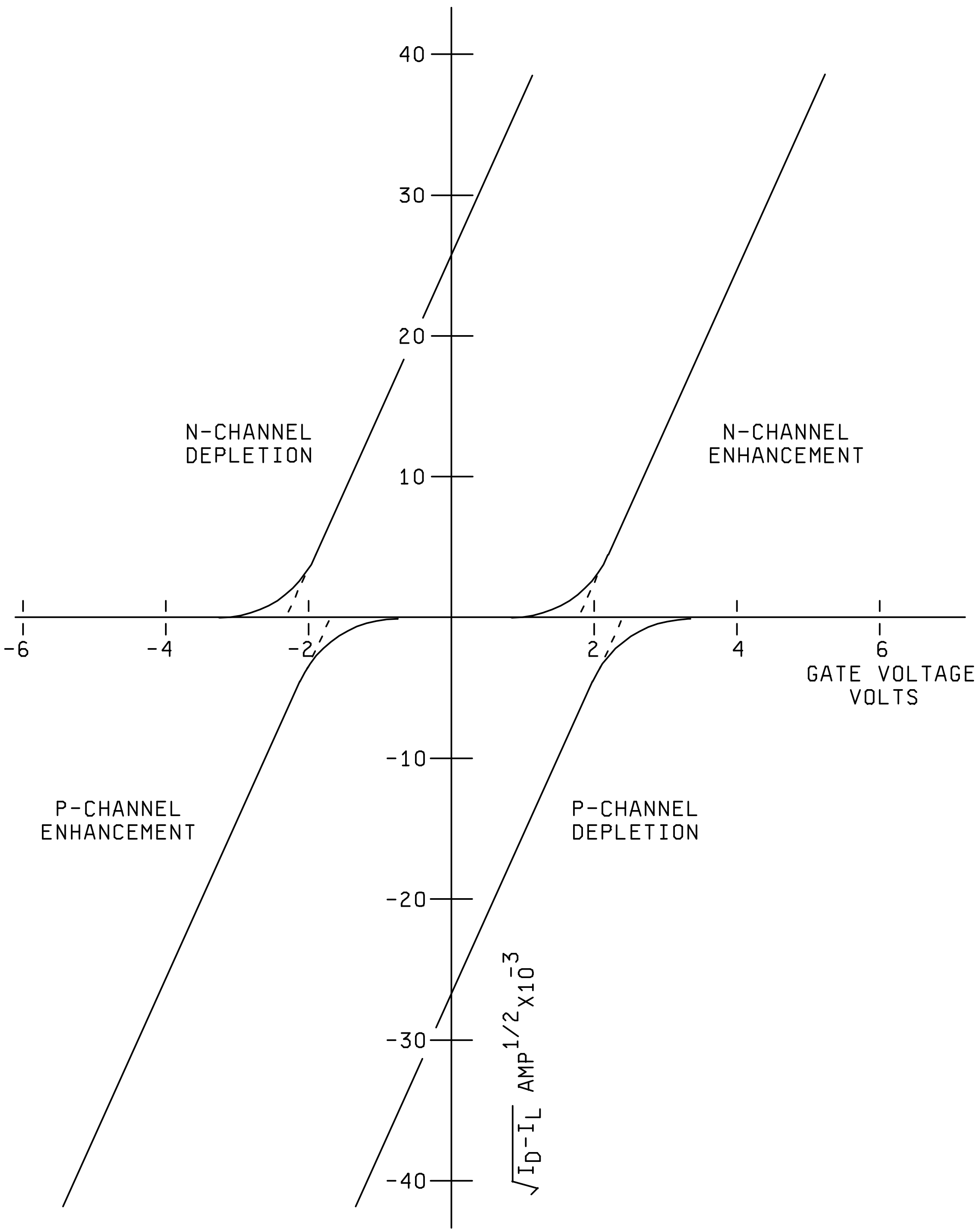


FIGURE 3404-3. Examples of curves.

METHOD 3405.1

DRAIN TO SOURCE ON-STATE VOLTAGE

1. Purpose. The purpose of this test is to measure the drain to source voltage of the field-effect transistor or IGBT at the specified value of drain current. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test circuit. See figure 3405-1.

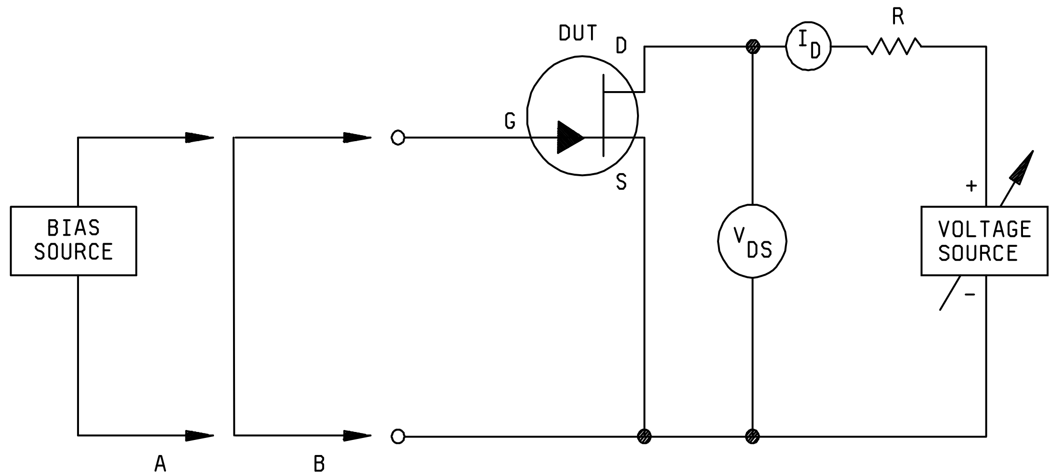


FIGURE 3405-1. Test circuit for drain to source on-state voltage.

3. Procedure. The specified bias condition shall be applied between the gate and source and the voltage source shall be adjusted to bring I_D to the specified value. The voltage V_{DS} may then be read.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test current (see 3.).

b. Gate to source bias condition:

A: Voltage-biased (specify bias voltage and polarity).

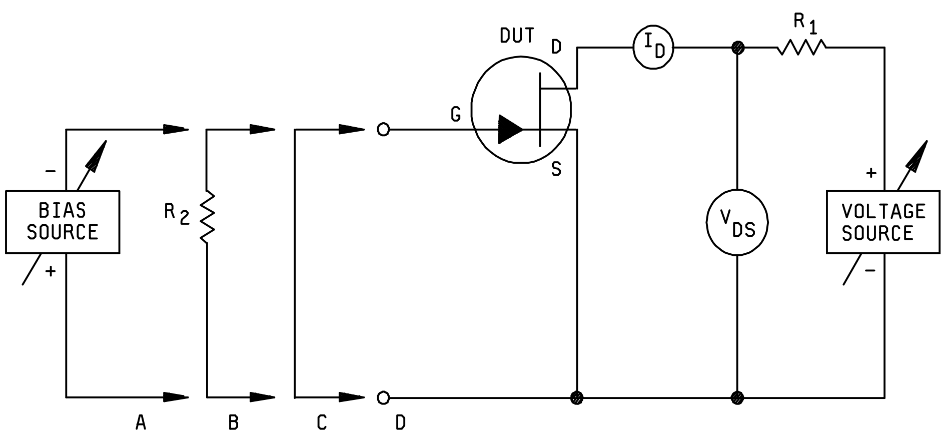
B: Short-circuited.

METHOD 3407.1

BREAKDOWN VOLTAGE, DRAIN TO SOURCE

1. Purpose. The purpose of this test is to determine if the breakdown voltage of the field-effect transistor or IGBT under the specified conditions is greater than the specified minimum limit. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test circuit. See figure 3407-1.



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 3407-1. Test circuit for breakdown voltage, drain to source.

3. Procedure. The resistor R_1 is a current-limiting resistor and should be of sufficiently high resistance to avoid excessive current flowing through the device and current meter. The voltage shall be gradually increased from zero, with the specified bias condition (condition A, B, C, or D) applied, until either the minimum limit for $V_{(BR)DSX}$ 1/ or the specified test current is reached. The device is acceptable if the minimum limit for $V_{(BR)DSX}$ is reached before the test current reaches the specified value. If the specified test current is reached first, the device shall be considered a failure.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test current (see 3.).

b. Bias condition:

A: Gate to source: Reverse bias. (Specify bias voltage.)

B: Gate to source: Resistance return. (Specify resistance of R_2.)

C: Gate to source: Short circuit.

D: Gate to source: Open circuit.

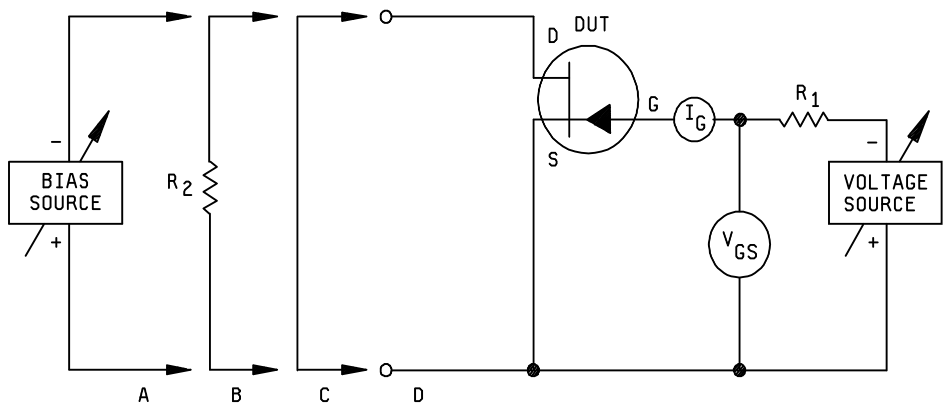
1/ $V_{(BR)DSX}$: Breakdown voltage, drain to source, with the specified bias condition applied from gate to source.

METHOD 3411.1

GATE REVERSE CURRENT

1. Purpose. The purpose of this test is to measure the gate reverse current of the field-effect transistor or IGBT under the specified conditions. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test circuit. See figure 3411-1.



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the volt meter readings shall be corrected for the drop across the ammeter.

FIGURE 3411-1. Test circuit for gate reverse current.

3. Procedure. The specified dc voltage shall be applied between the gate and the source with the specified bias condition (condition A, B, C, or D) applied to the drain. The measurement of current shall be made at the specified ambient or case temperature.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltage (see 3.).

b. Test temperature if other than +25°C ±3°C ambient (see 3.).

c. Bias condition:

A: Drain to source: Reverse bias. (Specify bias voltage.)

B: Drain to source: Resistance return. (Specify resistance of R_2.)

C: Drain to source: Short circuit.

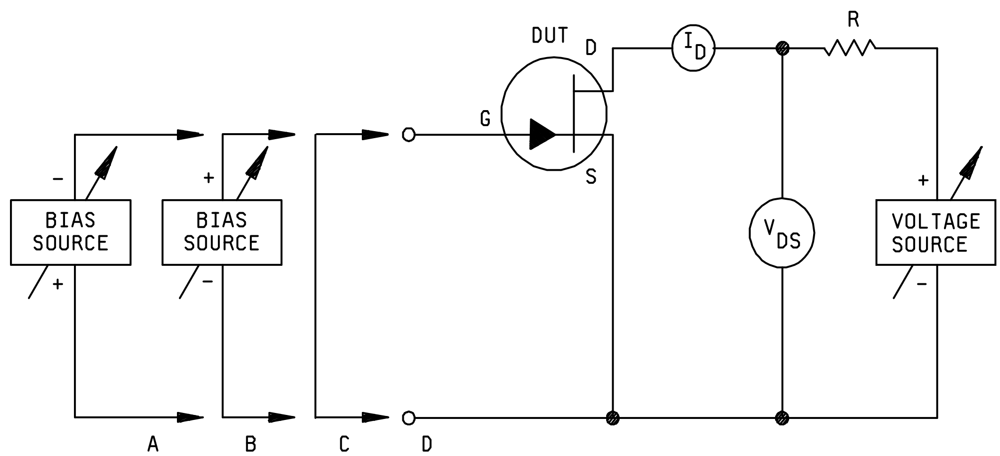
D: Drain to source: Open circuit.

METHOD 3413.1

DRAIN CURRENT

1. Purpose. The purpose of this test is to measure the drain current of the field-effect transistor or IGBT under the specified conditions. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test circuit. See figure 3413-1.



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the volt meter readings shall be corrected for the drop across the ammeter.

FIGURE 3413-1. Test circuit for drain current.

3. Procedure. The specified voltage shall be applied between the drain and source with the specified bias condition (condition A, B, C, or D) applied to the gate. The measurement of current shall be made at the specified ambient or case temperature.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltage (see 3.).

b. Test temperature if other than +25°C ±3°C ambient (see 3.).

c. Parameter to be measured.

d. Bias condition:

A: Gate to source: Reverse bias. (Specify bias voltage.)

B: Gate to source: Forward bias. (Specify bias voltage.)

C: Gate to source: Short circuit.

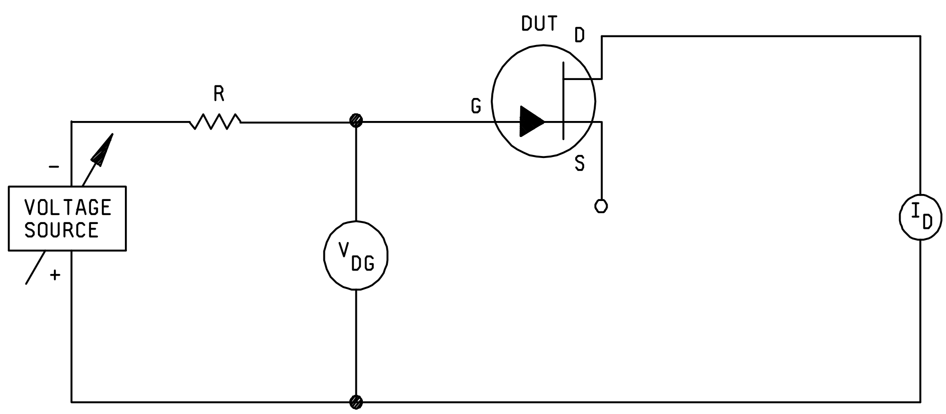
D: Gate to source: Open circuit.

METHOD 3415.1

DRAIN REVERSE CURRENT

1. Purpose. The purpose of this test is to measure the drain reverse current of the field-effect transistor or IGBT under the specified conditions. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test circuit. See figure 3415-1.



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the volt meter readings shall be corrected for the drop across the ammeter.

FIGURE 3415-1. Test circuit for drain reverse current.

3. Procedure. The specified dc voltage shall be applied between the drain and the gate. The measurement of current shall be made at the specified ambient or case temperature.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltage (see 3.).

b. Test temperature if other than +25°C ±3°C ambient (see 3.).

METHOD 3421.1

STATIC DRAIN TO SOURCE ON-STATE RESISTANCE

1. Purpose. The purpose of this test is to measure the resistance between the drain and source of the field-effect transistor or IGBT under the specified static condition. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test circuit. See figure 3421-1.

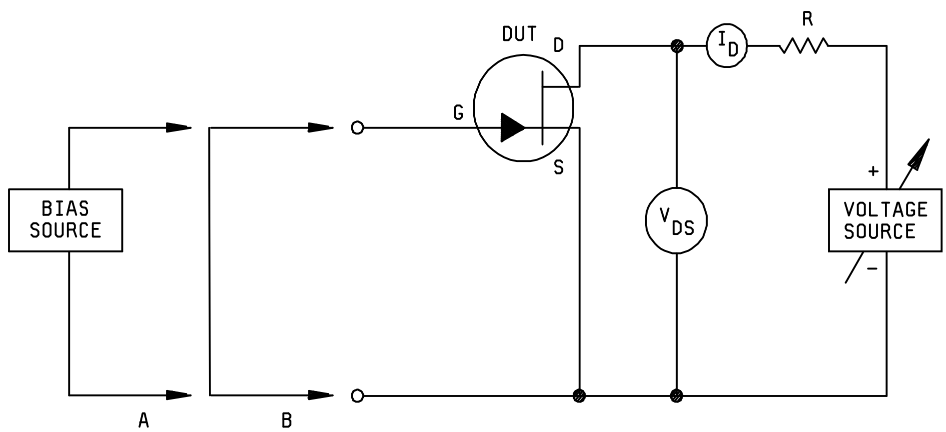


FIGURE 3421-1. Test circuit for static drain to source on-state resistance.

3. Procedure. The specified bias condition shall be applied between the gate and source and the voltage source shall be adjusted so that the specified current is achieved. The drain to source voltage shall then be measured.

$$\textit{Then:}\quad r_{DS(on)} = \frac{V_{DS}}{I_D}$$

4. Summary. The following conditions shall be specified in the detail specification:

a. Test currents.

b. Gate to source bias condition:

A: Voltage-biased (specify bias voltage and polarity).

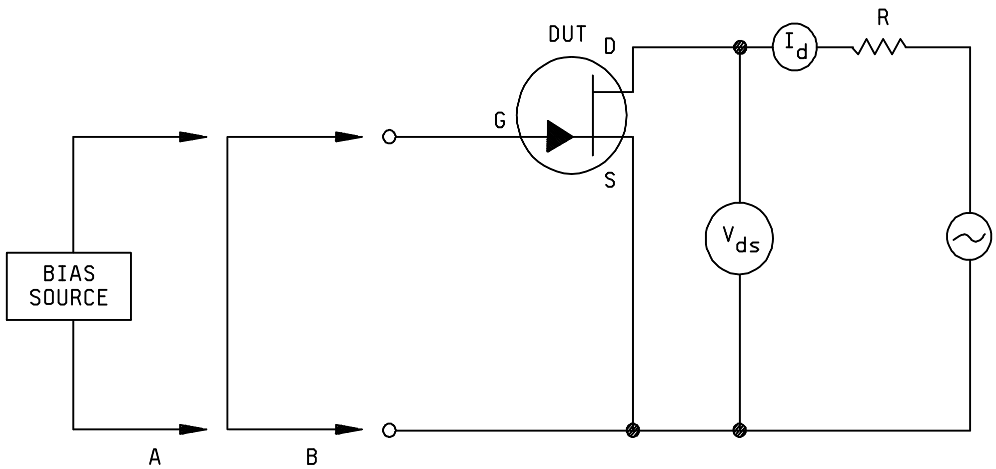
B: Short circuited.

METHOD 3423

SMALL-SIGNAL, DRAIN TO SOURCE ON-STATE RESISTANCE

1. Purpose. The purpose of this test is to measure the resistance between the drain and source of the field-effect transistor under the specified small-signal conditions.

2. Test circuit. See figure 3423-1.



NOTE: The ac voltmeter shall have an input impedance high enough that halving it does not change the measured value within the required accuracy of the measurement.

FIGURE 3423-1. Test circuit for small-signal, drain to source on-state resistance.

3. Procedure. The specified bias condition shall be applied between the gate and the source and an ac sinusoidal signal current, I_d, of the specified rms value shall be applied.

$$\text{Then:} \quad r_{ds(on)} = \frac{V_{ds}}{I_d}$$

4. Summary. The following conditions shall be specified in the detail specification:

a. Test current (see 3.).

b. Test frequency.

c. Gate to source bias condition:

A: Voltage-biased (specify bias voltage and polarity).

B: Short-circuited.

METHOD 3431

SMALL-SIGNAL, COMMON-SOURCE, SHORT-CIRCUIT, INPUT CAPACITANCE

1. Purpose. The purpose of this test is to measure the input capacitance of the field-effect transistor under the specified small-signal conditions.

2. Test circuit. The circuit and procedure shown are for common-source configuration. For other configurations the circuit and procedure should be changed accordingly.

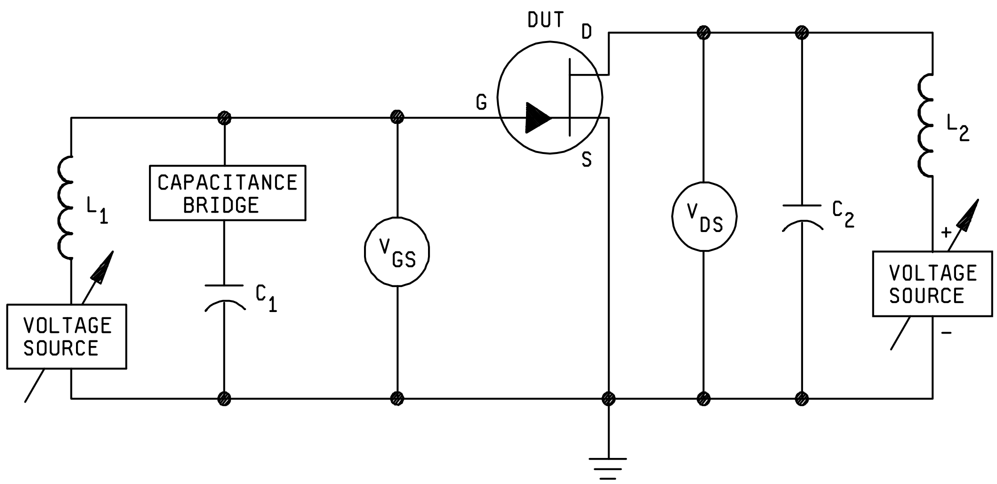


FIGURE 3431-1. Test circuit for small-signal, common-source, short-circuit, input capacitance.

3. Procedure. The capacitors C_1 and C_2 shall present short circuits at the test frequency. L_1 and L_2 shall present a high ac impedance at the test frequency for isolation. The bridge shall have low dc resistance between its output terminals and should be capable of carrying the test current without affecting the desired accuracy of measurement.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltages and currents.

b. Measurement frequency.

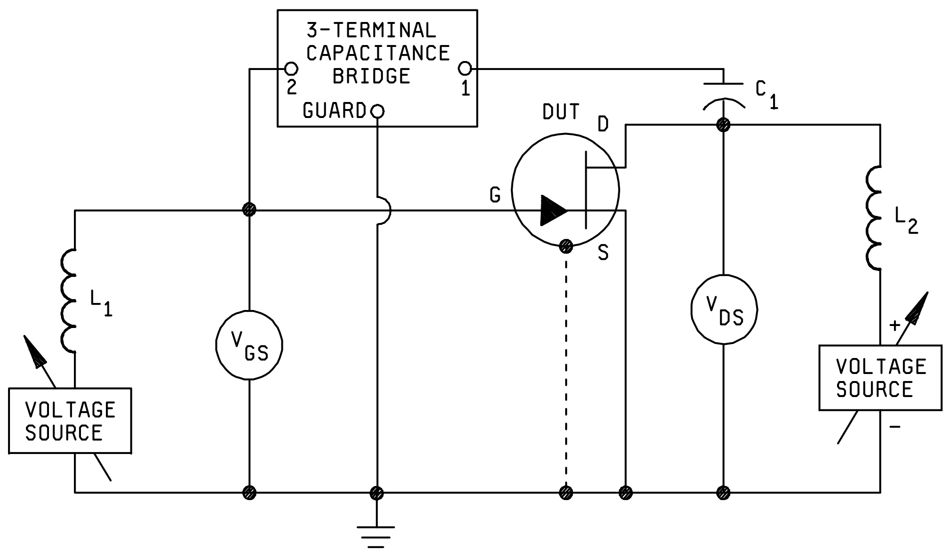
c. Parameter to be measured.

METHOD 3433

SMALL-SIGNAL, COMMON-SOURCE, SHORT-CIRCUIT, REVERSE-TRANSFER CAPACITANCE

1. Purpose. The purpose of this test is to measure the reverse-transfer capacitance of the field-effect transistor under the specified conditions.

2. Test circuit. The circuit and procedure shown are for common-source configuration. For other configurations the circuit and procedure should be changed accordingly. Terminal 2 of bridge shall be the terminal with an ac potential closest to the ac potential of the guard terminal so as to provide an effective short circuit of the input.



NOTE: The dotted connection between the case and ground shall be used for devices in which the case is not internally electrically connected to any element. If the case is internally electrically connected to any element, the dotted connection shall not be used.

FIGURE 3433-1. Test circuit for small signal, common-source, short-circuit, reverse-transfer capacitance.

3. Procedure. The capacitor C_1 shall present a short circuit at the test frequency. L_1 and L_2 shall present a high ac impedance at the test frequency for isolation. The bridge shall have low dc resistance between its output terminals and should be capable of carrying the test current without affecting the desired accuracy of measurement.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test voltages and currents.

b. Measurement frequency.

c. Parameter to be measured.

METHOD 3453

SMALL-SIGNAL, COMMON-SOURCE, SHORT-CIRCUIT, OUTPUT ADMITTANCE

1. Purpose. The purpose of this test is to measure the output admittance of the field-effect transistor under the specified small-signal conditions.

2. Test circuit. The circuit and procedure are shown for common-source configuration. For other configurations the circuit and procedure should be changed accordingly.

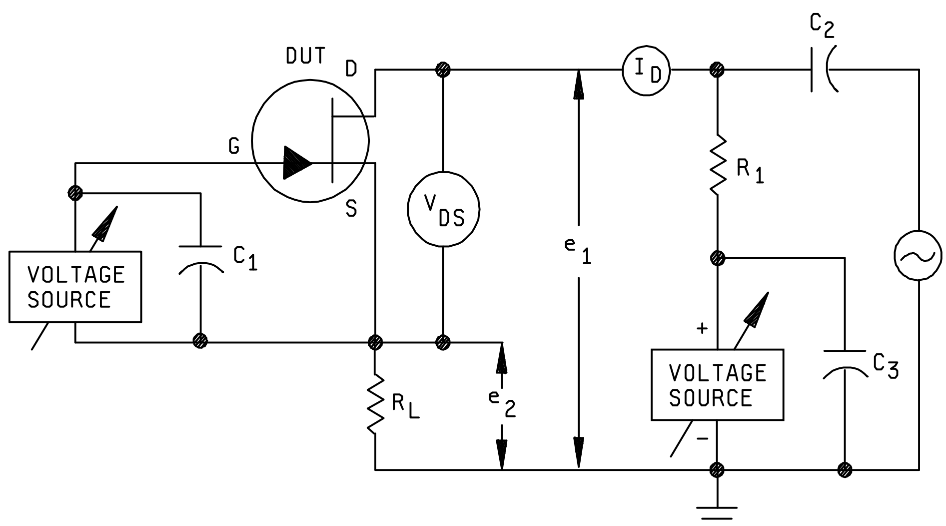


FIGURE 3453-1. Test circuit for small-signal, common-source, short-circuit, output admittance.

3. Procedure. The capacitors C_1, C_2, and C_3 shall present short circuits at the test frequency in order to effectively couple and bypass the test signal. R_1 and R_L shall be short circuits compared with the output impedance of the device. After setting the specified dc conditions, the V_{DS} meter shall be disconnected from the circuit while measuring e_1 and e_2. The voltages e_1 and e_2 shall be measured with high-impedance ac voltmeters.

$$\text{Then: } y_{os} = \frac{I_d}{e_1 - e_2} \quad \text{Where: } I_d = \frac{e_2}{R_L} \quad \text{Thus: } y_{os} = \frac{\frac{e_2}{R_L}}{e_1 - e_2}$$

4. Summary. The following conditions shall be specified in the detail specification:

a. Test frequency.

b. Test voltages and currents.

c. Parameter to be measured.

METHOD 3455

SMALL-SIGNAL, COMMON-SOURCE, SHORT-CIRCUIT, FORWARD TRANSADMITTANCE

1. Purpose. The purpose of the test is to measure the forward transadmittance of the field-effect transistor under the specified small-signal conditions.

2. Test circuit. The circuit and procedure shown are for common-source configuration. For other configurations the circuit and procedure should be changed accordingly.

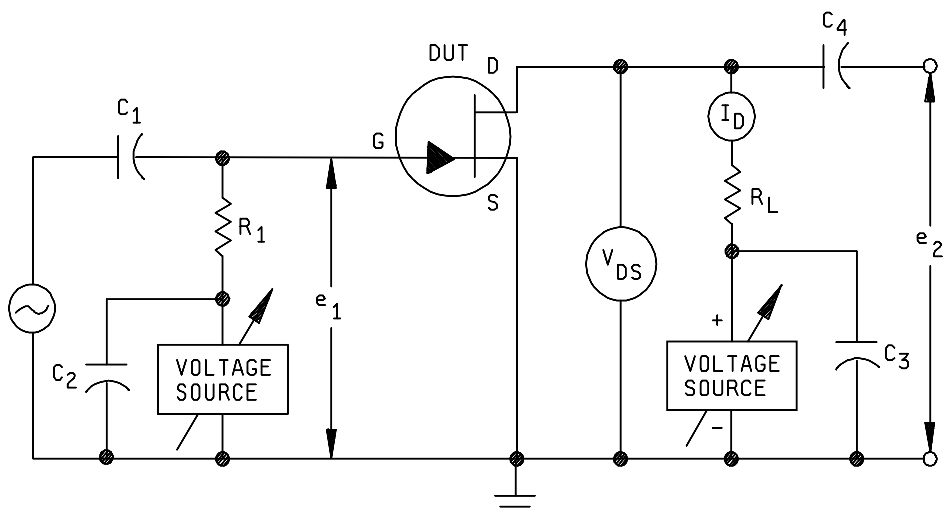


FIGURE 3455-1. Test circuit for small-signal, common-source, short-circuit, forward transadmittance.

3. Procedure. The capacitors C_1, C_2, C_3, and C_4 shall present short circuits at the test frequency in order to effectively couple and bypass the test signal. R_1 shall be a short circuit compared with the input impedance of the device. R_L shall be a short circuit compared with the output impedance of the device. The voltages e_1 and e_2 shall be measured with high-impedance ac voltmeters.

$$\text{Then: } y_{fs} = \frac{I_d}{e_1} \quad \text{Where: } I_d = \frac{e_2}{R_L} \quad \text{Thus: } y_{fs} = \frac{\frac{e_2}{R_L}}{e_1} = \frac{e_2}{e_1 \bullet R_L}$$

4. Summary. The following conditions shall be specified in the detail specification:

a. Test frequency.

b. Test voltages and currents.

c. Parameter to be measured.

METHOD 3457

SMALL-SIGNAL, COMMON-SOURCE, SHORT-CIRCUIT, REVERSE TRANSFER ADMITTANCE

1. Purpose. The purpose of the test is to measure the reverse transfer admittance under the specified small-signal conditions.

2. Test circuit. The circuit and procedure shown are for common-source configuration. For other configurations, the circuit and procedure should be changed accordingly.

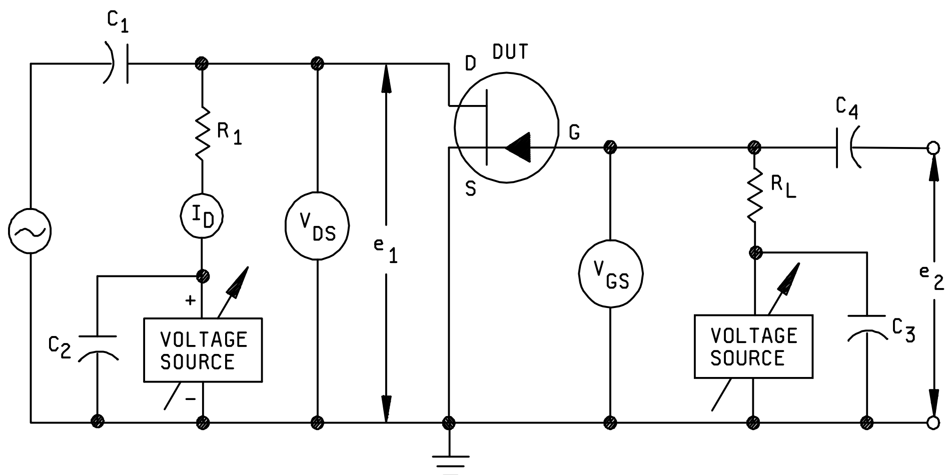


FIGURE 3457-1. Test circuit for small-signal, common-source, short-circuit, reverse transfer admittance.

3. Procedure. The capacitors C_1, C_2, C_3, and C_4 shall present short circuits at the test frequency in order to effectively couple and bypass the test signal. R_1 shall be impedance matched to the generator. R_L shall be a short-circuit compared with the input impedance of the device. The rms voltages e_1 and e_2 shall be measured with high-impedance ac voltmeters.

V_{DS} shall be adjusted to the specified value, then the gate voltage supply shall be adjusted so that V_{GS} or I_D equals the specified value, and the voltages e_1 and e_2 shall be measured.

$$\text{Then: } y_{rs} = \frac{I_g}{e_1} \quad \text{Where: } I_g = \frac{e_2}{R_L}$$

$$\text{Thus: } y_{rs} = \frac{\frac{e_2}{R_L}}{e_1} \quad \text{or } y_{rs} = \frac{e_2}{e_1 \; R_L}$$

4. Summary. The following conditions should be specified in the detail specification:

a. Test frequency.

b. Test voltages and currents.

c. Parameter to be measured.

METHOD 3459

PULSE RESPONSE (FET)

1. Purpose. The purpose of this test is to measure the pulse response ($t_{d(on)}$, t_r, $t_{d(off)}$, and t_f) of the field-effect transistor under the specified conditions.

2. Test circuit. The test circuit shall be as shown in the individual specification.

3. Procedure. The FET shall be tested in the specified circuit. $V_{in(on)}$, $V_{in(off)}$, pulse generator impedance, all circuit components, and supply voltages shall be as specified.

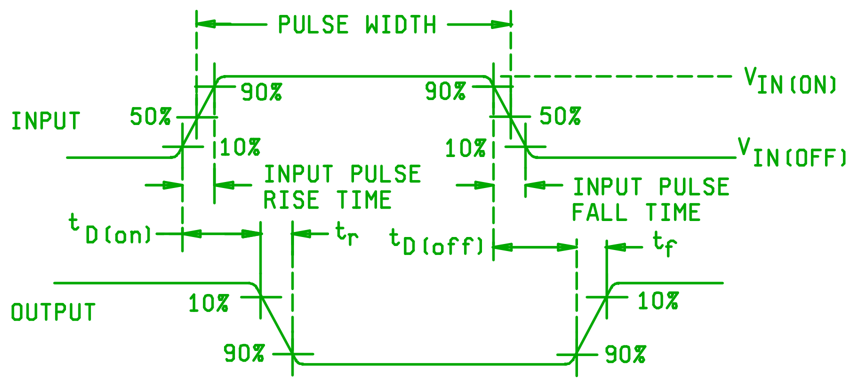


FIGURE 3459-1. Pulse characteristics.

Pulse characteristics are defined on figure 3459-1. The rise time, fall time, duty cycle or pulse repetition rate, and pulse width of the input waveform together with the input resistance, capacitance, and response time of the response detector shall all be such that halving or doubling these parameters will not affect the results of the measurement greater than the precision of measurement.

4. Summary. The following conditions shall be specified in the detail specification:

a. Input pulse levels $V_{in(on)}$ and $V_{in(off)}$.

b. Output impedance of pulse generator.

c. Circuit with all components.

d. All supply voltages.

e. Parameters to be measured.

METHOD 3461

SMALL-SIGNAL, COMMON-SOURCE, SHORT-CIRCUIT, INPUT ADMITTANCE

1. Purpose. The purpose of this test is to measure the input admittance of the field-effect transistor under the specified small-signal conditions.

2. Test circuit. The circuit and procedure shown are for common-source configuration. For other configurations the circuit and procedure should be changed accordingly.

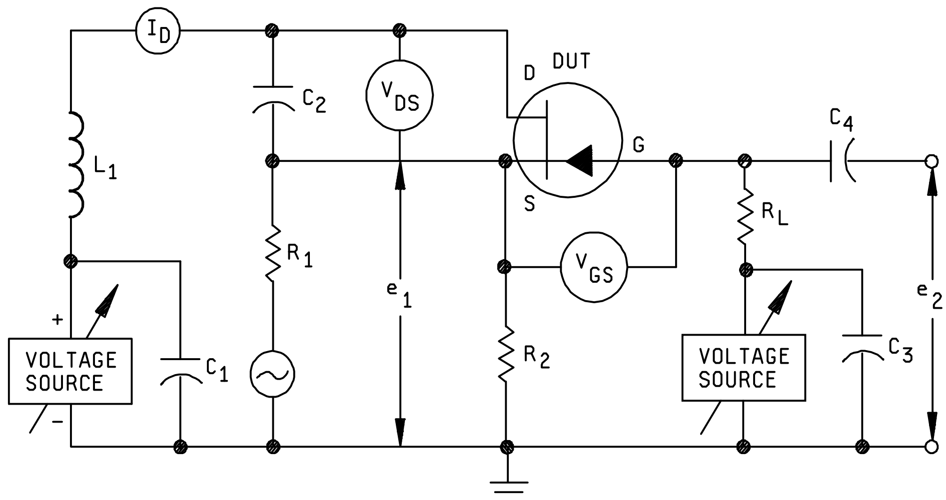


FIGURE 3461-1. Test circuit for small-signal, common-source, short-circuit, input admittance.

3. Procedure. The capacitors C_1, C_2, C_3, and C_4 shall present short circuits at the test frequency in order to effectively couple and bypass the test signal. R_1 facilitates the adjustment of e_1. Its use is optional. R_2 shall be such that dc biasing is possible. R_L shall be a short circuit compared with the input impedance of the device. V_{DS} shall be adjusted to the specified value, then the gate voltage supply shall be adjusted so that V_{GS} or I_D equals the specified value, and the voltages e_1 and e_2 shall be measured.

$$\text{Then: } y_{is} = \frac{I_g}{e_1} \quad \text{Where: } I_g = \frac{e_2}{R_L}$$

$$\text{Thus: } y_{is} = \frac{\frac{e_2}{R_L}}{e_1 - e_2} \quad \text{or} \quad y_{is} = \frac{e_2}{R_L\,(e_1 - e_2)}$$

$$e_1 \text{ must be greater than } e_2\text{; therefore, } y_{is} = \frac{e_2}{R_L \; e_1}$$

4. Summary. The following conditions shall be specified in the detail specification:

a. Test frequency.

b. Test voltages and currents.

c. Parameter to be measured.

METHOD 3469

REPETITIVE UNCLAMPED INDUCTIVE SWITCHING

1. Purpose. This purpose of this test method is to determine the repetitive inductive avalanche switching capability of power devices.

2. Scope. This method is intended as an endurance test for any power switching device designed and specified with repetitive avalanche capability.

3. Circuitry. The basic circuit is shown on figure 3469-1. The circuit shall be designed so that all stray reactances are held to a minimum. The inductor L shall be of a fast response type.

4. Definitions. The following terms and symbols apply to this test method:

T_J: Junction temperature.

$T_{J(max)}$: The maximum specified junction temperature.

$R_{\theta JC}$: Thermal resistance from the junction to the case.

L: Load inductance in accordance with DUT.

E_{AR}: Repetitive avalanche energy, minimum.

I_{AR}: Repetitive avalanche current, maximum.

E_{on}: On state energy.

f: Frequency.

T_C: Case temperature.

P_D: Power dissipation of device.

$V_{(BR)}$: Breakdown or avalanche voltage of device.

V_{DD}: Power supply voltage.

R_S: Stray circuit resistance.

t_{av}: time in avalanche.

5. Procedure.

5.1 Screening. The DUT must be screened prior to avalanche and meet all specified parameters.

5.2 Calculations. The energy delivered to the DUT can be calculated as follows:

a. $$E_{AR} = \frac{\dfrac{L * I_{AR^2} * V_{(BR)}}{\left[V_{(BR)} - V_{DD}\right]}}{2}$$

$$NOTE: \quad R_S = 0, where, \; V_{(BR)} = \frac{LI_{AR^2}}{t_{AV}}$$

b. $$E_{AR} = V_{(BR)} I_{AR} \left(\frac{L}{R_S}\right) \ln \left[\frac{I_{AR} R_S}{(V_{BR} - V_{DD}) + 1}\right]$$

NOTE: $R_S \neq 0$

5.2.1 Energy delivered. The actual energy delivered to the DUT can vary depending on the real value of R_S. Since this is test circuit dependent, the actual energy delivered must be verified by observing the voltage across the DUT and current through the DUT waveforms (see figure 3469-1). Empirically record the $V_{(BR)}$, I_{AR}, and t_{av}. Then calculate:

$E_{AR} = 1/2\ V_{(BR)} I_{AR}\ t_{av}$ (in accordance with figure 3469-1).

If this empirically derived value is not greater than or equal to the specified minimum E_{AR} value, the circuit must be compensated until it is.

5.3 Junction temperature. T_J during the test must be held constant to T_J (max) +0°C -10°C, based on the case temperature of the DUT and the $R_{\theta JC}$ or the junction temperature as determined using a TSP. The power dissipated in the DUT is equal to the sum of the on energy and the avalanche energy multiplied by the frequency. The E_{on} in most cases can be neglected.

So: $P_D = f * (E_{AR} + E_{on})$

$T_J = P_D * R_{\theta JC} + T_C$

The case temperature of the DUT will be measured at a specified reference point under the heat source. It is also possible to measure the temperature of the heat sink at a specified reference point provided that an accurate value of the thermal resistance case-to-heat-sink-reference-point is known. The measured junction temperature based on measurements of a TSP may also be substituted for the junction temperature calculated from case temperature.

5.4 Number of pulses. The DUT will be avalanched for a specified minimum number of pulses at specified conditions. Upon completion the specified device parameters will be tested.

6. Summary. Unless otherwise specified in the detail specifications, the following parameters shall be as follows:

E_{AR}: (Repetitive avalanche energy (joules)).

I_{AR}: (Repetitive avalanche current (amperes)).

T_J: +150°C +0°C, -10°C.

t_{av}: 2 µs minimum, 2 µs maximum.

f: 500 Hz, minimum.

N: 3.6 x 10^8 minimum number of pulses.

$$L = \left[\frac{2\ E_{AR}}{(I_{DI})^2}\right]\left[\frac{V_{BR} - V_{DD}}{V_{BR}}\right]\ nH\ minimum$$

Supply voltage ±50 V.

7. Failure criteria. The DUT must be within all specified parameter limits at the completion of the test. As a minimum, V_{BR} shall be greater than or equal to rated breakdown voltage and applicable leakage currents.

METHOD 3470.2

SINGLE PULSE UNCLAMPED INDUCTIVE SWITCHING

1. Purpose. This method is applicable to power MOSFET's and IGBT. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E. The purpose of this test method is to screen out weak devices which otherwise may result in costly equipment failures. This is accomplished by providing a controlled means of testing the capability of a power MOSFET or IGBT to withstand avalanche breakdown while turning off with an unclamped inductive load under specified conditions. The device capability is a strong function of the peak drain current at turn-off and the circuit inductance. Since no voltage clamping circuits or devices are employed, essentially, all of the energy stored in the inductor must be dissipated in the DUT at turn-off. It is not the intent of this test method to closely duplicate actual application conditions where device temperatures may approach maximum rated value, repetition rates may be 10 to 100 kHz, and voltage transients are usually only a few microseconds in duration. However, experience has shown that failures in actual applications can be greatly reduced or eliminated if devices are tested for avalanche operation under defined circuit conditions at very low repetition rates and at room ambient temperature.

2. Test procedures. The specified value of inductance L shall be connected into the circuit (see figures 3470-1 and 3470-2). The gate pulse shall be applied to the device at the specified repetition rate. The V_{DD} supply voltage shall be applied. The gate pulse width shall be adjusted as necessary until the specified drain current I_D is reached. Test failures are defined as those devices which fail catastrophically.

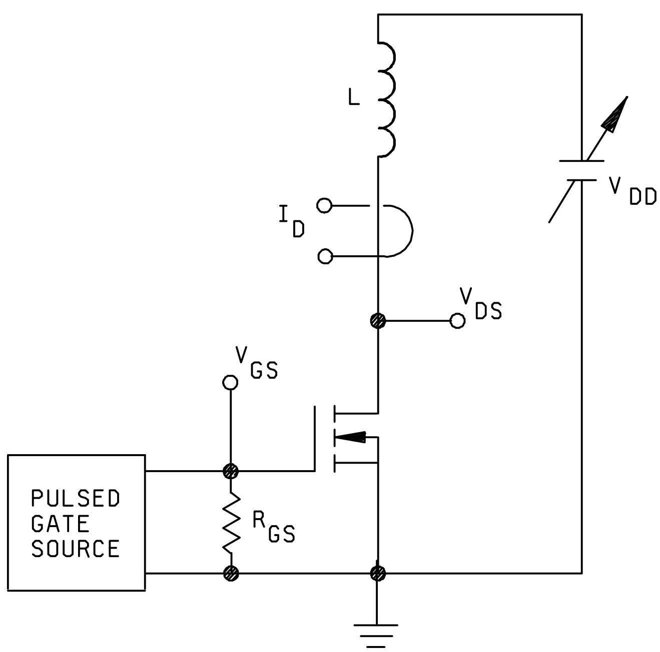
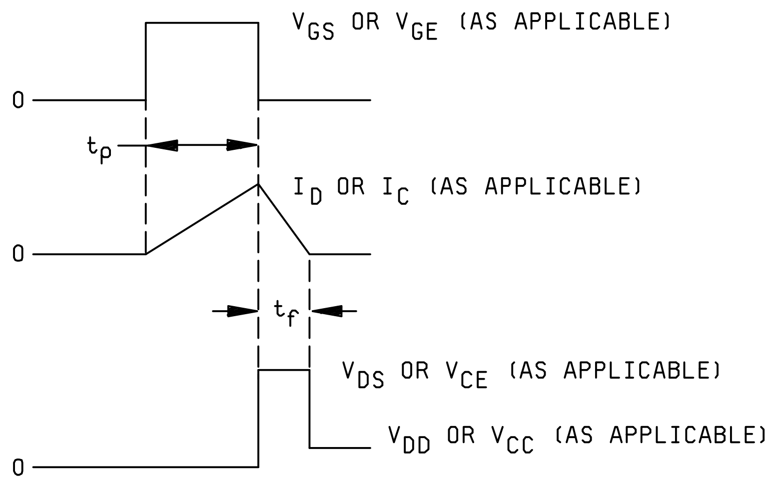


FIGURE 3470-1. Unclamped inductive switching circuit.

NOTE: The test circuit, shown for n-channel devices, is also applicable for p-channel devices with appropriate changes in polarities and symbols.



NOTES: The following notes are provided in the interest of achieving comparable results from various test circuits employed to perform this test.

a. Air core inductors are recommended for this test to avoid the possibility of core problems. If iron core inductors are used, care must be taken such that core saturation is not changing the effective value to the inductance L which will lead to non-repeatable test results.

b. The resistance of the inductor must be controlled since I^2R losses in the inductor will decrease the percentage of $LI^2/2$ stored energy transferred to the DUT. The relationship R = 0.015 (V_{DS}/I_D) applies for one percent of the stored energy being dissipated in the resistance. For two percent loss, R = 2 (.015) (V_{DS}/I_D) or (V_{CE}/I_C). The resistance loss shall be limited to two percent maximum, if not compensated by the equipment.

c. The gate to source resistor shall be closely connected to the test device. The gate to source resistor shall be a low enough value that the switching performance of the device does not affect the test and the inductor in the drain circuit determines the current waveform. The design of the pulsed gate source must be such that R_{GS} or R_{GE} is the effective gate to source resistance during the t_f portion of the test.

d. The repetition rate and duty cycle of the test shall be chosen so that device average junction temperature rise is minimal. Limits of one pulse per second or 0.5 percent duty cycle are recommended. The device peak junction temperature shall not exceed maximum rated value.

e. If the V_{DD} or V_{CE} power supply remains in series with the inductor during the t_f interval then the energy transferred to the DUT may be considerably higher than $LI^2/2$. If the gate pulse width is adjusted so that V_{CC} or $V_{DD} < 0.1\ V_{DS}$ or V_{CE} then the contribution of the power supply will be less than 10 percent of the stored $LI^2/2$ energy.

FIGURE 3470-2. Unclamped inductive switching power pulse.

3. Summary. The following conditions shall be specified in the detail specification:

a. Minimum peak current (I_D).

b. Peak gate voltage (V_{GS}).

c. Unless otherwise specified, gate to source resistor (R_{GS}) = 25 Ω to 50 Ω.

d. Initial case temperature (T_C).

e. Inductance (L).

f. V_{DD}.

METHOD 3471.2

GATE CHARGE

1. Purpose. The purpose of this test is to measure the gate charge (Q_g) of power MOSFET's and IGBT. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

1.1 Definitions.

a. Test 1: $Q_{g(th)}$ is the gate charge that must be supplied to reach the minimum specified gate-source threshold voltage. It establishes line loci through the origin of a Q = f(V_{gs}) graph that is invariant with I_D, V_{DD}, and T_J. It establishes a relationship with capacitance (i.e.,

$$C_{GS} = \frac{Q_{g(th)}}{V_{g(th)}} = \frac{Q_{gs}}{V_{GP}}).$$

b. Test 2: $Q_{g(on)}$ is the gate charge that must be supplied to reach the gate-source voltage specified for the device $r_{DS(on)}$ measurement.

c. Test 3: $Q_{gm(on)}$ is the gate charge that must be supplied to the device to reach the maximum rated gate-source voltage. $Q_{gm(on)}$ and $Q_{g(on)}$ establish line loci on a Q = f(V_{gs}) graph that may be considered invariant with I_D and T_J. The slope of the loci is invariant with V_{DD}, while the intercept with the Q axis is variant with V_{DD}.

d. Test 4: V_{GP} is the gate voltage necessary to support a specified drain current. V_{GP}, I_D is a point on the device gate voltage, drain current transfer characteristic. V_{GP} is variant with I_D and T_J. It may be measured one of two ways:

(1) Using a dc parameter test set employing a circuit similar to that described in method 3474 for SOA setting $V_{DD} > V_{GS}$.

(2) Using a gate charge test circuit employing a constant I_D drain load.

e. Test 5: Q_{gs} is the charge required by C_{GS} to reach a specified I_D. It is variant with I_D and T_J. It is measured in a gate charge test circuit employing a constant drain current load.

f. Test 6: Q_{gd} is the charge supplied to the drain from the gate to change the drain voltage under constant drain current conditions. It is variant with V_{DD} and may be considered invariant with I_D and T_J. It can be related to an effective gate-drain capacitance (i.e., $C_{rss} = Q_{gd}/V_{DD}$). The effective input capacitance is: $C_{iss} = C_{GS} + C_{rss}$.

2. Test procedure.

a. The gate charge test is performed by driving the device gate with a constant current and measuring the resulting gate source voltage response. Constant gate current scales the gate source voltage, a function of time, to a function of coulombs. The value of gate current is chosen so that the device on-state is of the order of 100 µs.

The resulting gate-source voltage waveform is nonlinear and is representative of device behavior in the low to mid-frequency ranges. The slope of the generated response reflects the active device capacitance ($C_g = dQ_g / dV_{GS}$) as it varies during the switching transition. The input characteristic obtained from this test reflects the chip design while avoiding high frequency effects.

b. Figure 3471-1 is the test circuit schematic for testing an n-channel device. Polarities are simply reversed for a p-channel device.

c. Figure 3471-2 is an example of a practical embodiment of figure 3471-1. It illustrates a gate drive and instrument circuit that will test n-channel and p-channel devices.

d. The circuit has I_g programmability ranging from microamperes to milliamperes. For very large power MOSFET devices, the output I_g can be extended to tens of milliamperes by paralleling additional CA3280 devices.

e. The circuit provides an independent gate voltage clamp control to prevent voltage excursions from exceeding test device gate voltage ratings.

f. The CA3240E follower ensures that the smallest power devices will not be loaded by the oscilloscope. (R_{in} = 1.5 T Ω, I_{IN} = 10 pA, C_{IN} = 4 pF).

g. Gate charge is to be measured starting at zero gate voltage to a specified gate voltage value.

h. The magnitude of input step constant gate current I_g should be such that gate propagation and inductive effects are not evident. Typically this means the device on-state should be of the order of 100 µs.

i. The dynamic response, source impedance, and duty factor of the pulsed gate current generator are to be such that they do not materially affect the measurement.

j. Typically, the instrument used for a gate charge measurement is an oscilloscope with an input amplifier and probe. The switching response and probe impedance are to be such that they do not materially affect the measurement. Too low a probe resistance relative to the magnitude of I_g can significantly increase the apparent Q_g for a given V_{GS}. Too high a value of probe capacitance relative to the device C_{iss} will also increase the apparent Q_g for a given V_{GS}.

$$I_g = \frac{C_g \ dV_{GS}}{dt}, \ Q_g = C_g \ V_{GS}.$$

3. Summary. Figure 3471-3 illustrates the waveform and tests 1 through 4, condition A. Figure 3471-4 illustrates the waveform for tests 2, 4, 5, and 6, condition B. Only four of the six tests need be performed since the results of the remaining two are uniquely determined and may be calculated. Either condition A or condition B may be used.

3.1 Condition A.

3.1.1 Test 1, $Q_{g(th)}$.

a. Case temperature (T_C): +25°C.

b. Drain current: $I_D \geq 100$ mA.

c. Off-state drain voltage (V_{DD}): Between 50 percent and 80 percent of the device's rated drain-source breakdown voltage.

d. Load resistor (R_L): Equal to V_{DD}/I_D.

e. Gate current (I_g): Constant gate current such that the transition from off-state to on-state or on-state to off-state is of the order of 50 μs. The value of I_g varies with die size and ranges from 0.1 mA to 5 mA.

f. Gate to source voltage ($V_{g(th)\ min}$): The minimum rated gate-source threshold voltage.

g. Minimum off-state gate charge ($Q_{g(th)}$): A minimum and maximum limit shall be specified.

3.1.2 Test 2, $Q_{g(on)}$.

a. T_C, I_D, V_{DD}, R_L, I_g: Same as test 1 in 3.1.1.

b. V_{GS}: The gate-source voltage specified for the $r_{DS(on)}$ test, $V_{(on)}$.

c. On-state gate charge ($Q_{g(on)}$): A minimum and maximum limit shall be specified.

3.1.3 Test 3, $Q_{gm(on)}$.

a. T_C, I_D, V_{DD}, R_L, I_g: Same as test 1 in 3.1.1.

b. V_{GS}: The maximum rated gate-source voltage, $V_{(max)}$.

c. Maximum on-state gate charge ($Q_{gm(on)}$): A minimum and maximum limit shall be specified.

3.1.4 Test 4, V_{GP}. This test is to be performed on a dc parameter test set.

a. I_D = The continuous rated drain current at T_C = +25°C.

b. $V_{DS} > V_{GS}$. Normally $V_{DD} \approx 3\ V_{GS}$ is satisfactory.

c. The pulse width and duty factor are such that they do not materially affect the measurement.

d. V_{GP} shall be specified as a maximum and minimum.

e. T_C = +25°C.

3.1.5 Test 5, Q_{gs}; test 6, Q_{gd}. No tests are required. The calculations in terms of the results of tests 1 through 4 are as follows:

a. $Q_{gs} = Q_{g(th)} \left[\frac{V_{GP}}{V_{g(th)\min}} \right]$.

b. Determine the fully on-state charge slope:

$$m = \left[\frac{V_{(\max)} - V_{(on)}}{Q_{gm(on)} - Q_{g(on)}} \right]$$

c. Determine the V_{gs} axis intercept:

$$b = V_{(on)} - m\ Q_{g(on)}.$$

d. Calculate Q_{gd}: $Q_{gd} = \left[\frac{(V_{GP} - b)}{m} \right] - Q_{gs}$.

3.2 Condition B.

3.2.1 Test 2, $Q_{g(on)}$.

a. Case temperature (T_C): +25°C.

b. On-state drain current (I_D): The continuous rated drain current at T_C = +25°C.

c. Off-state drain voltage (V_{DD}): Between 50 percent and 80 percent of the device's rated drain-source breakdown voltage.

d. The drain load shall be such that the drain current will remain essentially constant.

e. Gate current (I_g): Same as test 1 in 3.1.1, condition A.

f. Gate to source voltage $V_{(on)}$: Same as test 1 in 3.1.1, condition A.

g. On-state gate charge ($Q_{g(on)}$): A minimum and maximum limit shall be specified.

3.2.2 Test 4, V_{GP}.

a. T_C, I_D, V_{DD}, Load, I_g: Same as test 2 in 3.2.1, condition B.

b. V_{GP}: This is the gate plateau voltage where Q_{gs} and Q_{gd} are measured. This voltage is essentially constant during the drain voltage transition when Q_{gd} is supplied from the gate to the drain under constant I_g, I_D conditions.

3.2.3 Test 5, Q_{gs}.

a. T_C, I_D, V_{DD}, Load, I_g: Same as test 2 in 3.2.1, condition B.

b. V_{GS}: Equal to V_{GP} at the specified I_D.

c. Q_{gs}: A minimum and maximum limit shall be specified.

3.2.4 Test 6, Q_{gd}.

a. T_C, I_D, V_{DD}, Load, I_g: Same as test 2 in 3.2.1, condition B.

b. V_{GS}: Equal to V_{GP} at the specified I_D.

c. Q_{gs}: A minimum and maximum limit shall be specified.

3.2.5 Test 1, $Q_{g(th)}$; test 3, $Q_{gm(on)}$. No tests are required. The calculations in terms of the results of test 2, 4, 5, and 6 are as follows:

a. . $Q_{g(th)} = Q_{gs}\left[\frac{V_{g(th)}\min}{V_{GP}}\right]$.

b. Determine the fully on-state charge slope:

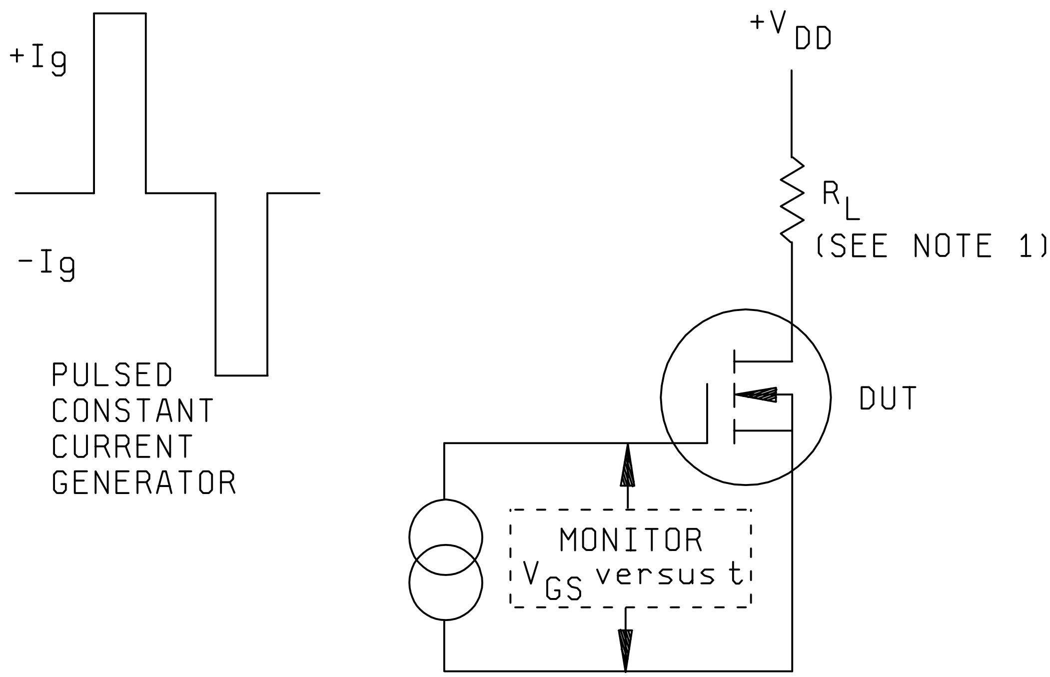
$$m = \left[\frac{V_{(on)} - V_{GP}}{Q_{g(on)} - Q_{gs} - Q_{gd}}\right]$$

c. Determine the V_{gs} axis intercept:

$$b = V_{(on)} - m\ Q_{g(on)}.$$

d. Calculate $Q_{gm(on)}$:

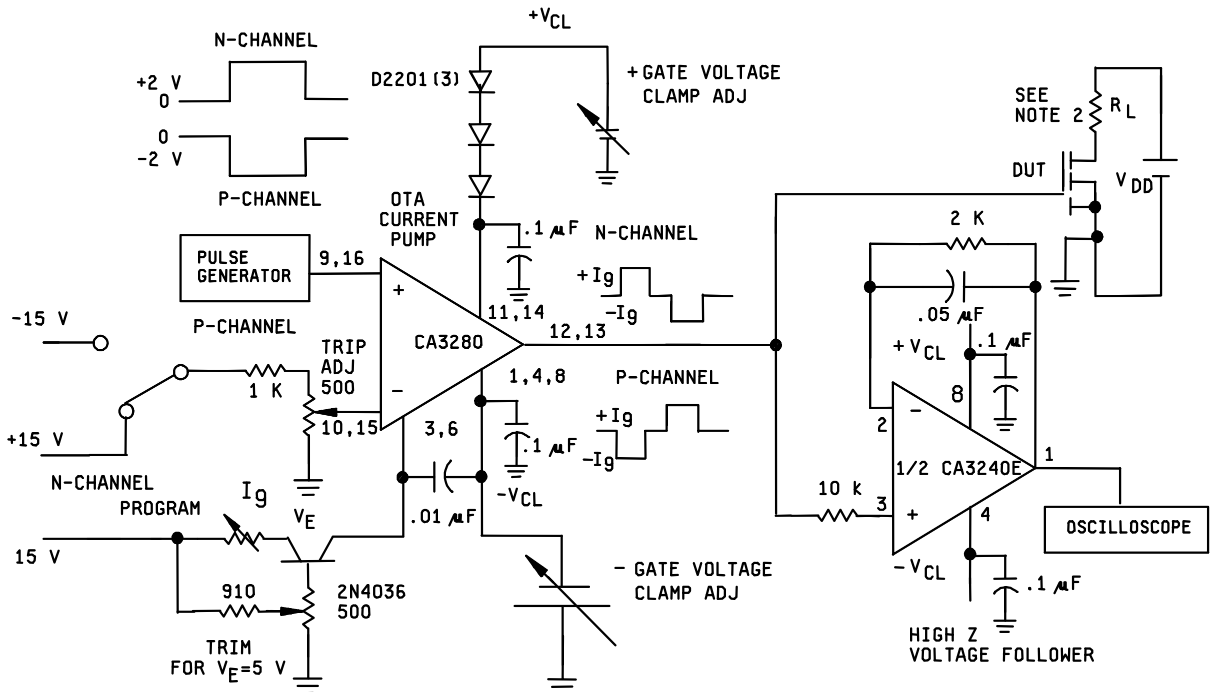
$$Q_{gm(on)} = \frac{[V_{(\max)} - b]}{m}$$



NOTES:

1. Condition B requires a constant drain current regulator.
2. I_g x t = Q_g.

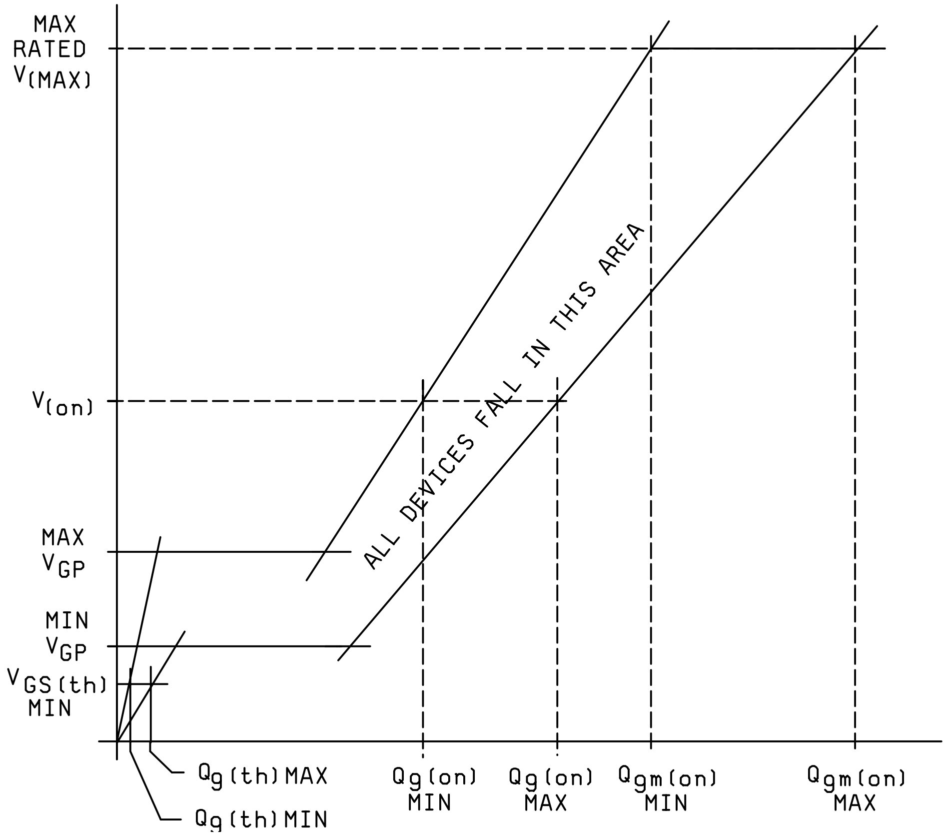
FIGURE 3471-1. Pulsed constant current generator.



NOTES:

1. This test method provides gate voltage as a monotonic function of gate charge. Charge or capacitance may be unambiguously specified at any gate voltage. Gate voltage assuring that the device is well into the on-state will result in very reproducible measurements. For a given device, the gate charges at these voltages are independent of drain current and a weak function of the off-state voltage.
2. Condition B requires a constant current drain regulator.

FIGURE 3471-2. Practical gate charge test circuit.



NOTES:
1. $Q_g = I_g t$.
2. V_{GP} is measured by a dc test, same I_D, $V_{DS} >> V_{GP}$ (see 3.14).
3. $V_{(max)}$ and $V_{(on)}$ are specified voltages for charge measurements $Q_{gm(on)}$ and $Q_{g(on)}$.
4. $V_{GS(th)}$ min is a specified voltage for measuring $Q_{g(th)}$.

FIGURE 3471-3. Gate charge characterization showing measured characteristics.

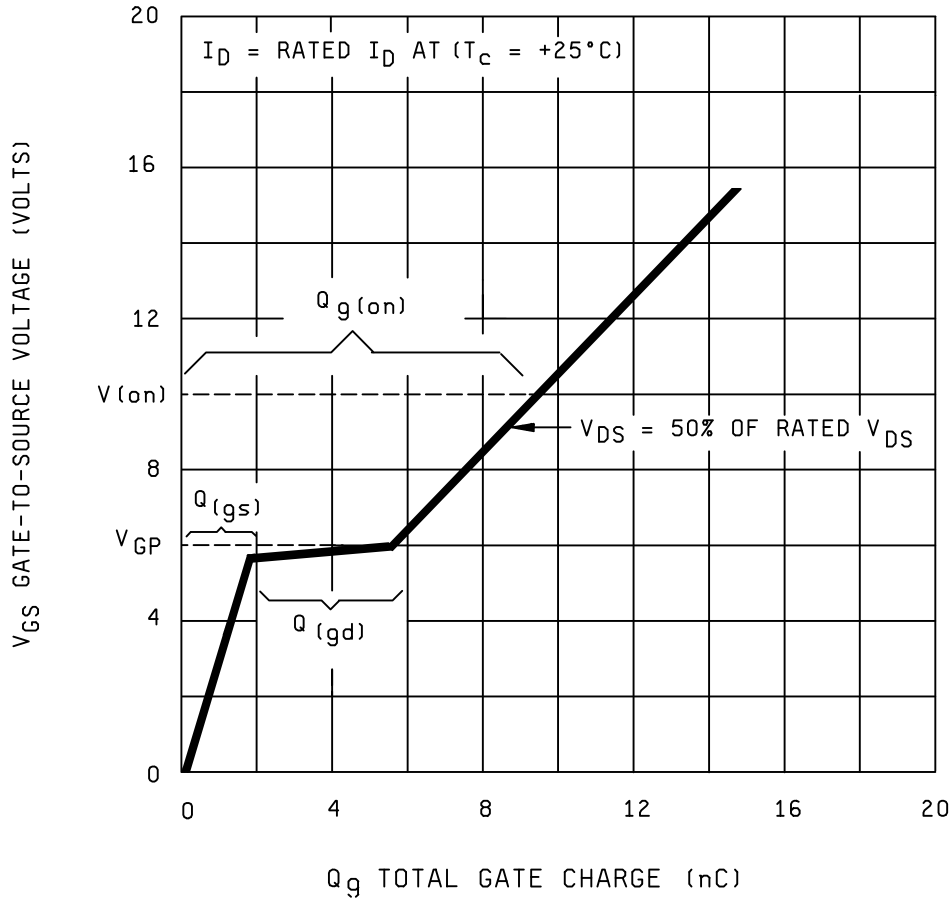


FIGURE 3471-4. Gate charge, condition B.

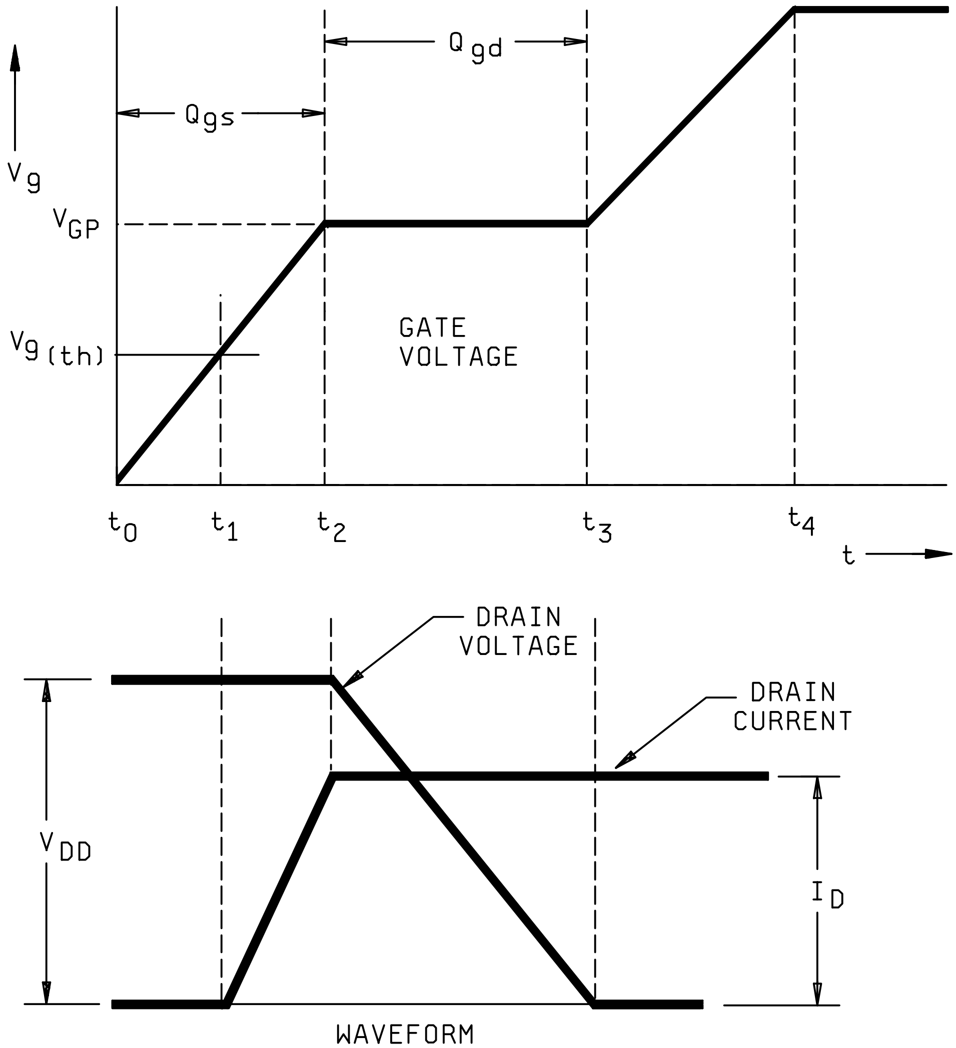


FIGURE 3471-5. Idealized gate charge waveforms, condition B.

METHOD 3472.1

SWITCHING TIME TEST

1. Purpose. The purpose of this test is to measure the pulse response ($t_{d(on)}$, t_r, $t_{d(off)}$, t_f) of power MOSFET or IGBT devices under specified conditions. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test procedure. Monitor V_{GS} and V_{DS} versus time using the following notes and precautions. Refer to figures 3472-1 through 3472-4 for clarification.

2.1 Notes and precautions.

a. This method presumes that good engineering practice will be employed in the physical construction of the test circuit, i.e., short leads, good ground plane, minimum gate to drain mutual inductance, and appropriate high speed generators and instruments.

b. The value of R_{GS} or R_{GE} includes instrumentation resistive loading. R_{GEN} and R_{GS} R_{GE} should be low enough in value that gate propagation effects are evident.

c. The value of L_{DST} or L_{CET}, C_{GST} or C_{GET}, and C_{DST} or C_{CET} are understood to include those of the test fixture, circuit elements, instrumentation; and any added values, exclusive of the DUT. L_{DST} or L_{CET} shall not exceed 100 nH nor shall (C_{DST} or C_{CET}) or (C_{GST} or C_{GET}) exceed 100 pF. Devices with small die may need smaller values of L_{DST} or L_{CET}, C_{DST} or C_{CET}, and C_{GST} or C_{GET}. L_{DST}, C_{DST}, and C_{GST} need not be measured when using figure 3472-3 and figure 3472-4. When $r_{CS(on)}$ or $r_{DS(on)}$ is measured at a V_{GS} or V_{GE} of less than 10 V, then figure 3472-3 and figure 3472-4 do not apply.

d. Gate circuit inductance need not be specified. With the DUT removed, the gate-source voltage waveform should be free of anomalies that could materially affect the measurement. Inductance is difficult to measure accurately in a well designed test fixture. The gate drive common should be Kelvin connected to the device source lead.

e. Passive circuit elements referred to in this method are lumped parameter representations whose values would be those obtained through the use of an RLC bridge using a 1 MHz test frequency.

f. Voltage and current sources are to be interpreted as effective idealizations of active elements.

g. The phrase "affect the measurement" is intended to mean that doubling a value will not affect results greater than the precision of measurement.

h. The turn-off drain voltage overshoot should not be allowed to exceed the device rated drain-source breakdown voltage. Drain circuit ringing begins when the inductive time constant is 25 percent of the capacitive time constant. Ringing is particularly serious when testing low voltage high current devices at high speeds. When the ratio $L_{DST}/R^2{}_L(C_{DST} + C_{OSS})$ exceeds 10, test conditions may have to be adjusted to ensure that device breakdown is not reached.

i. The instrument used for switching parameter measurement is an oscilloscope with input amplifiers and probes. The affect on rise and fall times can be estimated by the following relationship:

$$(\text{measurement rise time})^2 = (\text{actual rise time})^2 + (\text{amplifier rise time})^2 + (\text{probe rise time})^2$$

j. When two channels with probes are involved in a measurement (turn-on and turn-off delays), the relative channel probe delays should not materially affect the measurement. Simultaneous viewing the same waveform using the two channel/probes is an effective means of estimating errors.

k. Unless otherwise specified, half rated drain voltage and rated drain current are mandatory conditions for measuring switching parameters.

l. When measuring rise time, $V_{GS(on)}$ shall be as specified on the input waveform. When measuring fall time $V_{GS(off)}$ shall be specified on the input waveform. The input transition and drain voltage response detector shall have rise and fall response times such that doubling these responses will not affect the results greater than the precision of measurement. The current shall be sufficiently small so that doubling it does not affect test results greater than the precision of measurement.

3. Test circuit and waveform: See figures 3472-1, 3472-2, 3472-3, and tables 3472-I and 3472-II.

TABLE 3472-1. Switching time circuit parts list.

Part	No.	Value or size	Manufacturer	PIN
On-board supply	1	15 volts	Datel	UPM 15/100-A
Voltage regulator	1	TO-220 package	National	LM317
Timer	1	8-pin DIP package	National	LM555
Drivers	1	50 V, Hex1, p-channel	I.R.C.	IRFD9010
	1	100 V, Hexz, n-channel	I.R.C.	IRFD1ZO
	2	50 V, Hex2, p-channel	I.R.C.	IRFD9020
	2	50 V, Hex2, n-channel	I.R.C.	IRFD020
Resistors 1/	2	4.95 KΩ, .25 W, ±1 percent	Dale	CMF604951FT0
	1	220 Ω, 0.5 W, ±1 percent	Dale	CMF602200FT0
	1	5 KΩ variable	Dale	724, 5 K, ±10 percent
	1	2.2 MΩ, .25 W, ±1 percent	Dale	CMF602204FT0
	1	360 Ω, .25 W, ±1 percent	Dale	CMF603600FT0
	1	100 Ω, .25 W, ±1 percent	Dale	CMF601000FT0
Capacitors	14	1 μF, 50 V, ±10 percent	Mallory	M30R105K5
	10	.82 μF, 600 V, ±10 percent	CRC	B55F824KXC
	7	.15 μF, 50 V, ±10 percent	Mallory	M30R154K5
	4	.01 μF, 50 V, ±10 percent	Mallory	M10R103K5
	2	22 pF, 600 V, ±5 percent	AVX	AQ14BG220JU
	1	100 pF, 100 V, ±10 percent	Sprague	TST10
	1	100 μF, 450 V, -10 percent, +5 percent	Sprague	53D101F450JS6
	1	.01 μF, 600 V, ±5 percent	Sprague	715P10356KD3
DUT socket	1	TO-3	Loranger	3128-032-4225
BNC	3	PC board mount	Pomona Elect.	4578
Transformer	1	Torroidal core	Micrometals	T5-12
Banana plugs	2	Standard uninsulated	Pomona	3267
Circuit board 2/	1	10.5" x 7.50"		

1/ All resistors are metal-film.
2/ .062 inch (1.57 mm) double-sided board with 3 ounces copper and 60/40 tin-lead of .0003 inch (0.008 mm) thickness.

TABLE 3472-2. Switching time circuit, component layout list. 1/ 2/

Label	Component	Value
R1	Resistor	220 Ω
R2	Variable resistor	5 KΩ
R3	Resistor	2.2 MΩ
R4	Resistor	360 Ω
R5	Resistor	100 Ω
R6	Gate resistor	Varies
R7	Drain resistor	Varies
C1, C2, C4, C26	Capacitor 50 V	.01 μF
C3-C10, C12, C14	Capacitor	1 μF
C16, C18, C20, C22	Capacitor	1 μF
C11, C13, C15, C17	Capacitor	.15 μF
C19, C21, C23	Capacitor	.15 μF
C25	Capacitor	100 pF
C27, C29	Capacitor	22 pF
C28	Capacitor 600 V	.01 μF
C30	Capacitor	100 μF
C31-C40	Capacitor	.82 μF
Q1	MOSFET (4 pin DIP)	IRFD9010
Q2, Q3	MOSFET (4 pin DIP)	IRFD9020
Q4	MOSFET (4 pin DIP)	IRFD1ZO
Q5, Q6	MOSFET (4 pin DIP)	IRFD020
Q7	Regulator (TO220)	LM317
Q8	Timer (8-pin DIP)	LM555
T1	Iso. transformer	T5-12

1/ Figure 3472-3 board layout is an artist's view for an n-channel TO-3 package. The following companies will provide the circuit boards or a drawing of the exact board layout for a TO-3 as well as other packages such as the TO-39, TO-61, and TO-66:

a. Integrated Technology Corporation
1228 N. Stadem Drive
Tempe, AZ 85281

b. TEC
9800 Vesper Avenue
Unit 28
Panorama City, CA 91402

2/ L_{DST}, C_{DST}, and C_{GST} need not be measured when using these circuit boards derived from figures 3472-3 and 3472-4.

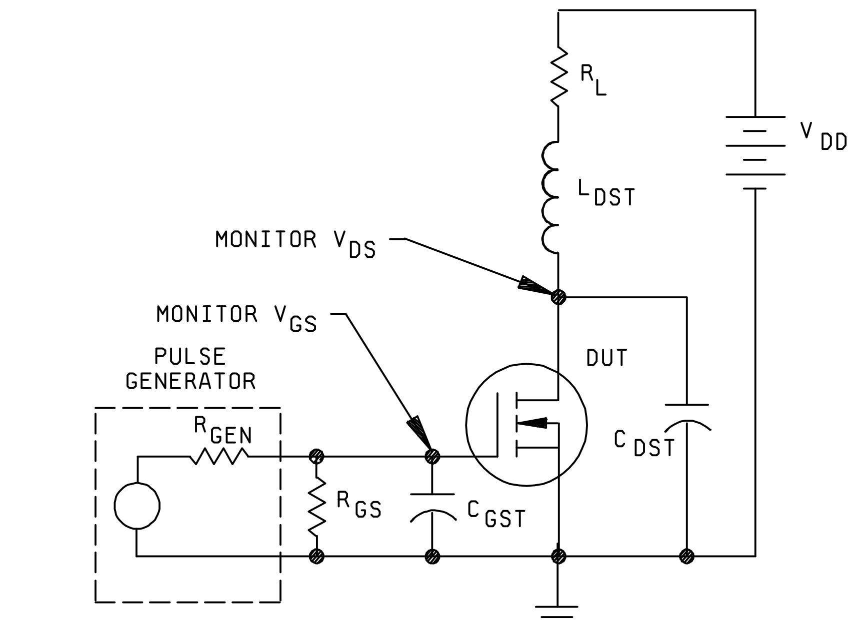


FIGURE 3472-1. Switching time test circuit.

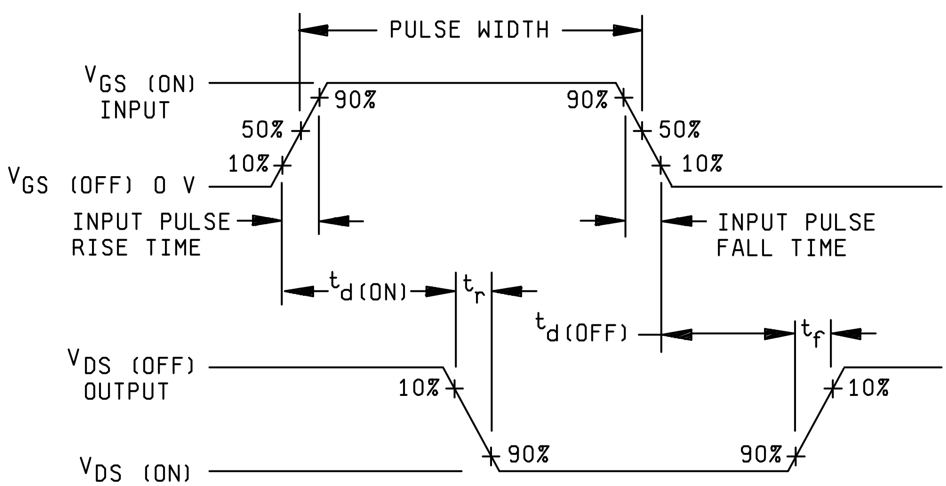


FIGURE 3472-2. Switching time waveforms.

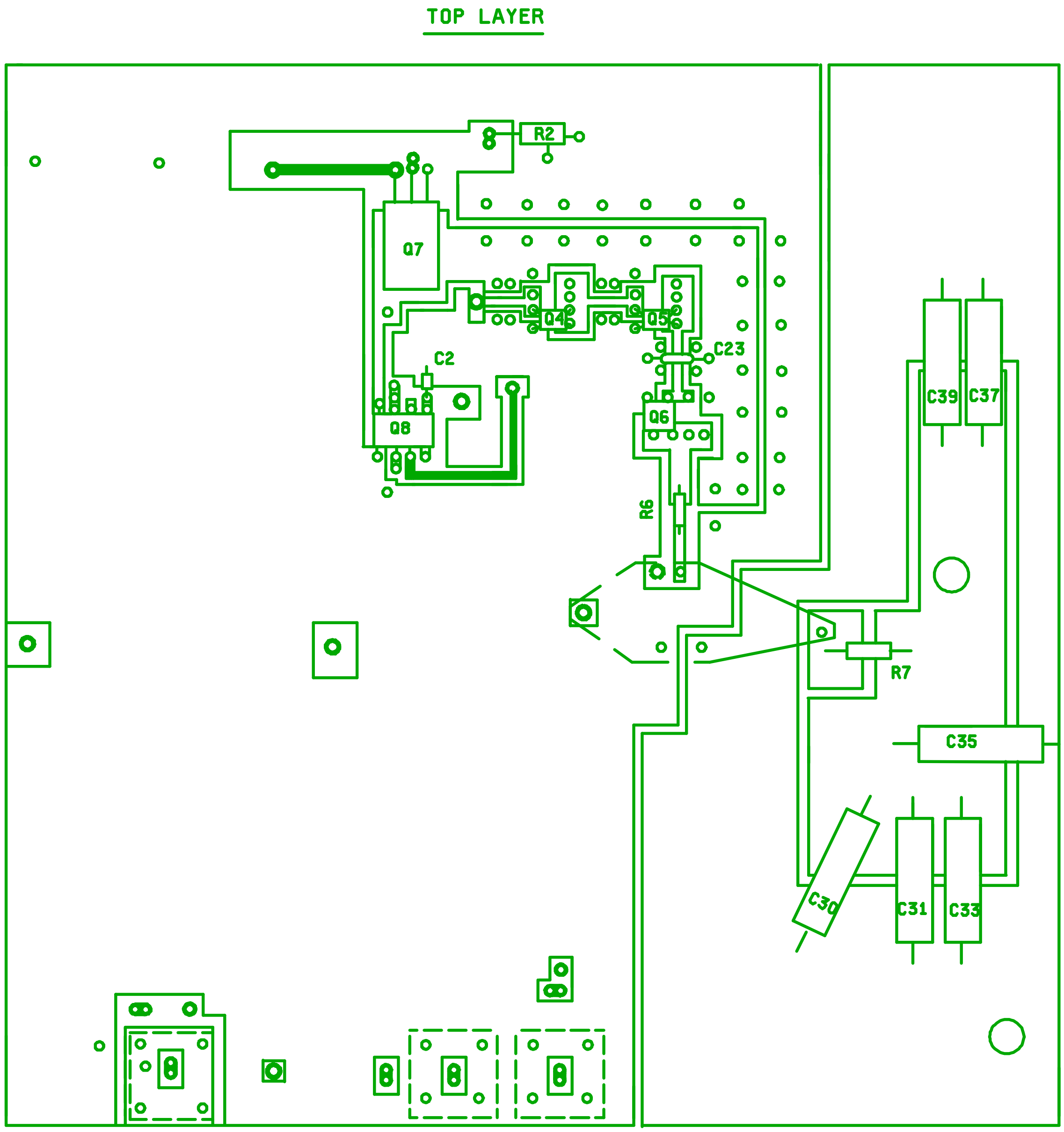


FIGURE 3472-3. Board layout.

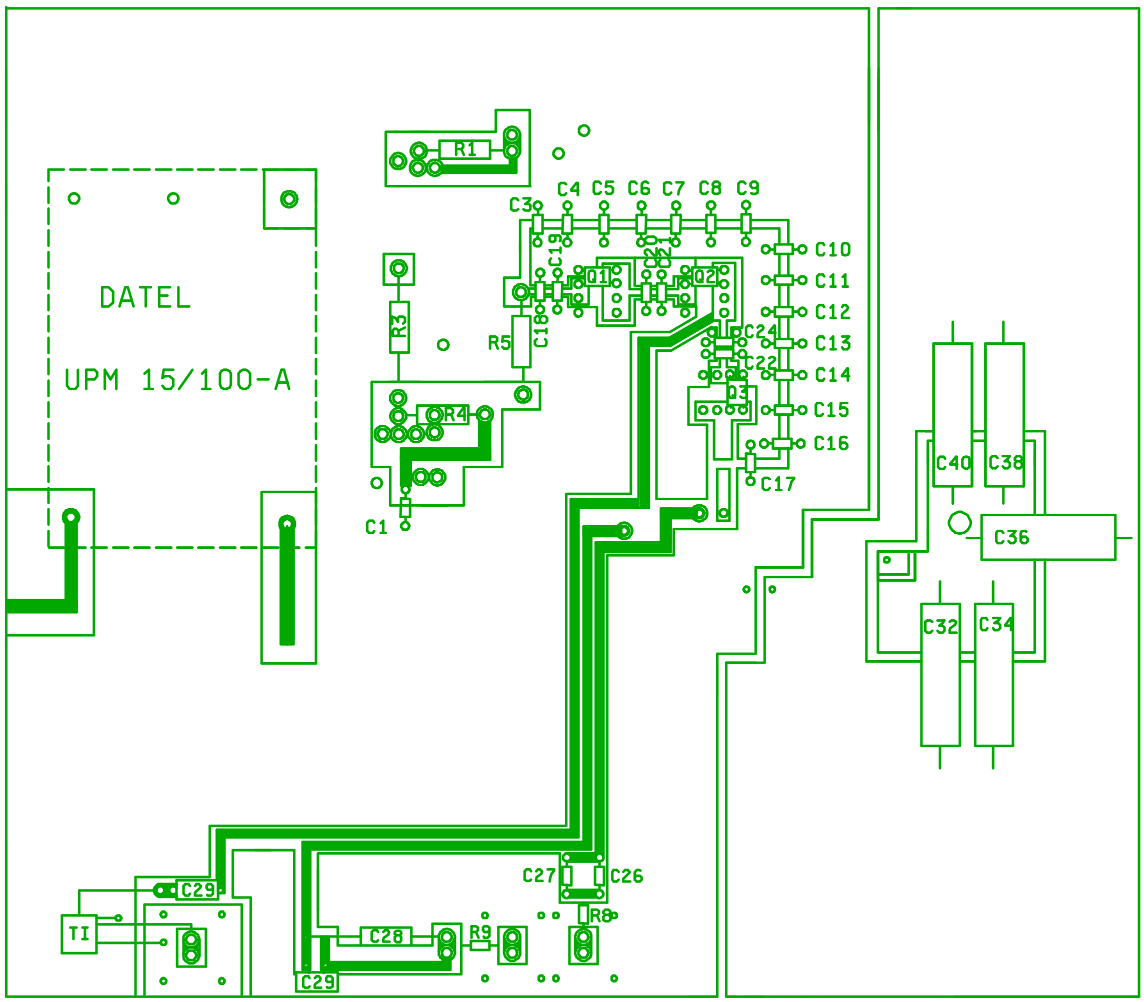


FIGURE 3472-3. Board layout - Continued.

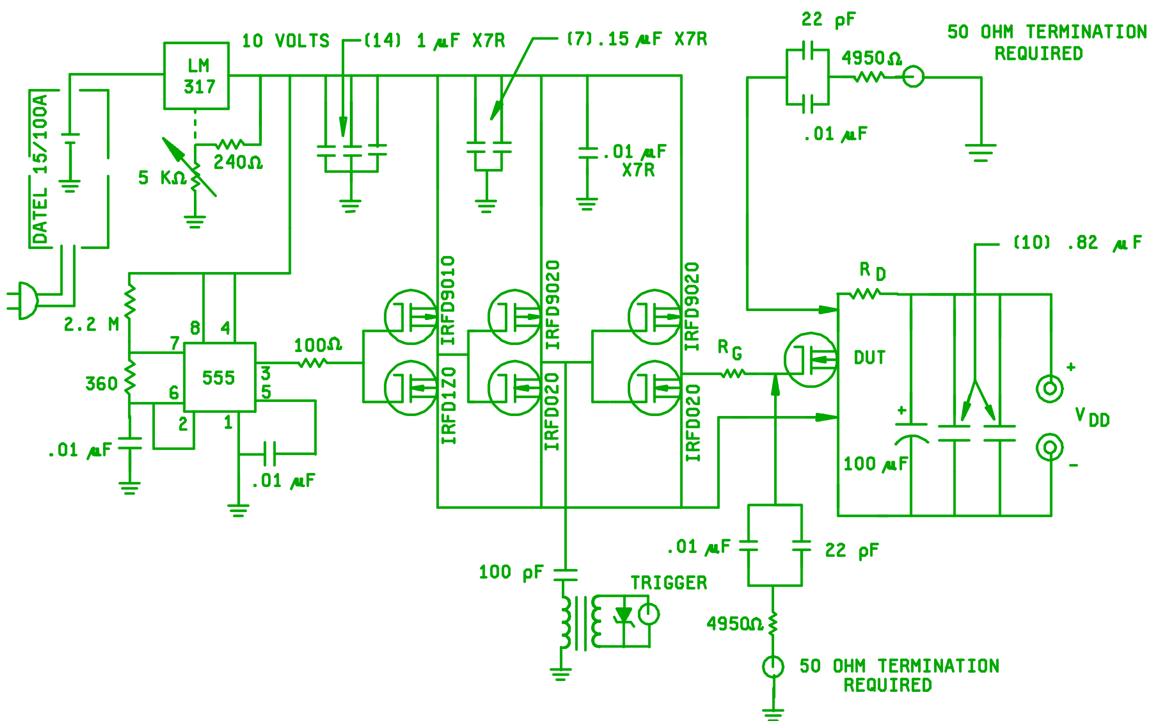


FIGURE 3472-4. Stand alone switching circuit.

4. Summary. The following conditions shall be specified in the detail specification:

a. T_C: Unless otherwise specified, case temperature = +25°C.

b. I_D: On-state drain current (see 4.1.a.).

c. V_{DD}: Off-state drain voltage (see 4.1.a. and 4.1.b.).

d. R_L: Nominally equal to V_{DD}/I_D (see 4.1.b.).

e. V_{GS}: On-state gate voltage (see 4.1.c.).

f. R_{GS}: Gate to source resistance.

g. R_{GEN}: Resistance looking back into the generator.

METHOD 3473.1

REVERSE RECOVERY TIME (t_{rr}) AND RECOVERED CHARGE (Q_{rr})
FOR POWER MOSFET (DRAIN-TO-SOURCE) AND POWER RECTIFIERS WITH $t_{rr} \leq 100$ ns

1. Purpose. The purpose of this test is to determine the time required for the DUT to switch off when a reverse bias is applied after the DUT has been forward biased and to determine the charge recovered under the same conditions.

2. Test conditions.

2.1 Test condition A, reverse recovery time (t_{rr}). Monitor diode current versus time. If the DUT is a power MOSFET, the gate lead must be shorted to the source lead. Use the following notes and precautions as a guide. Refer to figures 3473-1 through 3473-3 for clarification.

2.1.1 Notes and precautions.

a. This method presumes that good engineering practice will be employed in the construction of the test circuit, i.e., short leads, good ground plane, minimum inductance of the measuring loop, and minimum self-inductance (L_1) of the current sampling resistor (R_4). Also, appropriate high speed generators and instruments.

b. The measuring-loop inductance (L_{LOOP}, see figure 3473-1) represents the net effect of all inductive elements, whether lumped or distributed, i.e., bonding wires, test fixture, circuit board foil, inductance of energy storage capacitors. The value of L_{LOOP} should be 100 nH or less. The reason for controlling this circuit parameter is that it, combined with diode characteristics, determines the value of t_b.

c. The turn-off reverse-voltage overshoot shall not be allowed to exceed the device rated breakdown voltage. Ringing and overshoot may become a problem with $R_{LOOP} < 2(L/C)^{1/2}$; where $L = L_{LOOP}$. That is another reason for minimizing L_{LOOP}.

d. Regarding breakdown voltage, $-V_4$ should be kept as specified.

e. The self-inductance of the current-sample resistor R_4 (see figure 3473-1) must be kept low relative to t_a because the observed values of t_a and I_{RM} increase with increasing self-inductance. Since the value of R_4 is not specified, the recommended maximum inductance is expressed as a time constant (L_1/R_4) with a maximum value of t_a(minimum)/10, where t_a(minimum) is the lowest t_a value to be measured. This ratio was chosen as a practical compromise and would yield an observed t_a which is 10 percent high ($\Delta t_a = L_1/R_4$). The I_{RM} error is a function of the L_1/R_4 time constant and di/dt. For a di/dt of 100A/µs the observed I_{RM} would also be 10 percent high. $\Delta I_{RM} = L_1/R_4$ di/dt.

f. The di/dt of 100A/µs was chosen so as to provide reasonably high signal levels and still not introduce the large I_{RM} errors caused by higher di/dt.

g. The forward current (I_F) used for this test shall be as specified at T = +25°C.

h. The values of t_a, t_b, and I_{RM} are to be measured and recorded separately. $t_{rr} = t_a + t_b$.

i. The forward current value must be specified, otherwise the t_a and I_{RM} values have little useful meaning.

j. The forward current generator consisting of Q_1, Q_2, R_1, and R_2 may be replaced with any functionally equivalent circuit. Likewise the current-ramp generator consisting of Q_3, Q_4, R_3, and C_1.

2.2 Condition B, reverse recovered charge (Q_{rr}). This method is direct reading and therefore does not require an oscilloscope. Use the following notes and precautions as a guide. Refer to figures 3473-4 and 3473-5 for clarification.

2.2.1 Notes and precautions.

a. This method presumes that good engineering practice will be employed in the construction of the test circuit, i.e., short leads, good ground plane, minimum inductance of the measuring loop. Also, appropriate high speed generators and instruments.

b. The measuring-loop inductance (L_{LOOP}, see figure 3473-4) represents the net affect of all inductive elements in the loop, whether lumped or distributed, i.e., DUT bonding wires, test fixture, circuit board foil, inductive component of energy storage capacitors. The value of L_{LOOP} should be 100 nH or less.

c. The turn-off reverse-voltage overshoot shall not be allowed to exceed the device rated breakdown voltage. Ringing and overshoot may become a problem when $R_{LOOP} < 2(L/C)^{1/2}$; where $L = L_{LOOP}$.

d. Regarding breakdown voltage, $-V_4$ should be kept as specified.

e. The di/dt of 100A/µs was chosen as a compromise between having reasonably high signal levels for the faster devices and the need to keep the reverse voltage as low as possible. Higher di/dt requires a higher reverse voltage to overcome the drop across L_{LOOP}.

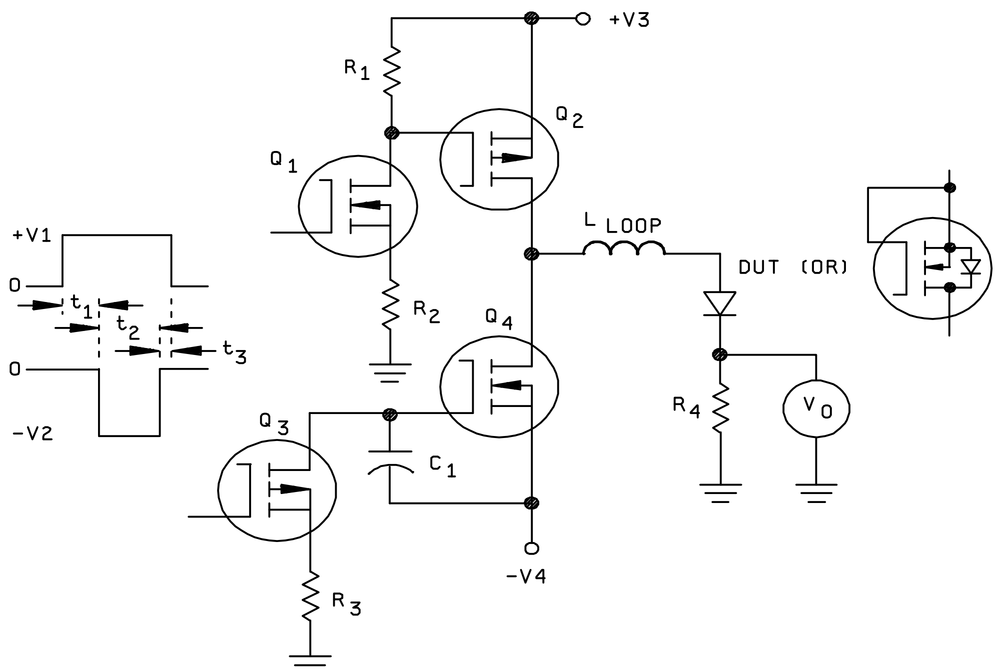
f. The forward current (I_F) used for this test shall be as specified at +25°C.

g. The capacitor C_2 (see figure 3473-4) shall be large enough so that there is no appreciable voltage drop across it. Reducing its value by 50 percent shall not change the reading by more than the required measurement accuracy.

h. The current meter across C_2 should have as low a resistance as possible. Doubling the resistance shall not change the reading by more than the required measurement accuracy. A good compromise would be a digital ammeter with a full scale drop of 0.2 volt. If the reverse bias supply is 30 volts, the maximum meter potential differences is then less than one percent of supply voltage.

i. The recommended pulse repetition rate is 1 kHz ±5 percent.

j. The forward current generator consisting of Q_1, Q_2, R_1, and R_2 may be replaced by any functionally equivalent circuit. Likewise the reverse current-ramp generator consisting of Q_3, Q_4, R_3, and C_1.



$t_1 >= 5\ t_a$ (max)
$t_2 > t_{rr}$
$t_3 > 0$

$$\frac{L_1}{R_4} <= \frac{t_a(\min)}{10}$$

NOTES:

1. V1 amplitude controls forward current (I_f).
2. V2 amplitude controls di/dt.
3. L_1 is self inductance of R_4.
4. t_a (max) is longest t_a to be measured.
5. t_a (min) is shortest t_a to be measured.

FIGURE 3473-1. t_{rr} test circuit.

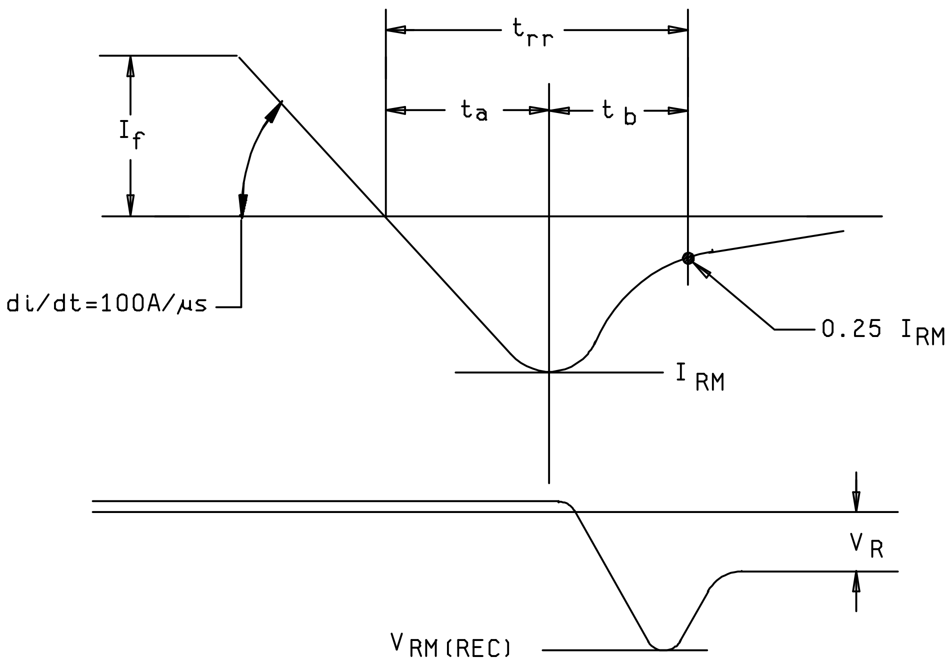


FIGURE 3473-2. Generalized reverse recovery waveforms.

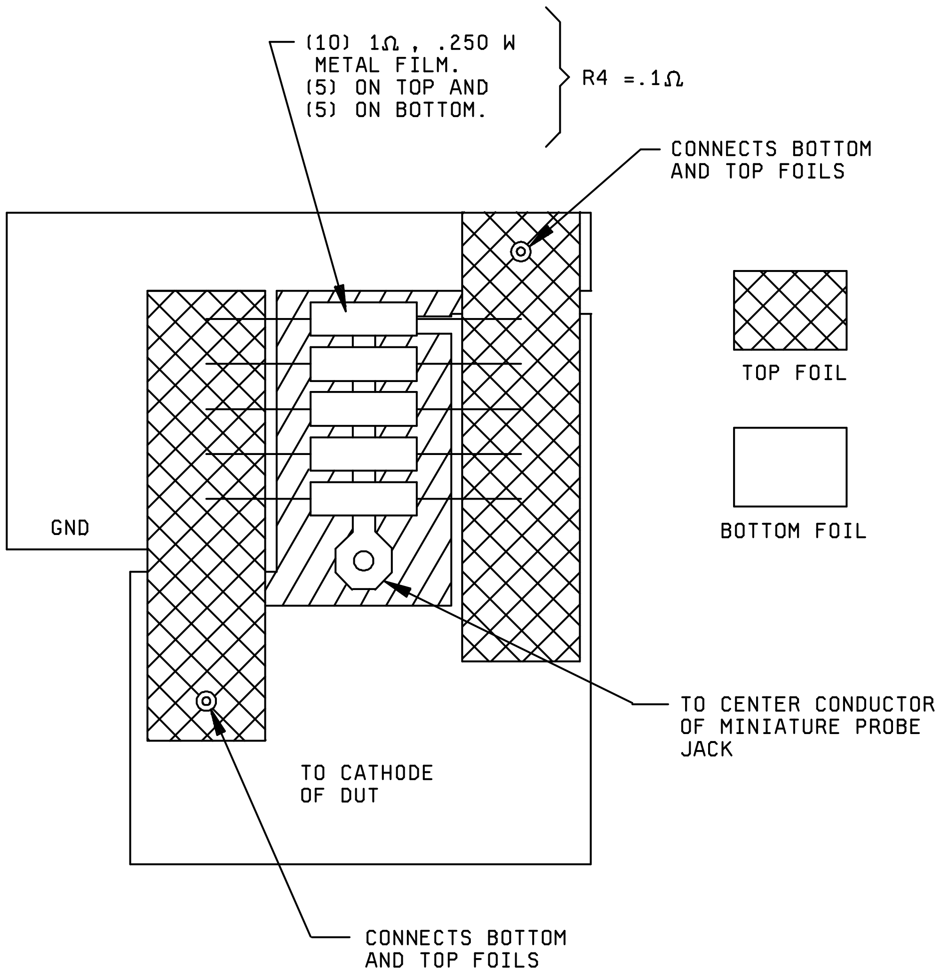
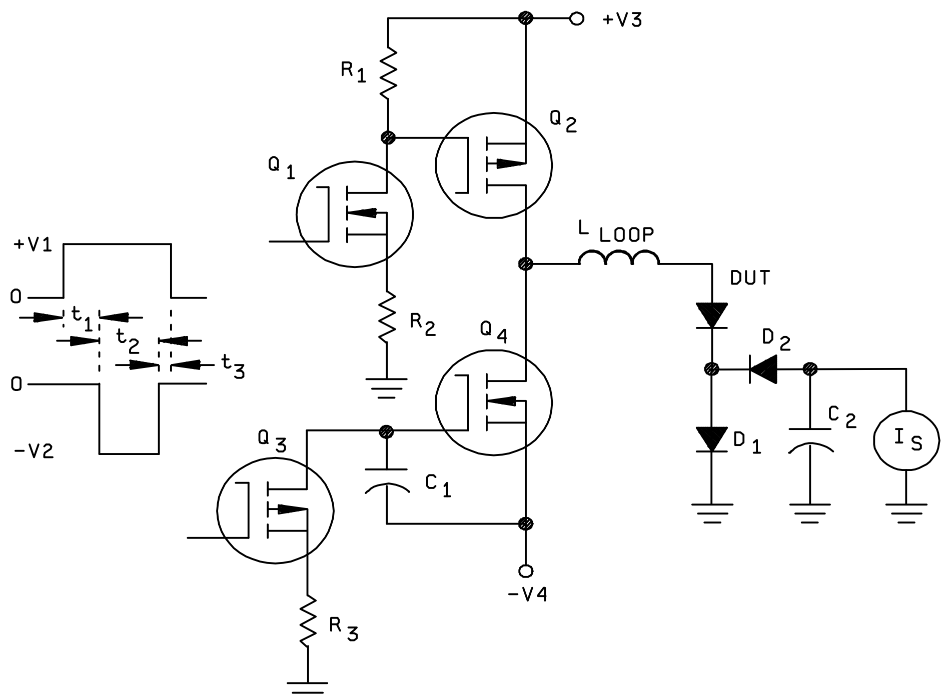


FIGURE 3473-3. Suggested board layout for low L_1 /R_4.

Bottom resistor current flow is in opposite direction of top resistor current flow, providing magnetic field cancellation. Sense lead to center conductor of probe jack exits at right angle to resistor axes and is located between the resistor layers; five on top layer and five on bottom layer.



NOTES:
1. D_1 provides forward current path to ground.
2. D_2 steers reverse signal current into integrating capacitor (C_2).
3. V1 amplitude controls forward current (I_f).
4. V2 amplitude controls di/dt.
5. t_1 > = 5 t_a (max); t_a (max) is the highest t_a to be measured.
6. $t_2 > t_{rr}$.
7. $t_3 > 0$.
8. D1 is a low voltage Schottky rectifier.
9. D2 must have a much lower recovered charge than the value being measured.
10. $Q_{rr} = I_S$ PRR; where PRR is pulse repetition rate.
11. di/dt = 100 A/µs.

FIGURE 3473-4. Q_{rr} test circuit.

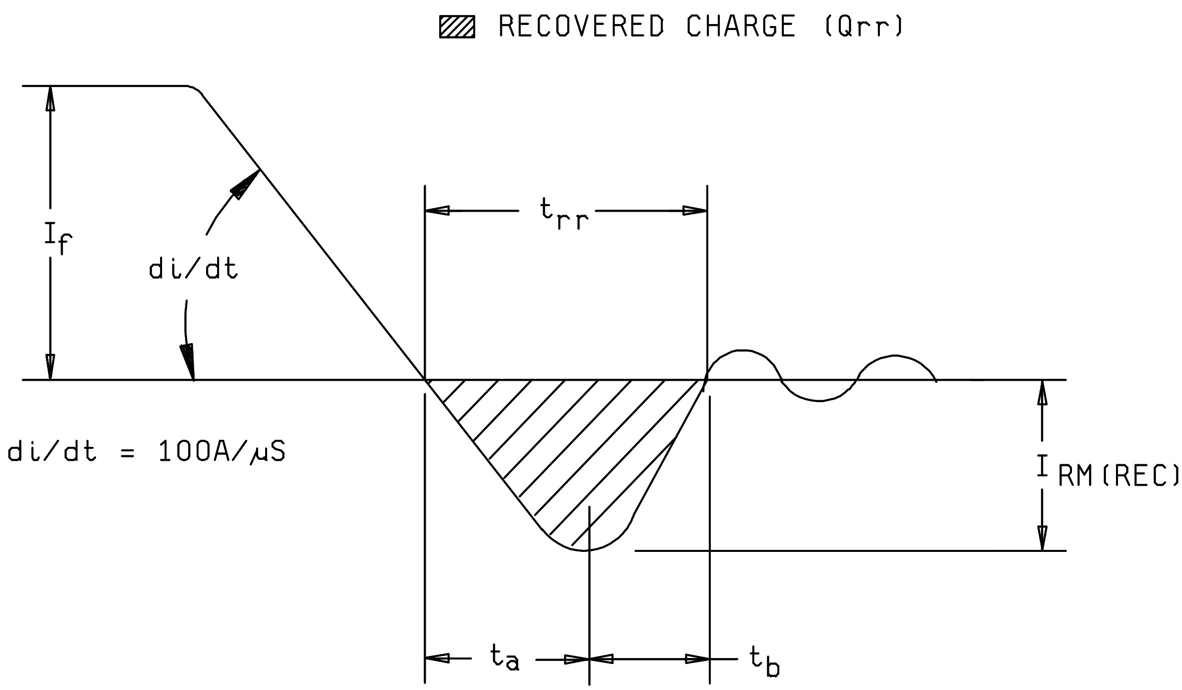


FIGURE 3473-5. Typical t_{rr} waveform (for mnemonic reference only).

3. Summary. Unless otherwise specified in the detail specification, the following conditions shall be:

a. T_C: Case temperature = +25°C.

b. I_F: As specified at +25°C.

c. di/dt: 100A/µs.

d. $-V_4$: Reverse-ramp power supply voltage.

e. V_{DD}: As specified.

METHOD 3474.1

SAFE OPERATING AREA FOR POWER MOSFET's OR INSULATED GATE BIPOLAR TRANSISTORS

1. Purpose. The purpose of this test is to verify the boundary of the SOA as constituted by the interdependency of the specified voltage, current, power, and temperature in a temperature stable circuit. Deliberate consideration is given to the problem of unavoidable case temperature rise during the test. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

1.1 Definitions:

a. P_D: Test power dissipation (watts).

b. D_F: Linear derating factor (W/°C).

c. I_D: Test current (amperes).

d. V_{DD}: Test power supply voltage (volts).

e. V_{DS}: Drain to source voltage (volts).

f. T_J: Junction temperature (°C).

g. T_{JM}: Maximum rated junction temperature (°C).

h. T_C: Case temperature (°C).

i. t_p: Test pulse duration (seconds).

j. P_{DM}: Maximum rated power dissipation (watts).

k. T_{CR}: Rated SOA case temperature (°C).

l. T_A: Ambient temperature (°C).

m. T_S: Heat sink temperature (°C).

n. $R_{\theta JC}$: Junction to case thermal resistance (K/watt).

o. $R_{\theta CS}$: Case to heat sink thermal resistance (K/watt).

p. $R_{\theta SA}$: Heat sink to ambient thermal resistance (K/watt).

2. Test circuit. See figure 3474-1. Circuit polarities shall be reversed for p-channel devices.

a. R_S shall be a Kelvin contact resistor of five percent tolerance.

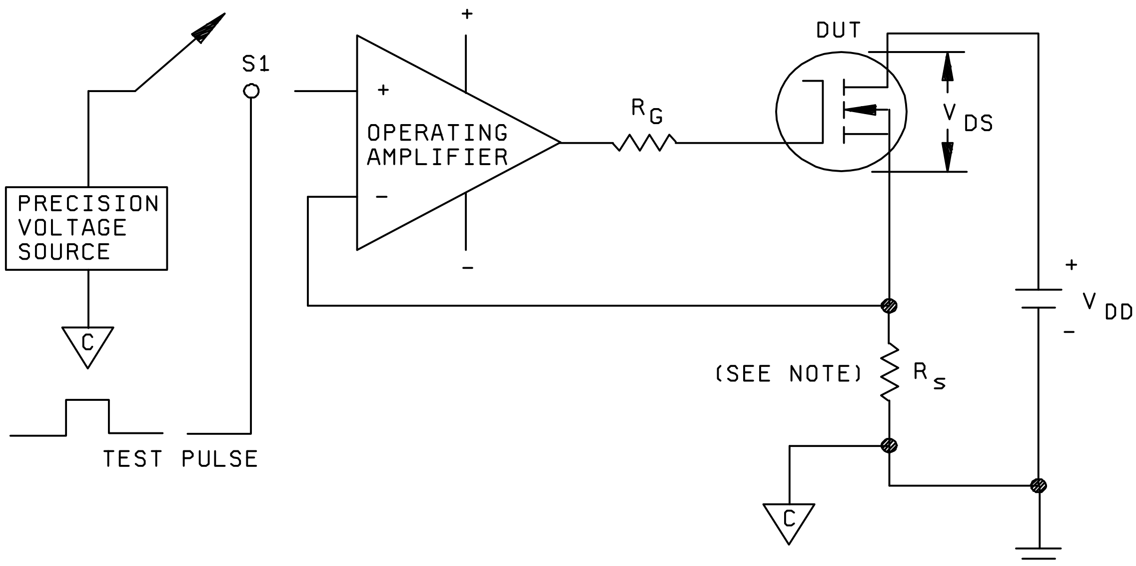
b. Operational amplifier shall have a speed and accuracy such that the errors it produces will contribute less than a five percent error to the measurement.

c. Precision voltage source shall have an accuracy of five percent.

d. S1 shall have adequate speed and characteristics such that the accuracy of the measurement will not be affected by more than five percent.

e. V_{DD} shall be maintained to within five percent.

f. t_p shall be maintained to within five percent.



NOTE: Low inductance resistor.

FIGURE 3474-1. SOA test circuit.

g. Total test accuracy shall be maintained to within 10 percent.

h. R_G shall be selected to eliminate parasitic oscillations.

3. Procedure. Set the precision voltage source to I_D x R_S. Applied V_{DD} to the circuit. Close S1 for t_p seconds.

4. Summary. Just like in any practical application, the junction temperature during an SOA test can be calculated by adding all of the temperature drops in the system to the ambient temperature:

$R_S \leq$ (Maximum rated gate voltage) I_D not to exceed (.2 x maximum rated V_{DS})/I_D
$T_J = T_A + \Delta$sink to ambient + Δcase to sink + Δjunction to case

$$I_D = \frac{(P_{DM} - (T_C - T_{CR}) \times D_F)}{V_{DS}}$$

Under a controlled set of conditions, such as those that are encountered in an SOA test, the case temperature can be measured and therefore known as a constant. This simplifies the expression substantially:

$T_J = T_C + \Delta$junction to case
$T_J = T_C + P_D \times R_{\theta JC}$

By substituting in the maximum rated junction temperature and rearranging the terms, the maximum power dissipation for this condition can be calculated:

$$P_D \; \frac{(T_{JM} - T_C)}{R_{\theta JC}}$$

If a case temperature of T_{CR}°C was chosen for the purpose of specifying the device SOA, then a derating factor "D_F" can be determined:

$$D_F = \frac{P_{DM}}{(T_{JM} - T_{CR})}$$

P_{DM} can be any P_{DM} from the SOA curves for that particular device type, either dc or pulsed. The maximum power dissipation for any case temperature can now be readily calculated and used in an SOA test

$P_D = P_{DM} - (T_C - T_{CR}) \times D_F$

Unless otherwise specified in the detail specification, the following conditions shall apply:

a. V_{DS} = as specified.

b. I_D = as calculated above.

c. +20°C $\leq T_C \leq$ +45°C.

d. t_p shall be that which corresponds with the SOA curve being used.

e. $D_F = \frac{P_{DM}}{(T_{JM} - T_{CR})}$.

f. R_S = as calculated above.

g. P_{DM} shall be a value chosen from one of the SOA curves for that particular device either dc or pulsed.

h. $V_{DD} = V_{DS} + I_D \times R_S$.

METHOD 3475.1

FORWARD TRANSCONDUCTANCE (PULSED DC METHOD) OF POWER MOSFET's OR INSULATED GATE BIPOLAR TRANSISTORS

1. Purpose. This method establishes a basic test circuit for the purpose of establishing forward transconductance (g_{FS}) using pulsed dc for the test conditions to enable measurements above the small signal (g_{FS}) output current levels. The described method is adaptable to ATE where large ac test currents are often impractical. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Procedure. The gate-source voltage (V_{GS1}) is applied as necessary to achieve a specified drain-source current. I_{D1} shall be five percent minimum less than the value of I_D used in specifying $r_{DS(on)}$ (normally 50 percent of rated dc current). The gate-source voltage (V_{GS1}) is then decreased to achieve a second drain-source current (I_{D2}). I_{D2} shall be five percent minimum below the I_{D1} used in specifying $r_{DS(on)}$. The drain-source voltage (V_{GS2})shall remain equal to the value specified for establishing I_{D2}.

Calculation:

$$g_{FS} = \frac{I_{D1} - I_{D2}}{\Delta V_{GS}}$$

Where: $\Delta V_{GS} = V_{GS1} - V_{GS2}$

NOTE: ΔV_{GS} should not be set lower than 0.05 volt or test equipment accuracy can adversely effect measurement. I_{D1} and I_{D2} can be adjusted such that ΔV_{GS} is $\geq$ 0.1 volt. In all cases I_{D1} and I_{D2} should be adjusted so they are equally above and below specified current. The formula below can be used as initial reference point:

If:

$$\Delta V_{GS} = \frac{I_{D1} - I_{D2}}{G_{FS}}$$

then:

$$\frac{I_{D1} - I_{D2}}{2} = \Delta I_D \textit{ desired}$$

The previous calculations can be used in establishing minimum ΔV_{GS} desired to achieve highest accuracy.

3. Test circuit. See figure 3475-1.

4. Summary. Unless otherwise specified in the detail specification, the following conditions shall apply:

a. I_{D1} = 0.5 I_D continuous at T_C = +25°C x 1.05 minimum.

b. I_{D2} = 0.5 I_D continuous at T_C = +25°C x 0.95 minimum.

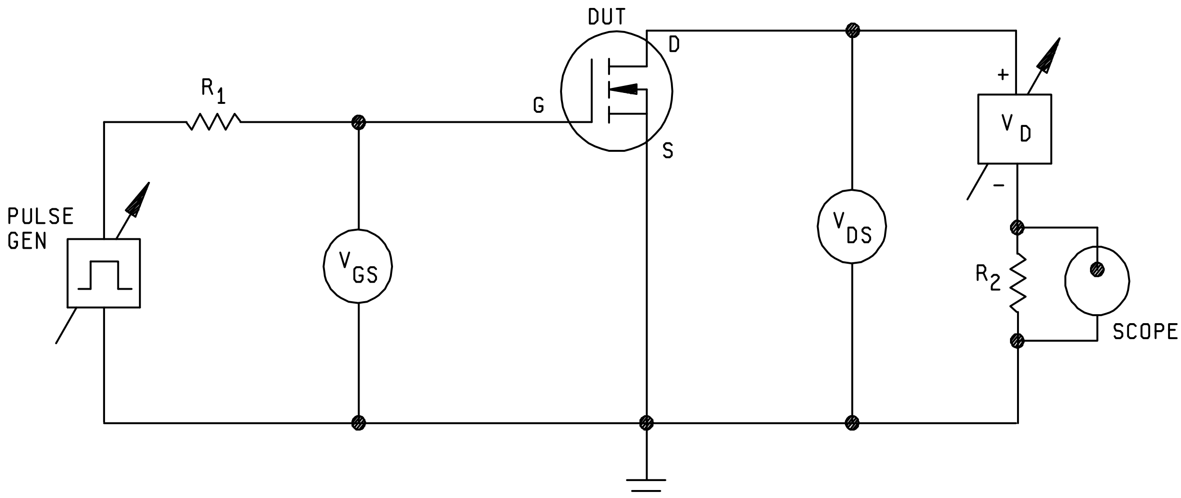
c. V_{DS} = 4 $r_{DS(on)}$ x 0.5 I_D continuous or as necessary to be in the active region.

d. $\Delta V_{GS} \geq$ 0.1 volts.

e. $r_{DS(on)}$ as specified.

f. Pulse width ≤ 300 μs.

g. Unless otherwise specified, (T_C) = (Temperature of case) = +25°C.



NOTES:

1. Pulse the device according to MIL-STD-750. Resistor R_1 shall be used to damp spurious oscillations that can occur (approximately 100 Ω).
2. The device used for circuit illustration is an n-channel, enhancement-mode FET. The methodology described is not limited solely to this type of device. For all other field effect devices where the power ratings are such that the dc method is the preferred method, the parameter symbols need only indicate the appropriate voltage or current polarity.
3. When performing this test on a nonheat-sinked part, the following caution is applicable. The implementation of this test requires the use of repeated incremental steps of gate voltage, while measuring drain current. The number of steps and the duration of each step result is cumulative energy which may thermally overstress the part if it is not heat-sinked. A stepped program to perform this test will result in higher power dissipation during test of a unit requiring a high gate drive voltage than during test of a unit requiring a lesser gate drive voltage.
4. R_2 is a noninductive, current sensing resistor and is normally ≤ 0.1 Ω.

FIGURE 3475-1. Forward transconductance circuit.

METHOD 3476

COMMUTATING DIODE FOR SAFE OPERATING AREA TEST PROCEDURE FOR MEASURING DV/DT DURING REVERSE RECOVERY OF POWER MOSFET TRANSISTORS OR INSULATED GATE BIPOLAR TRANSISTORS

1. Purpose. The purpose of this test method is to define a way for verifying the diode recovery stress capability of power MOSFET transistors. For the IGBT, replace the MOSFET designators for drain and source with the IGBT designators for collector and emitter, D = C and S = E. The focus is on simplicity and practicality.

2. Scope. This method covers all power transistors which have an internal diode capable of commutating current generated during reverse recovery.

3. Definitions.

a. R_G: Gate drive impedance.

b. R_{DUT}: Gate to source circuit resistance at DUT.

c. T_j: Semiconductor junction temperature.

d. V_{GEN}: Gate generator voltage (volts) for drive transistors.

e. V_{DD}: Supply voltage.

f. I_{FM}: Maximum body diode forward current.

g. Driver: A device is used in the lower portion of an "H" bridge (see figure 3476-1) and is an equivalent to the DUT.

h. $L_{(LOAD)}$: Load inductor. Shall be of a large enough value such that the decay of current during the forward conduction of the DUT is less than five percent of I_{FM}.

i. t_{rv}: Drain voltage rise time. Measured between 10 percent of V_{DD} and 90 percent of V_{DD} of the voltage waveform. Limits shall be recorded during the test and a typical value shall be contained in the detail specification.

j. t_{rr}: Reverse recovery time.

k. V_{DS}: Drain-source voltage.

l. $V_{(BR)DSS}$: Breakdown voltage drain-source.

m. I_{GSS}: Reverse gate current, drain shorted to source.

n. I_{DSS}: Zero gate voltage drain current.

o. $R_{DS(ON)}$: Static drain-source on state resistance.

4. Circuit. Basic circuitry for testing this parameter is shown on figure 3476-1. Idealized waveforms are shown on figure 3476-2. Snubbers may not be used. Stray capacitance and inductance, especially in the source of the drive transistor, must be minimized.

The basic principle of the circuit may not be altered, that is, the lower "H" bridge device must be equivalent to the DUT. The circuit may operate continuously, or, single shot, as long as the required test conditions are achieved. Gate drive to the driver may be any Thevenin equivalent of that specified.

To test continuously or single shot, the electrical sequence is almost the same.

a. Drive is turned on until current in $L_{(LOAD)}$ is higher than I_{FM}.

b. Driver is turned off until current in DUT reaches I_{FM}. The minimum time for DUT forward conduction is 5 μs, or, 10 times the rated maximum t_{rr}, whichever is greater.

c. If testing "repetitively" then go back to step 1. Else, driver is turned on for the reverse recovery period of the device plus a minimum additional one microsecond. The DUT shall be monitored for V_{DS} collapse during this additional time period, and gate drive to the driver transistor may be removed at any time a failure is encountered.

If the device operates with a low repetition rate, the device may not be exposed to sufficient energy to cause a catastrophic failure. The circuit must be equipped to either cause catastrophic failure or generate a failure signal in the event of a collapse of V_{DS} during voltage recovery.

5. Specification details. The specification may take the form of a single point tabular specification, a graphical representation, or both. Ideally, a device will have both. This will allow for easy comparison of devices with the tabular specification, but still have the detail of the graph available to the designer.

a. A tabular specification will define a single point of operation. The following must be specified in the detail specification:

1.	R_G Gate drive impedance	_____ Ω
2.	V_{GEN} Gate generated voltage	_____ V
3.	I_{FM} Maximum forward current	_____ A
4.	V_{DD} Supply voltage	_____ V
5.	T_j Junction temperature	_____ °C
6.	dv/dt	_____ V/ns minimum

b. A graphical representation could take several different forms; for example, R_G versus I_{FM}, di/dt versus dv/dt, or I_{FM} versus V_{DS}. An example of R_G versus I_{FM} is shown on figure 3476-3.

6. Acceptance criteria. If a specification requires that this test be performed for verification of a maximum limit, then the device V_{DS} must not collapse during or after reverse recovery and (in addition) must pass any specified parametric limits, as a minimum $V_{(BR)DSS}$, I_{GSS}, I_{DSS}, and $R_{DS(ON)}$.

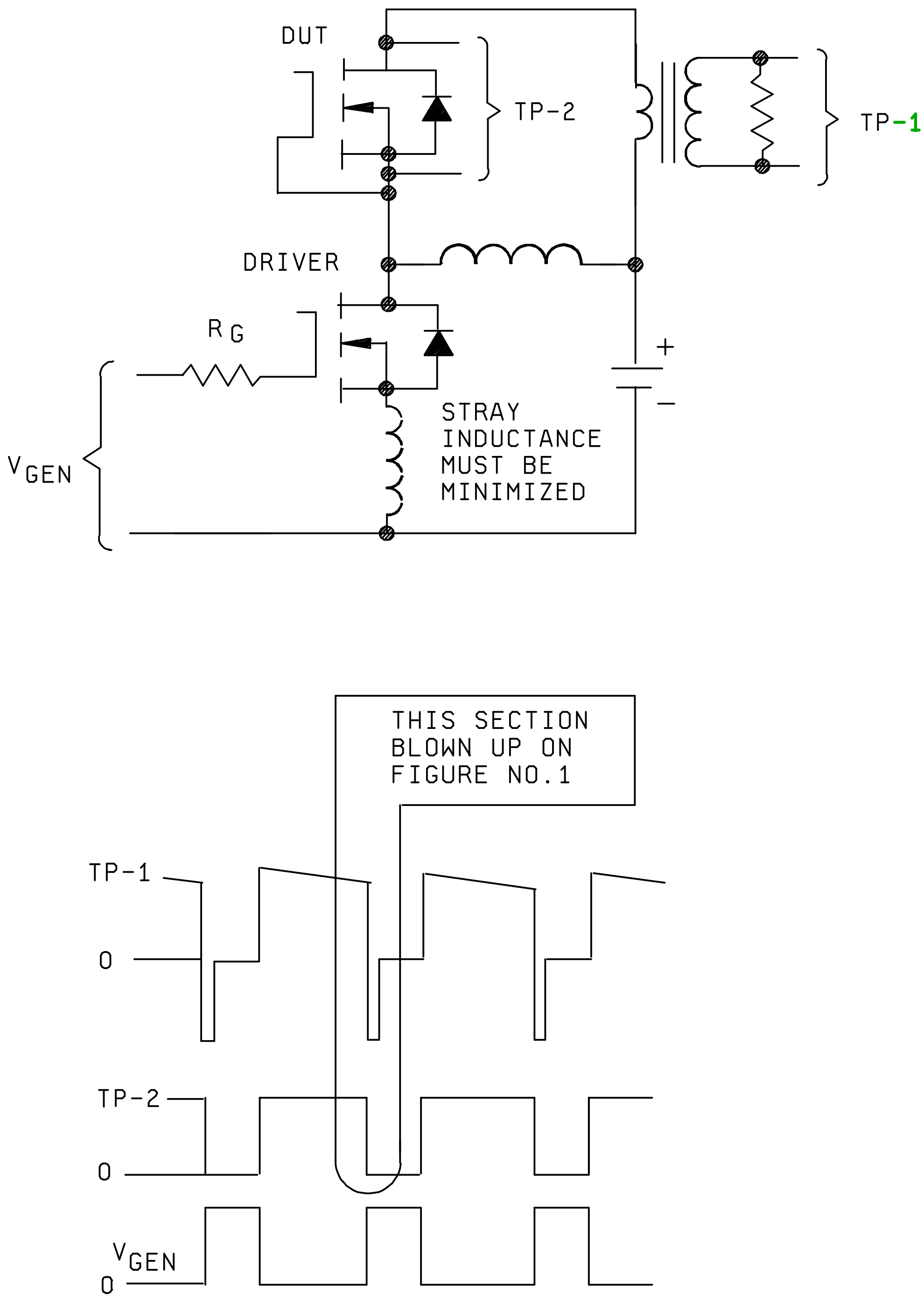


FIGURE 3476-1. Body diode test circuit.

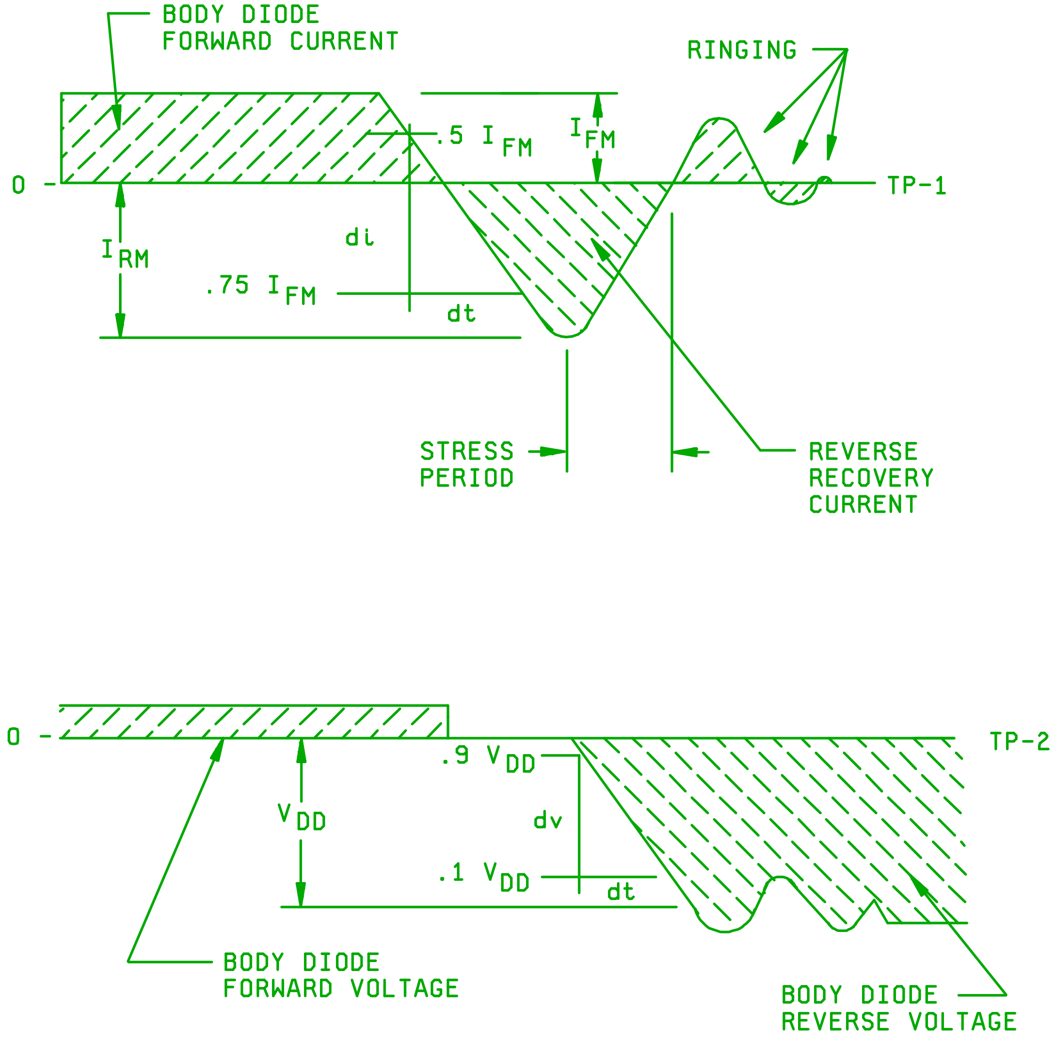


FIGURE 3476-2. Body diode waveforms.

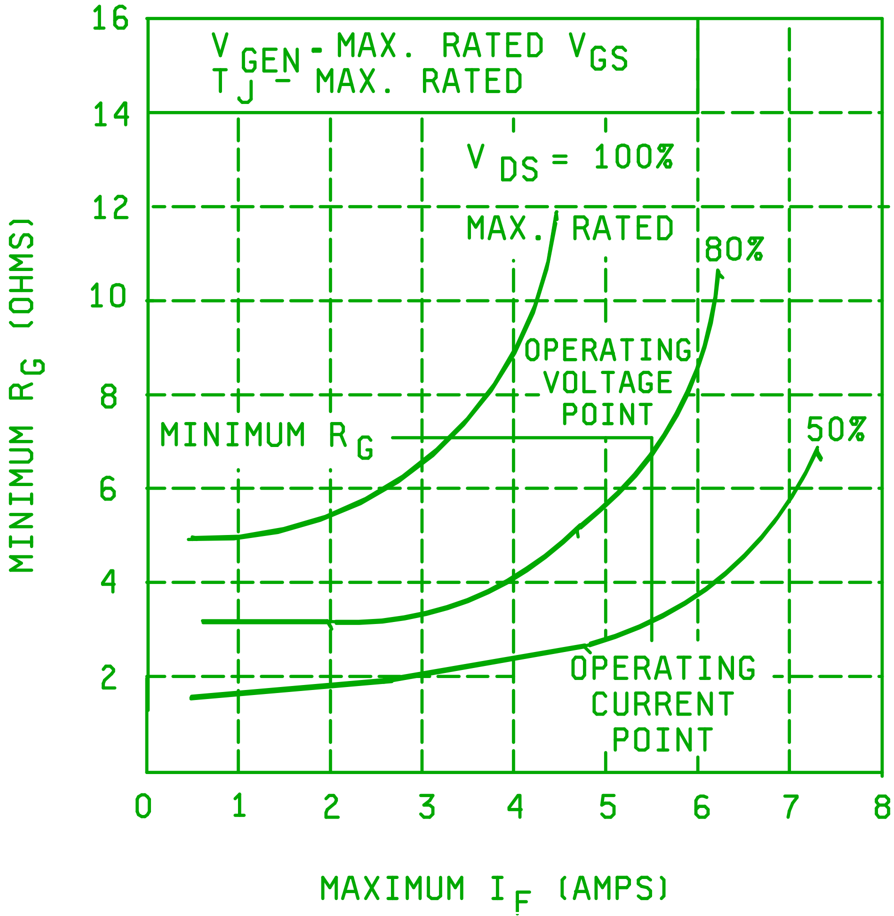


FIGURE 3476-3. Example of graphic representation.

METHOD 3477.1

MEASUREMENT OF INSULATED GATE BIPOLAR TRANSISTOR TOTAL SWITCHING LOSSES AND SWITCHING TIMES

1. Purpose. This method defines the basic test circuitry and waveform definitions by which to measure the total switching losses of an IGBT.

2. Scope. This method applies only to measurements of IGBT devices without an integral diode.

3. Definitions.

a. $V_{(BR)CES}$: Collector/emitter breakdown voltage.

b. I_{CE}: Test current.

c. V_{GE}: Gate to emitter voltage.

d. R_G: Gate drive series resistance.

e. V_{CL}: Clamp voltage (80 percent rated $V_{(BR)CES}$).

f. t0: Time point where V_{CE} is at 10 percent of the specified gate drive.

g. t1: Time point where i_{CE} = 5 percent I_{CE} (maximum).

h. t2: Time point where V_{CE} = 5 percent V_{CL} when V_{CE} is decreasing.

i. t3: Time point where V_{CE} = 5 percent V_{CL} when V_{CE} is increasing.

j. t4: t3 + 5 µs.

k. $t_{d(on)}$: Turn on delay time.

l. t_r: Rise time.

m. $t_{d(off)}$: Turn off delay time.

n. t_f: Fall time.

o. W_{ON}: Turn on switching losses.

p. W_{OFF}: Turn off switching losses.

q. W_{TOT}: Total switching losses.

r. T_j: Semiconductor junction temperature.

s. V_G: Gate drive voltage.

4. Circuitry. Figure 3477-1 shows the basic test circuit. The circuit has to satisfy two fundamental requirements.

a. The circuit reflects the losses that are attributed to the IGBT only and is independent from those due to other circuit components, like the freewheeling diode.

b. The operation of the circuit shown on figure 3477-1 is as follows:

The driver IGBT builds the test current in the inductor. When it is turned off, current flows in the zener. At this point, the switching time and switching energy test begins, by turning on and off the DUT. In its switching, the DUT will see the test current that is flowing into the inductor and the voltage across the zener, without any reverse recovery component from a freewheeling diode. This test can exercise the IGBT to its full voltage and current without any spurious effect due to diode reverse recovery.

Input drive duty cycle should be chosen such that T_j is not affected. Control of T_j is best done using external methods.

5. Method. Figure 3477-2 shows the DUT current and voltage waveforms and test points.

5.1 Energy loss during turn on. During turn on, the energy loss is defined as follows:

(1) $$W_{ON} = \int_{t1}^{t2} i_{CE} \bullet V_{CE} \, dt \text{ joules / pulse}$$

Refer to figure 3477-2 for t1 and t2

5.2 Energy loss during turn off. During turn off, the energy loss is defined as follows:

(2) $$W_{ON} = \int_{t4}^{t3} i_{CE} \bullet V_{CE} \, dt \text{ joules / pulse}$$

Refer to figure 3477-2 for t3 and t4

5.3 Total switching loss. The total switching loss is the sum of equations (1) and (2).

(3) $W_{TOT} = W_{ON} + W_{OFF}$ joules/pulse

5.4 Switching time measurements. Switching time measurements, while not the preferred method of delineating between devices, may be determined using the rules below and as seen on figure 3477-2.

a. $t_{d(on)}$: The interval measured from the 10 percent point of the rising input pulse V_g and the 10 percent rise of the output current I_C.

b. t_r: The interval measured from the 10 percent to the 90 percent point of the rising output current I_C.

c. $t_{d(off)}$: The interval measured from the 90 percent point of the falling input pulse V_g to the 90 percent point of the falling output current I_C.

d. t_f: The interval measured from the 90 percent to the 10 percent point of the falling output current I_C.

6. Equipment. A modern high speed digitizing system is recommended. The measurement of W_{ON} or W_{OFF} is accomplished by accessing the output V(t) and I(t) waveforms, digitizing them, and transmitting the data to a computer where W_{ON} or W_{OFF} is calculated and the results displayed. Two factors of importance must be considered.

a. Sample spacing must be short relative to transition times for accurate and repeatable results.

b. The relative V(t), I(t) channel delay must be known and accounted for in the computer program that does the point by point multiplication and summation that determines either W_{ON} or W_{OFF} (see figure 3477-2).

7. Specifications.

a. V_{CL}: Clamp voltage ____ V

b. I_{CE}: Maximum test current A ____ A

c. V_{GE}: Gate to emitter voltage ____ V

d. R_G: Gate resistance ____ Ω

e. T_j: Junction temperature ____ °C

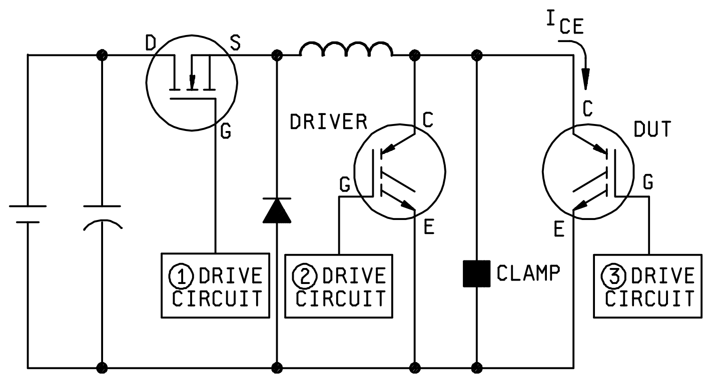


FIGURE 3477-1. Test circuit.

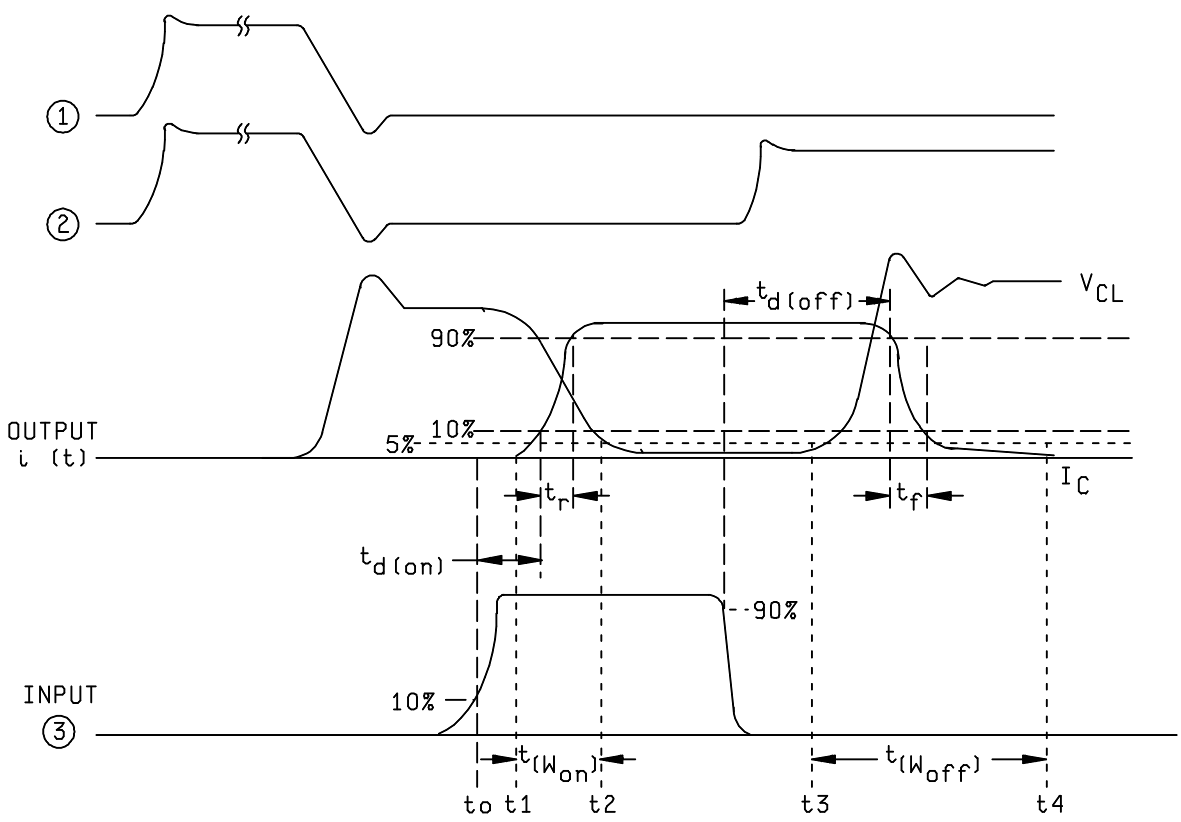


FIGURE 3477-2. Typical clamped inductive waveforms.

METHOD 3478

POWER TRANSISTOR ELECTRICAL DOSE RATE TEST METHOD

1. Purpose. This test method establishes a baseline methodology for characterizing high-voltage transistors to high gamma dose rate radiation and for establishing electrical criteria to evaluate key test fixture parameters. From this data, a valid comparison can then be made between the device's response and its radiation data. Since power transistors are susceptible to radiation-induced burnout/damage, this test method should be considered a destructive test. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Definitions. Definitions, symbols, and terms used in this method are provided below:

a. Power transistor burnout: Burnout is defined as a condition that renders the power transistor nonfunctional, usually a result of current-induced avalanche and second breakdown. Identification is accomplished by observing the drain current during irradiation and by verifying the device's performance after irradiation.

b. Symbols and terms:

di/dt: Change in current with respect to time (amperes per second).

dv/dt: Change in voltage with respect to time (volts per second).

I_{ds}: Measured current flowing into drain (amperes).

L_S: Calculated stray inductance observed by the DUT's response (henrys).

PW: Radiation pulse width defined by the full-width half-max (FWHM) measurement (seconds).

RC: Time constant equal to the resistance times capacitance

R_S: Calculated stray resistance observed by the DUT's response (ohms).

V_{ds}: Applied measured drain-to-source voltage (volts).

V_{gs}: Applied measured gate-to-source voltage (volts).

3. Test plan. A detailed test plan shall be prepared specifying, as a minimum, the following information:

a. Identify device types to be tested.

b. Identify number of samples.

c. Test fixture characteristics of stray R_S and L_S: based upon previous data or calculations (see 5.8).

d. Electrical characterization required in accordance with detailed specifications before and after the radiation event.

e. Electrical parameters to be monitored.

f. Complete description of test system (e.g., schematics, flow charts).

4. Apparatus.

4.1 Instrumentation. Instrumentation required to monitor and test the device to high gamma dose rate radiation will generally consist of the following type of equipment.

a. Curve tracer.

b. Digital or analog voltmeter.

c. DC current probe.

d. Digital or analog current meter.

e. Digitizer or storage scope.

f. High-voltage power supply.

4.2 Holding fixture. The holding fixture may be mandated by the test facility. Coordination between users and facility is an absolute necessity. The fixture shall be capable of interfacing the power and signal lines between the test board and DUT, as well as, collimating the radiation beam to expose only the DUT.

4.3 Test fixture. The test board shall be constructed to meet the following requirements:

a. Construction: Circuit layout and construction are critical. Circuit layout and construction shall be optimized to minimize stray L_S and R_S effects presented to the DUT. Applicable gauge wires, ground planes, and materials shall be used to minimize these effects of stray inductance and resistance. Wire lengths shall be kept to an absolute minimum.

   CAUTION: Wires lengths connecting the DUT in excess of four inches (101.60 mm) should be re-evaluated to determine shortest possible wire length.

b. Components: Circuit components shall be chosen to optimize performance. Capacitors shall have high "Q" ratings reflecting high di/dt. The test circuit shall have multiple capacitors in parallel, minimizing the parasitic resistance presented by each capacitor while obtaining the required dv/dt response. DC current probes shall be passive having minimal "ac" insertion resistance. The current probe shall also be capable of measuring a large current without saturating its magnetic core.

c. DUT package: Circuit and device parameters will dictate the power transistor response to high gamma dose rate radiation. The DUT shall be tested in the same package type that will be used in the system. If a different package type is used, then electrical, mechanical, and thermal properties of that package need to be considered and their effects accounted for in the test results.

d. Test circuit: Schematically, test circuits are shown on figure 3478-1 and representative waveforms are depicted on figure 3478-2. Components and wiring shall not be placed directly in the radiation beam. An isolation resistor shall be placed between the "stiffening" capacitors and high-voltage power supply, minimizing its interaction with the DUT response. The resistor value will depend on the RC time constant required to isolate interaction. Biasing of the gate shall be accomplished using an RC filtering or ballasting resistor network (see figure 3478-1a or 3478-1b), unless it is connected directly to the common source (see figure 3478-1c).

   CAUTION: Peak currents in excess of 1,000 amperes with di/dt in excess of 1,000 amperes per microsecond are possible.

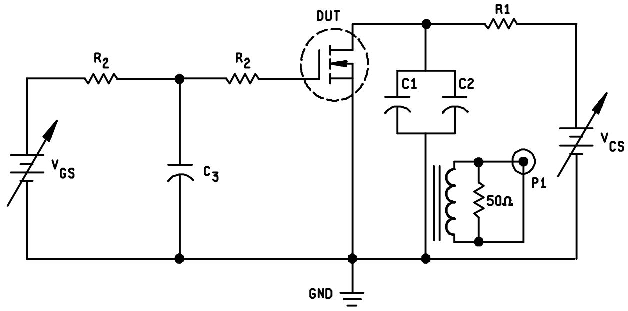


FIGURE 3478-1a. Gate bias configuration 1.

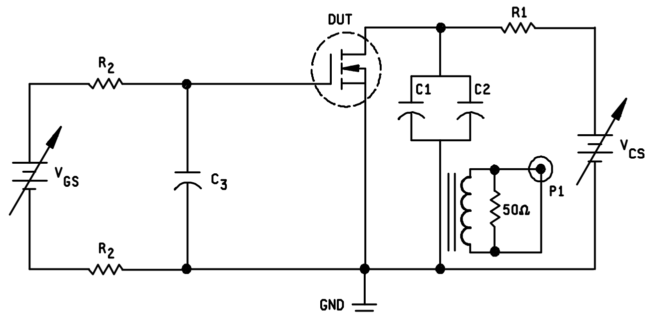


FIGURE 3478-1b. Gate bias configuration 2.

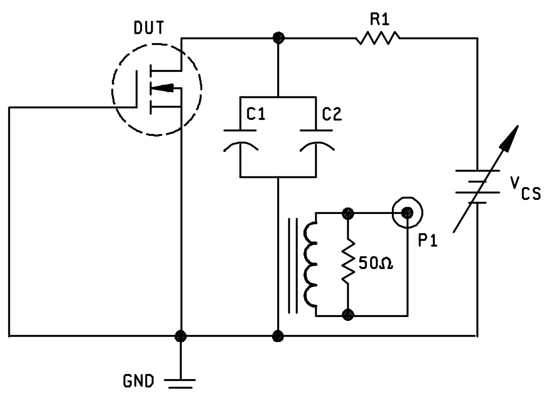


FIGURE 3478-1c. No gate bias configuration 3.

NOTES:
1. C1: Consists of several small capacitors (typically .1 μF).
2. C2: Consists of several large capacitors (typically 200 μF).
3. R1: Drain isolation resistor (typically > 1 kΩ).
4. R2: Gate filter resistor (typically 1 kΩ).
5. C3: Gate filter capacitance (typically 0.1 μF).
6. P1: Current probe (Pearson Model +11 or similar).

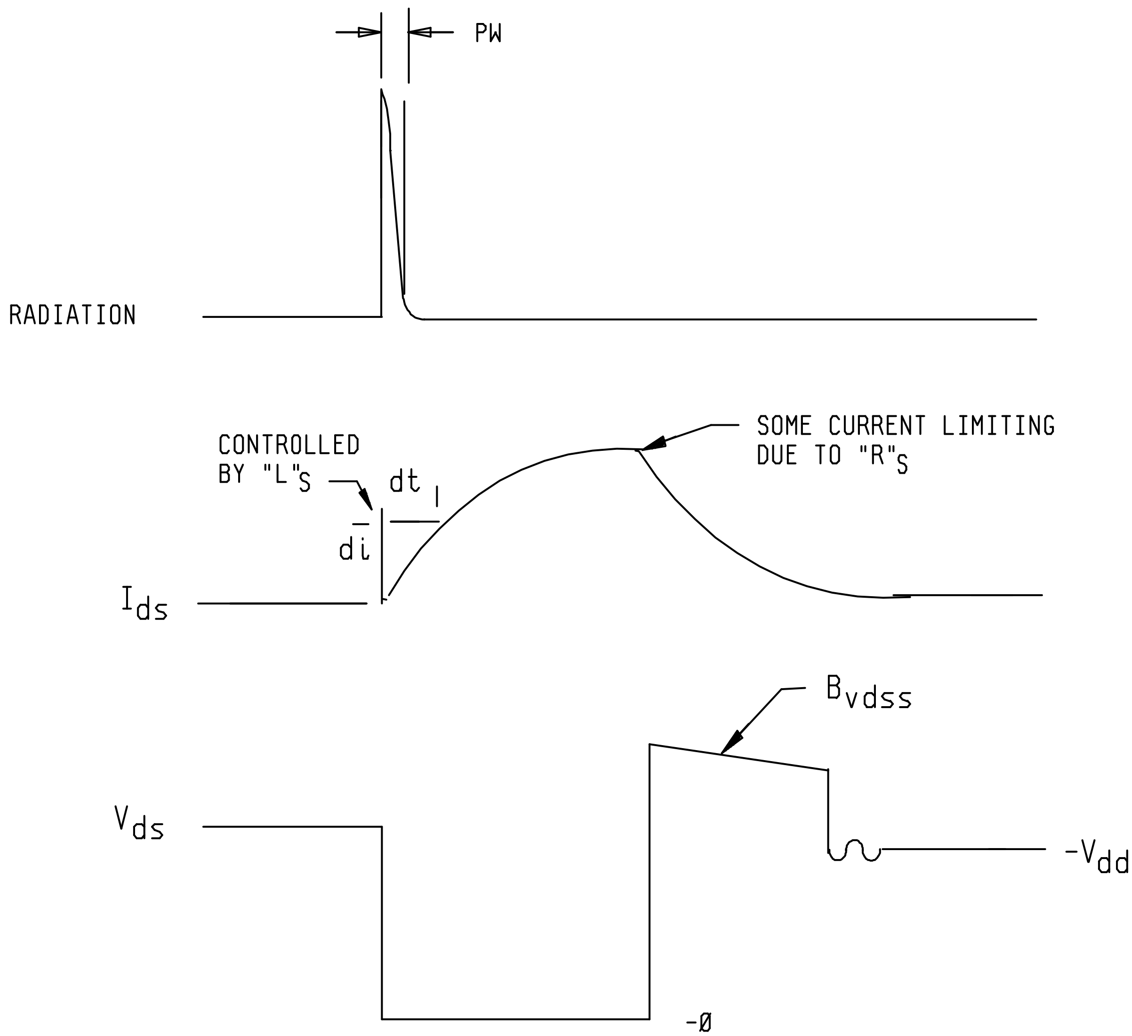


FIGURE 3478-2. Actual test waveforms.

5. Procedure. Two essential requirements are outlined in this procedure that allow a meaningful analysis of a device's radiation response as compared to data obtained on a different test fixture.

a. In 5.1 through 5.7 below, the procedure to characterize power transistor to high gamma dose rate radiation and what data to collect and record are described.

b. In 5.8 below, there is a description for a technique to extract key electrical parameters, L_s and R_s, allowing the test fixture to be characterized using the above radiation data.

5.1 Sample size. A minimum of five samples per device type shall be tested to determine the dose rate response of each power transistor type. All devices shall meet the electrical specifications required for that particular device type before initial exposure.

5.2 Identification. In all cases, each test sample shall be individually marked to ensure that the test data can be traced to its corresponding test sample.

5.3 Radiation source.

a. The radiation source shall be either a flash x-ray or a LINAC.

b. The facility/source shall be capable of varying the dose rate levels to characterize the device's response to various dose rates.

c. The minimum pulse width shall be performed using a 20 to 50 ns pulse width (FWHM).

5.4 Dosimetry. Dosimetry shall be used to measure the actual dose in rad(Si) of the radiation pulse. Any dosimetry technique that meets ASTM standards (ASTM F526-77) may be used.

5.5 Waveform recording. The voltage, V_{ds}, and test current, I_{ds}, shall be monitored before, during, and after each irradiation. Voltage in excess of the maximum input voltage of the recording device shall be attenuated.

5.6 Test conditions. The DUT shall be biased with the specified test conditions and verified for each irradiation. Drain and gate current shall be monitored before, during, and after each exposure. The capacitive load across the drain/source shall maintain the drain bias voltage, V_{ds}, during the exposure within ±10 percent of that specified. The test shall not be repeated until the "stiffening" capacitors have sufficiently recharged. All tests shall be performed at the required ambient temperature.

CAUTION: Some transistors may require a gate bias to turn the DUT "off" after the radiation event.

5.7 Test setup/sequence.

a. Tune LINAC/flash x-ray to desired pulse width and dose rates and perform initial beam dosimetry.

b. Install holding fixture and test system circuitry.

c. Insert DUT (precharacterized in accordance with detailed specification).

d. Apply and verify test voltage to gate (V_{gs}).

e. Apply and verify test voltage to drain (V_{ds}).

f. Connect monitors to appropriate recorders.

g. Expose DUT to desired dose rate.

h. Record photocurrent (I_{ds}) and V_{ds} response.

i. Record test information: Test conditions V_{ds} and V_{gs}; actual dose rate, accumulated total dose, date, and other information pertinent to test.

j. Verify survivability of test device: Check electrical parameters to determine any damage.

k. Repeat with new test conditions: Different V_{ds}, dose rate, or V_{gs}.

5.8 Determination of stray inductance/resistance. Knowing the stray components, L_S and R_S, will provide a technique to compare test data from different test fixtures and packages. L_S and R_S will limit the amount of current flow and the peak current observed by the DUT.

a. Using the recorded photocurrent waveforms, the quantitative values of the stray resistance, R_S, and inductance, L_S, can be extracted for that test fixture and package.

CAUTION. The stray fixture components may change with exposure to radiation, testing, or time.

b. Determine the inductance, L_S, from the relationship:

$$\left(\frac{di}{dt}\right) = \left(\frac{V_{ds}}{L_s}\right)$$

and

$$L_s = \frac{V_{ds}}{\left(\frac{di}{dt}\right)}$$

The calculated inductance will be influenced by the series resistance; and, therefore, the value of the di/dt response shall be based upon the change in primary photocurrent between its 0 percent to 10 percent response. The L_S value shall be determined from this experimental data.

c. Determine the resistance, R_S, from the relationship:

$$I_{ds} = \left(\frac{V_{ds}}{R_s}\right) * \left[1 - \left(\exp - \left((t * \frac{R_s}{L_s}\right)\right)\right]$$

The calculated resistance should be determined from the peak primary photocurrent response and its corresponding time. Using iterative calculations, R_S shall be determined within ±5 percent based upon this experimental data.

6. Documentation. Test records shall be maintained by the experimenter. Test records shall include the following:

a. Part type, item, and lot identification.

b. Date of test and operator's name.

c. Identification of radiation source and pulse width.

d. Description of test system and circuit.

e. Description of dosimetry techniques and circuits.

f. Test bias conditions.

g. Recorded voltage current waveforms.

h. Minimum dose rate V_{ds} to induce burnout.

i. Maximum dose rate V_{ds} not to induce burnout.

j. Device leakage currents before and after irradiation.

k. Recorded waveforms of pulse shape intensity.

l. Accumulated total dose.

m. Ambient test temperature.

n. Calibration records and serial numbers, if required.

o. DC electrical measurements after radiation event.

6.1 Reporting. This documentation shall be used to prepare a summary describing the test system, data, results, and analysis. The summary shall include a description of the device, dc electrical parameters before and after testing, a statistic summary indicating the sample mean and standard deviation of each device type, plots of photocurrent versus dose rate at a specified V_{ds} and V_{gs}, calculations for stray L_s and R_s for the test fixture for each device type or package type, and a general synopsis of the test results.

METHOD 3479

SHORT CIRCUIT WITHSTAND TIME

1. Purpose. In some circuits, such as motor drives, it is necessary for a semiconductor device to withstand a short circuit condition for short periods of time. During such a condition, the current in the device is dependent on the gain of the device and the level of the drive supplied. It is important for the designer to know how long a device can survive a short circuit condition with a given drive level. Fault detect circuits can be designed to react within this time period. In some cases the junction temperature may exceed the maximum rating. If it does, the rating shall be nonrepetitive with a limit on the maximum number of events over the lifetime of the device. Otherwise, it will be a repetitive rating. In the case of a nonrepetitive rating, the manufacturer shall perform adequate reliability testing so as to ensure the validity of this rating. For military specifications, the controlling document shall mandate such tests.

2. Scope. This method covers all power semiconductors or hybrids that can be turned off with a control terminal and which are intended for use as switching devices. Power MOSFET's, IGBT's, and bipolar transistors are examples of these devices.

3. Definitions.

a. T_j: Junction temperature (°C). Its starting value shall be specified, and controlled to five percent at the beginning of the test.

b. t_{SC}: Short circuit withstand time (seconds). Measured between the time the device drive rises above 50 percent of its peak value, and when it falls below 50 percent of its peak value.

c. V_{SC}: Nominal short circuit voltage (volts). Must be maintained between +5 percent and -10 percent of the specified value during the test.

d. L_S: Stray inductance of the output circuit shall be kept as low as is practical, in order to verify this the maximum value of L_S shall be a condition of the test called out on the detailed specification of the device (see figure 3479-2). L_S = V dt/di during the first 10 percent of the output current waveform.

e. Drive: One of the following:

V_{DRIVE} = Nominal drive voltage (volts).

I_{DRIVE} = Nominal drive current (amperes).

This value must be maintained to within ±5 percent of the specified value. In a graphical representation, various levels of "drive" may be specified, as shown on figure 3479-3. The speed of turn-off shall be such that avalanching the DUT is prevented.

f. R_{DRIVE}: The output impedance of the drive circuitry.

4. Circuitry. Electrical test circuitry is as shown on figure 3479-1. Drive circuitry must be appropriate for the device being tested, whether voltage or current driven. Care must be taken to minimize stray inductance in the output circuit in order to avoid limiting the current during the test, or avalanching the device during turn off at the end of the test.

4.1 Procedure for measurement of short circuit withstand time (see figure 3479-2).

a. t0: Apply test voltage.

b. t1: Apply drive signal.

c. t2: Device drive reaches 50 percent of maximum value.

d. t3: Remove drive signal.

e. t4: Device drive falls to 50 percent of maximum value.

f. t5: Remove test voltage.

5. Acceptance criteria. DC electrical test shall be conducted before and after the test. Exactly which parameters are to be measured will be device dependent, and shall be called out on the detail specification.

6. Specification. Tabular specification shall be as follows:

t_{SC} short circuit withstand time		_____ μs at:
1.	V_{SC} short circuit voltage	_____ V
2.	Drive voltage (or current)	_____ V (or A)
3.	T_j junction temperature	_____ °C
4.	R_{DRIVE} output impedance	_____ Ω
5.	L_S stray inductance	_____ nH

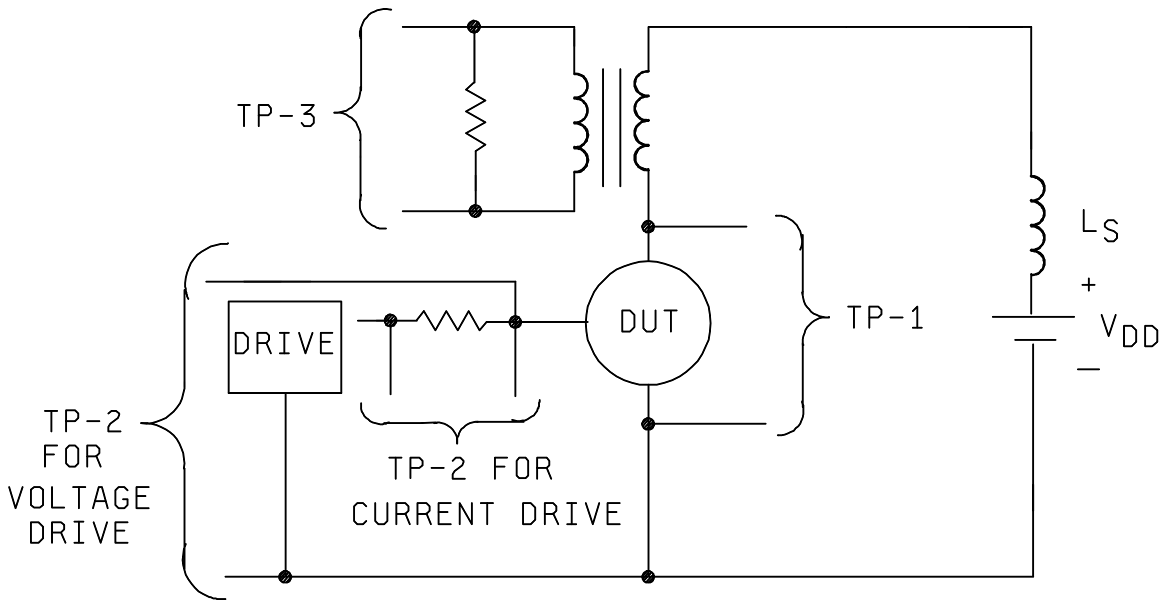


FIGURE 3479-1. Test circuit.

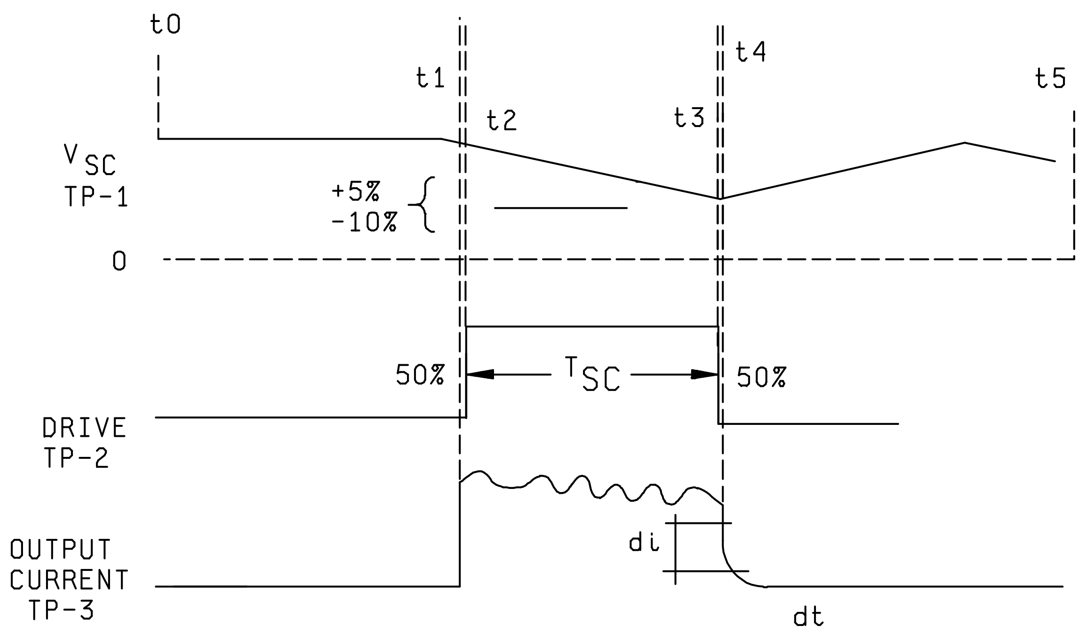


FIGURE 3479-2. Short circuit withstand time waveform.

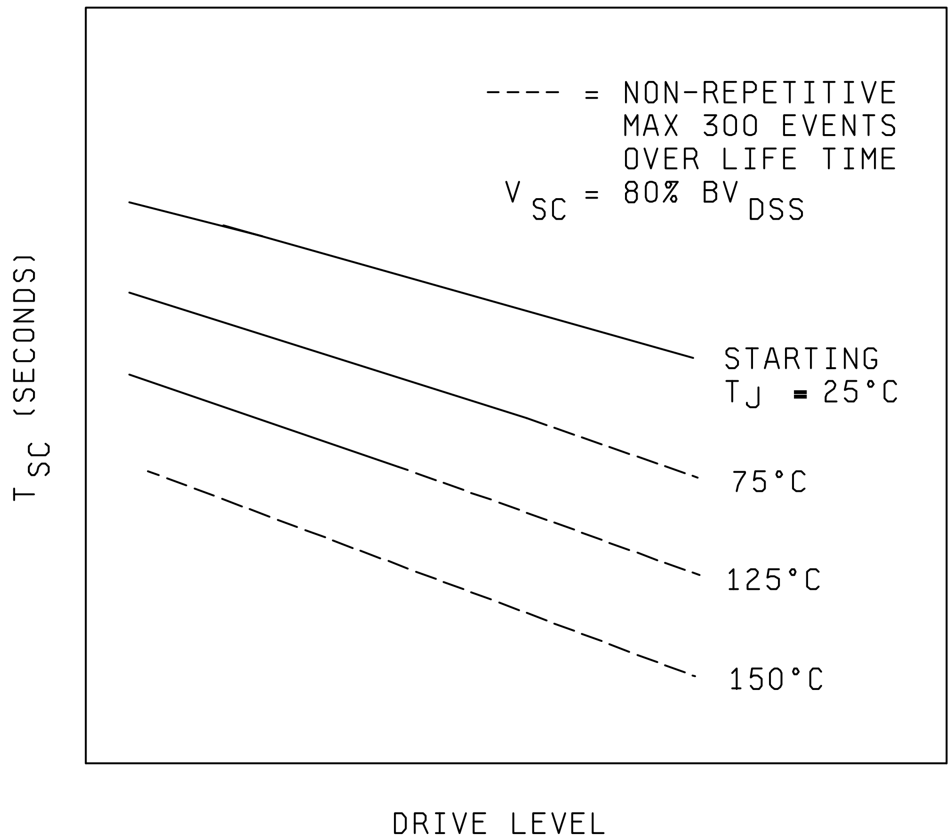


FIGURE 3479-3. Sample graphical specification.

METHOD 3490

CLAMPED INDUCTIVE SWITCHING SAFE OPERATING AREA FOR MOS GATED POWER TRANSISTORS

1. Purpose. To define a method for verifying the inductive switching SOA for MOS gated power transistors, to assure devices are free from latch up.

2. Scope. This method includes all power MOSFETs and IGBTs used in switching applications for power supplies and motor controls.

3. Circuitry. As shown on figure 3490-1, a simple inductive load circuit is employed. Drive circuitry applies a voltage to the DUT to achieve a specified current. The turn-off dv/dt is controlled by a gate resistor. A clamping diode or suppression device is used to limit the maximum voltage which occurs during turn-off. The clamping device must be located as close as possible to the DUT to minimize voltage spikes due to stray inductance L_S.

4. Definitions:

T_J: Junction temperature (°C): Shall not exceed maximum rating of the DUT.

T_A: Ambient temperature (°C): Temperature used to heat the DUT.

T_C: Case temperature (°C): Temperature of the DUT as measured on the exterior of the package as close as possible to the die location.

V_{CC}: Collector supply voltage, dc.

V_{CF}: Clamping voltage.

V_{CES}: Collector to emitter voltage gate shorted to emitter.

V_{DSS}: Source to drain voltage gate shorted to source.

V_{DM}: Maximum off-state voltage measure at the DUT which is caused by stray inductance between the DUT and the voltage suppressor. V_{DM} is due to L di/dt generated during turn-off.

I_L: Load current through inductor and DUT.

V_G: Drive voltage from a voltage source used to turn-on and turn-off the MOS DUT to achieve a specified current.

R_g: Resistor in series with the gate which is used to limit turn-off dv/dt during switching.

dv/dt: Change in voltage during turn-on and turn-off measured between 75 percent and 25 percent of total clamp voltage during turn-off.

t_p: Pulse width between turn-on and turn-off of DUT.

L_S: Stray series inductance due to layout of circuit.

L: Series inductance.

5. Specification conditions. The following conditions shall be specified in the detail specification:

V_{CC}:	V.
V_{CF}:	V.
I_L:	A.
$T_C = T_A$:	°C.
L:	mH.
t_p:	μs.
dv/dt:	V/μs minimum.
N:	Number of pulses.

6. Acceptance criteria.

a. No degradation of blocking voltage at the end of test shall be permitted.

b. Latch-up or reduction of I_L shall not be observed.

c. DUT must meet group A, subgroup 2 limits.

7. Comments and recommendations.

a. Gate resistor or gate drive source must be as close as possible to the DUT to minimize oscillations during turn-off.

b. Gate resistor valve or gate drive is selected to assure minimum peak dv/dt is achieved.

c. V_{CF} clamping device should be as close as possible to the DUT to minimize voltage over shoot. A general guideline is V_{CF} should not exceed 110 percent of V_{DM} and must be less than avalanche breakdown of DUT.

d. L should be selected to assure peak current is reached. The I_C will not be reached if too large of an inductor is used.

e. Safety precautions should be taken when testing high voltage devices and rules and regulations for handling high voltage devices should be followed.

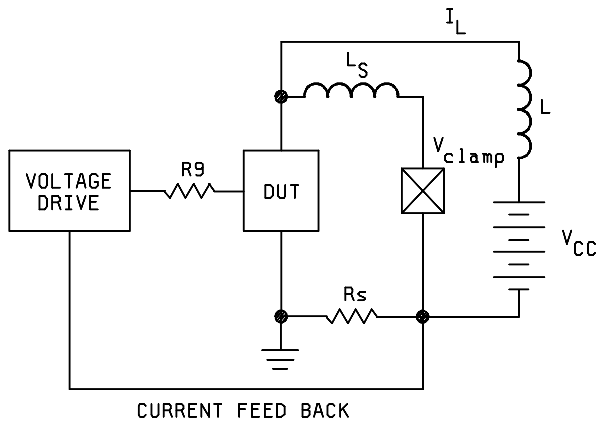
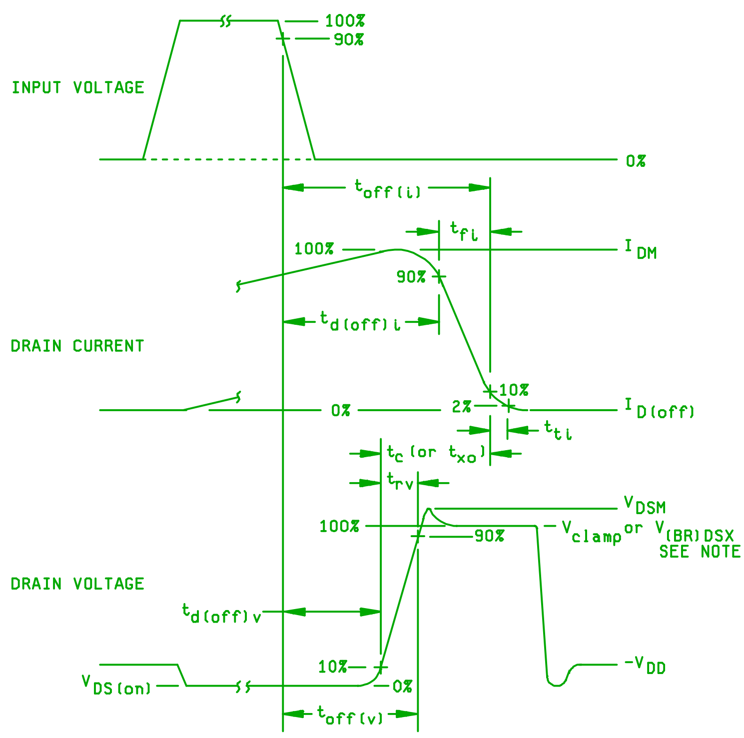


FIGURE 3490-1. Inductive load circuit.



NOTES:

1. V_{clamp} (in a clamped inductive-load switching circuit) or $V_{(BR)DSX}$ (in an unclamped circuit) is the peak off-state.
2. Drain and source references for MOSFETs are equivalent to collector and emitter references for IGBTs.

FIGURE 3490-2. Inductive load waveform.

3500 Series

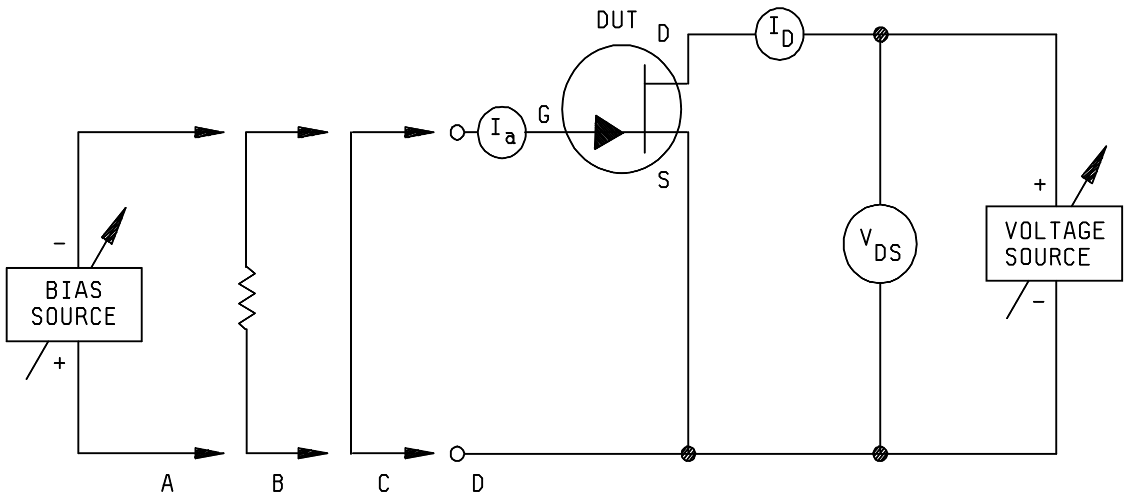
Electrical characteristics tests for Gallium Arsenide transistors

METHOD 3501

BREAKDOWN VOLTAGE, DRAIN TO SOURCE

1. Purpose. The purpose of this test is to determine if the breakdown voltage of the gallium arsenide field-effect transistor under the specified conditions is greater than the specified minimum limit.

2. Test circuit. See figure 3501-1.



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 3501-1. Test circuit.

3. Procedure. A negative (reverse) voltage shall be applied to the gate, with the specified bias condition (condition A) applied, then a positive voltage applied to the drain. The device is acceptable if the gate current 1/ is less than the maximum specified with the voltage bias conditions on the gate and drain as specified in the detail specification. With the specified gate and drain voltages, if the specified maximum gate current is exceeded, the device shall be considered a failure.

4. Summary. The following conditions shall be specified in the detail specification:

a. Test current (see 3).

b. The bias condition is gate to source and drain to source - reverse bias (specify bias voltages).

1/ I_q - - - - - Breakdown voltage as determined by maximum. Allowed gate current, with the specified bias condition applied from gate to source and drain to source.

METHOD 3505

MAXIMUM AVAILABLE GAIN OF A GaAs FET

1. Purpose. This method establishes a basic test circuit for the purpose of determining the associated gain of a gallium arsenide field-effect transistor (FET).

2. Procedure. Configure the test setup as shown on figure 3505-1. First apply the gate voltage (V_{GS}) then apply the drain voltage (V_{DS}). Adjust the gate voltage so that the FET is biased at the specified operating point as noted in the detail specification, such as I_{DS} = 50 percent of I_{DSS}. Adjust the input and output tuners so that the transistor exhibits maximum output power and near maximum gain, that is, the transistor's gain must not be compressed more than 2 dB. The input power level is then reduced by at least 10 dB. At this reduced input signal level, the small signal gain is defined as G0.

Calculation:

G_{1dB} = G0 - 1.0 dB (Associated gain at the 1 dB compression point).

The gain of the FET (output power/input power in dB) is recorded as the input power is increased in 1 dB increments. When the measured gain of the FET is less than or equal to G_{1dB}, as calculated above, the output power is recorded and this value represents the 1 dB compression point (P_{1dB}) power level and is used in determining the pass/fail status of the DUT in accordance with the value specified in the detail specification.

3. Test circuit. See figure 3505-1.

4. Summary. Unless otherwise specified in the detail specification, the following condition shall apply: T_C = (Temperature of case) = +25°C.

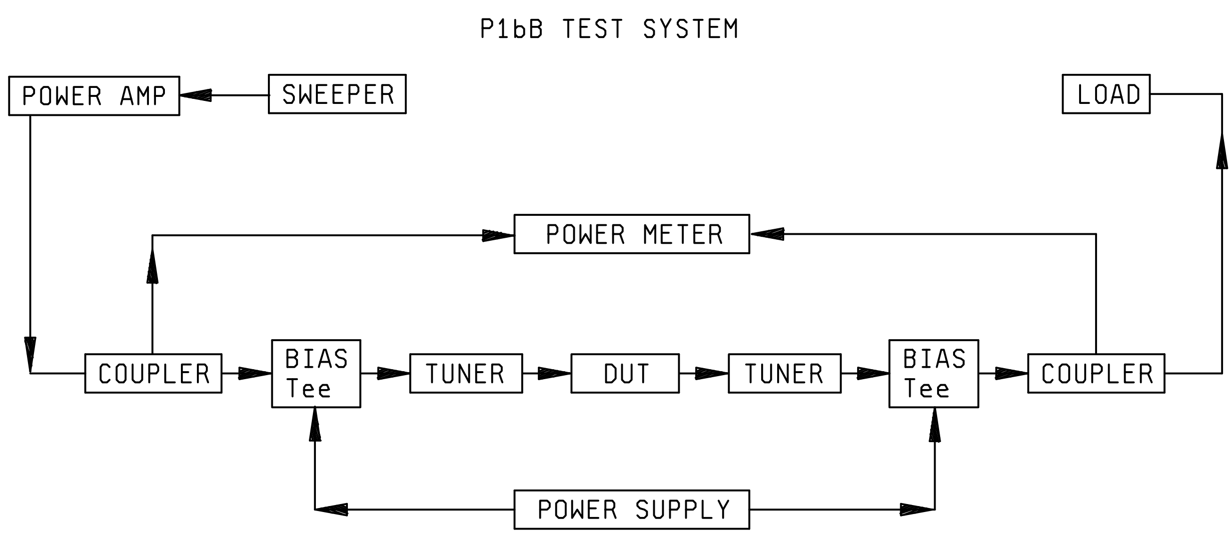


FIGURE 3505-1. Test circuit.

METHOD 3510

1 dB COMPRESSION POINT OF A GaAs FET

1. Purpose. This method establishes a basic test circuit for the purpose of determining the 1 dB compression point of a gallium arsenide FET.

2. Procedure. Configure the test setup as shown on figure 3510-1. To prevent damage to the DUT, first apply the gate voltage (V_{GS}) then apply the drain voltage (V_{DS}). Adjust the gate voltage so the FET is biased at the specified operating point as noted in the detail specification, such as I_{DS} = 50 percent of I_{DSS}. Adjust the input power to the level and frequency given in the detail specification; adjust the input and output tuners so the transistor exhibits maximum output power while its gain remains within 2 dB of the manufacturer's specified minimum gain for the part and while the gate current remains within the range specified in the detail specification. The gate current must also remain within the range specified in the detail specification. The input power level is then reduced by 10 dB or some greater amount specified in the detail specification. At this reduced input signal level the small signal gain is defined as G0.

Calculation: G_{1dB} = G0 = 1.0 dB.

The gain of the FET (output power/input power in dB) is recorded as the input power is increased in increments of 1 dB decreasing to 0.25 dB, or smaller, as G_{1dB} is approached. When the gain of the FET is less than or equal to G_{1dB}, as calculated above, the output is recorded and this value represents the 1 dB compression point (P_{1dB}) and is used in determining the pass/fail status of the DUT in accordance with the value specified in the detail specification.

3. Test circuit. See figure 3510-1.

4. Summary. Unless otherwise specified in the detail specification, the following condition shall apply: (T_C) = (Temperature of case) = +25°C.

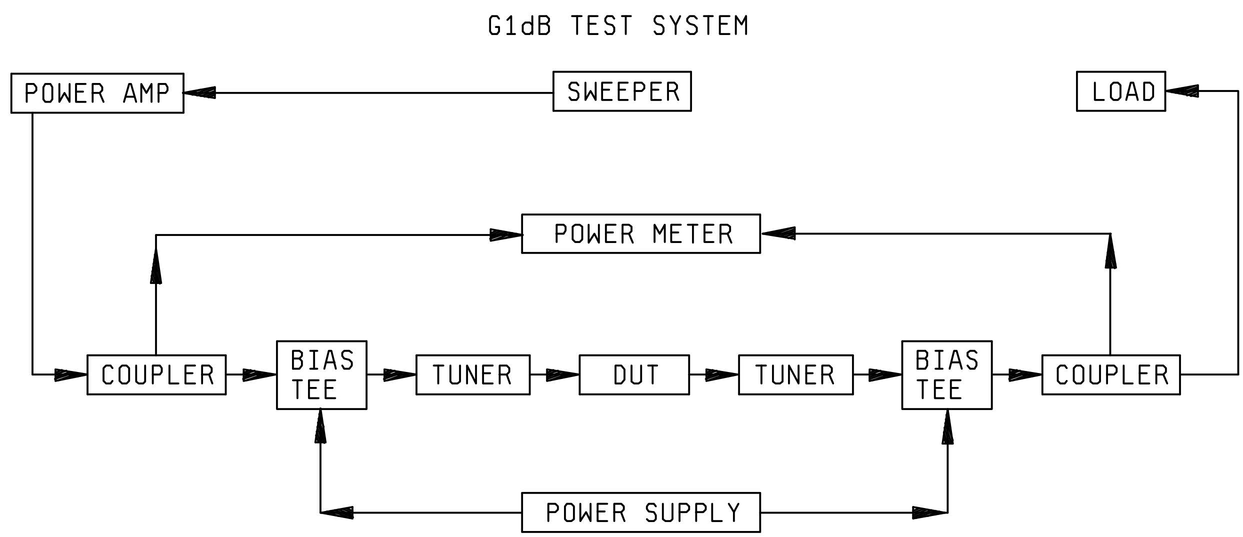


FIGURE 3510-1. Test system.

METHOD 3570

GaAs FET FORWARD GAIN (Mag S21)

1. Purpose. This method establishes a basic test method, test setup, and procedure for measuring the forward gain (Magnitude of S21) of GaAs FETs.

2. Procedure. Configure and calibrate the test setup as shown on figure 3570-1. To prevent damage to the DUT, first apply the gate voltage (V_{GS}) and then apply the drain voltage (V_{DS}) to the bias levels specified in the detail specification. Adjust the gate voltage so that the DUT is biased at the specified operating point, such as I_{DS} = 50 percent of I_{DSS}. Record the DUT's magnitude of S21 (in dB) using the network analyzer as shown on figure 3570-1.

3. Test circuit. See figure 3570-1.

4. Summary. Unless otherwise specified in the detail specification, the following condition shall apply: (T_C) = (Temperature of case) = +25°C.

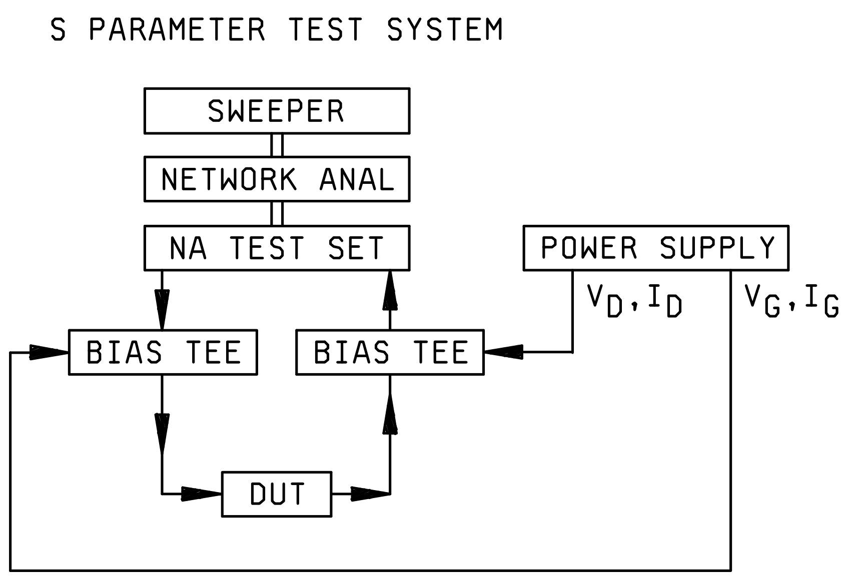


FIGURE 3570-1. Parameter test system.

METHOD 3575

FORWARD TRANSCONDUCTANCE

1. Purpose. This method establishes a basic test circuit for the purpose of establishing forward transconductance gm for gallium arsenide field-effect transistors.

2. Procedure. The gate to source voltage (V_{g1}) is applied as necessary to achieve the specified drain to source current (I_{DS1}). The gate to source voltage is reduced gradually or increased gradually by 0.050 volts (V_{g2}) and the drain to source current is measured (I_{DS2}). The transconductance (gm) is calculated using the following formula:

Calculation:

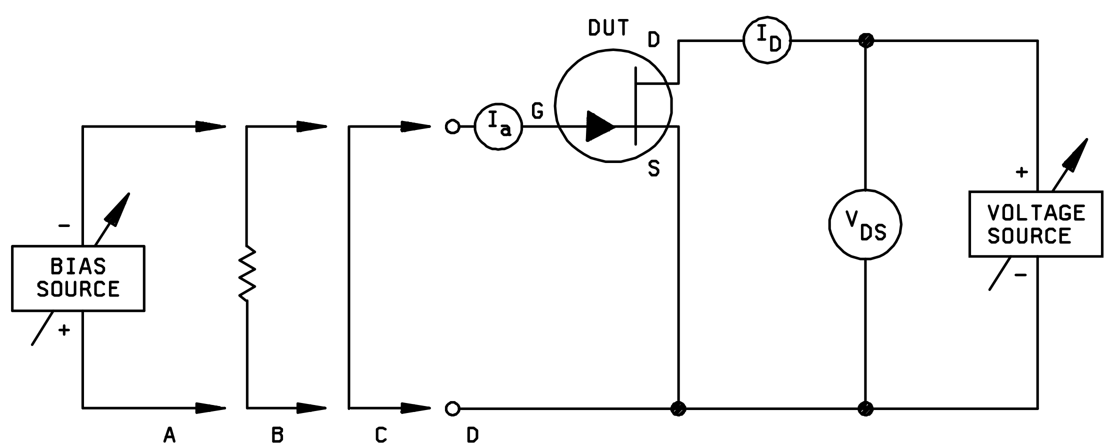
$$gm = \left| \frac{I_{d1} - I_{d2}}{0.050} \right|$$

3. Test circuit. See figure 3575-1.

4. Summary. Unless otherwise specified in the detail specification, the following conditions shall apply:

a. I_{D1} = 0.5 I_{DSS} ±10 percent I_{DSS}.

b. Unless otherwise specified, T_C = (Temperature of case) = +25°C.



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 3575-1. Forward transconductance circuit.