The documentation and process conversion measures necessary to comply with this Notice shall be completed by

INCH-POUND

MIL-STD-750D
NOTICE 2
23 February 1996

NOTICE OF CHANGE

MILITARY STANDARD

TEST METHODS FOR SEMICONDUCTOR DEVICES

TO ALL HOLDERS OF MIL-STD-750D:

1. THE FOLLOWING PAGES OF MIL-STD-750D HAVE BEEN REVISED AND SUPERSEDE THE PAGES LISTED:

METHOD	NEW PAGE	DATE	SUPERSEDED PAGE	DATE
---	9	23 February 1996	9	28 February 1995
---	10	23 February 1996	10	28 February 1995
---	11	23 February 1996	11	28 February 1995
---	12	23 February 1996	12	28 February 1995
---	15	23 February 1996	15	18 May 1995
---	16	23 February 1996	16	18 May 1995
---	17	23 February 1996	17	REPRINTED WITHOUT CHANGE
---	18	23 February 1996	18	28 February 1995
1020.2	3	23 February 1996	3	28 February 1995
1020.2	4	23 February 1996	4	REPRINTED WITHOUT CHANGE
2037	1	23 February 1996	1	REPRINTED WITHOUT CHANGE
2037	2	23 February 1996	2	28 February 1995

2. THE FOLLOWING TEST METHODS OF MIL-STD-750D HAVE BEEN REVISED AND SUPERSEDE THE TEST METHOD LISTED:

METHOD	DATE	SUPERSEDED METHOD	DATE
1001.2	23 February 1996	1001.1	28 February 1995
1011.1	23 February 1996	1011	28 February 1995
1015.1	23 February 1996	1015	28 February 1995
1021.3	23 February 1996	1021.2	28 February 1995
1038.4	23 February 1996	1038.3	28 February 1995
1046.3	23 February 1996	1046.2	28 February 1995
2069.1	23 February 1996	2069	28 February 1995
2072.6	23 February 1996	2072.5	28 February 1995
2074.3	23 February 1996	2074.2	28 February 1995
2076.3	23 February 1996	2076.2	28 February 1995
3105.1	23 February 1996	3105	28 February 1995
4026.3	23 February 1996	4026.2	28 February 1995
4031.4	23 February 1996	4031.3	28 February 1995

3. RETAIN THIS NOTICE AND INSERT BEFORE TABLE OF CONTENTS.

4. Holders of MIL-STD-750D will verify that page changes and additions indicated above have been entered. This notice page will be retained as a check sheet. This issuance, together with appended pages, is a separate publication. Each notice is to be retained by stocking points until the military standard is completely revised or canceled.

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Navy - EC
Air Force - 17
NASA - NA

Review activities:
Army - AR, ER, MI
Navy - AS, CG, MC, SH
Air Force - 19, 85, 99

Preparing activity:
DLA - ES

(Project 5961-1792)

b. Connectors to test boards or trays. After the test boards are loaded with devices, inserted into the system, and brought up to the specified operating conditions, each required test voltage and signal condition shall be verified in at least one location on each test board or tray so as to assure electrical continuity and the correct application of specified electrical stresses for each connection or contact pair used in the applicable test configuration. The system may be opened for a maximum of 10 minutes.

c. At the conclusion of the test period, prior to removal of devices from temperature and bias conditions, the voltage and signal condition verification of 4.4b shall be repeated.

d. For class S devices, each test board or tray and each test socket shall be verified prior to test to assure that the specified bias conditions are applied to each device. This may be accomplished by verifying the device functional response at each device output(s) or by performing a socket verification on each socket prior to loading. An approved alternate procedure may be used.

4.4.1 Bias interruption. Where failures or open contacts occur which result in removal of the required bias stresses for any period of the required bias duration, the bias time shall be extended to assure actual exposure for the total minimum specified test duration. Any loss(es) or interruption(s) of bias in excess of 10 minutes total duration while the chamber is at temperature during the final 8 hours of burn-in shall require extension of the bias duration for an uninterrupted 8 hours minimum, after the last bias interruption.

4.5 Requirements for HTRB and burn-in.

a. The temperature of +20°C minimum is the ambient air temperature to which all devices should be exposed during power screening where room ambient is specified.

b. An increase in effective ambient temperature from cumulative induced power to DUTs shall not result in device junction temperature exceeding maximum ratings.

c. Ambient temperature shall not be measured in the convection current (above) or downstream (Fan Air) of DUTs.

d. Moving air greater than 30 CFM (natural convection) may be allowed for the purpose of temperature equalization within high device density burn-in racks.

e. High velocity or cooled air shall not be used for the purpose of increasing device ratings.

f. Power up of burn-in racks may occur when ambient is less than specified. When thermal equilibrium has been reached, or five hours maximum has occurred, the ambient shall be at the specified value. Time accrued prior to reaching specified ambient shall not be chargeable, to the life test duration.

g. If the ambient at or beyond the five hour point is not the specified value, a nonconformance shall exist requiring corrective action.

h. Time is not chargeable during the period when specified conditions are not maintained. If device maximum ratings(if life test, finish the test and use for credit; if shippable, use this criteria)are exceeded and the manufacturer intends to submit the lot affected, the product on test must be evaluated by re-starting the burn-in or HTRB from zero hours at the specified temperature and verifying that the end-point failure rate is typical for this product type from a review of established records.

i. Chamber temperature for HTRB and burn-in shall be controlled to ±3 percent of the specified value. (Unless otherwise specified in 4.1.1.) This temperature shall be maintained within the chamber. Forced air may be used to equalize temperature within the chamber but shall not be used as a coolant to increase device power capability.

4.6 Bias requirements.

a. Bias errors at the power supply source caused by changing power supply loads during temperature transitions shall not exceed ±5 percent of that specified value.

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b. Bias values at the source, during stabilized conditions, shall not exceed ±3 percent of the specified value.

c. Burn-in apparatus shall be arranged so as to result in the approximate average power dissipation for each device whether devices are tested individually or in a group. Bias and burn-in circuitry tolerances should not vary test conditions to individual devices by more than ±5 percent of specified conditions.

d. Normal variation in individual device characteristics need not be compensated for by burn-in circuitry.

e. Burn-in equipment shall be arranged so that the existence of failed or abnormal devices in a group does not negate the effect of the test for other devices in the group. Periodic verification will assure that specified conditions are being maintained. Verification shall be performed, as a minimum, at the starting and end of screening.

f. Lead, stud, or case mounted devices shall be mounted in their normal mounting configuration and the point of mechanical connection shall be maintained at no less than the specified ambient.

4.7 Destructive tests. Unless otherwise demonstrated, the following MIL-STD-750 tests are classified as destructive:

METHOD NUMBER	TEST
1017	Neutron irradiation
1019	Steady state total dose irradiation
1020	ESDS classification
1021	Moisture resistance
1036,1037	Intermittent operation life
1041	Salt atmosphere
1042 (Condition D)	Burn-in/life test for power MOSFETs
1046	Salt spray
1056	Thermal shock (glass strain)
2017	Die shear test
2031	Soldering heat
2036	Terminal strength
2037	Post seal bond strength
2075	Decap internal visual design verification
2077	SEM

All other mechanical or environmental tests (other than those listed in 4.8) shall be considered destructive initially, but may subsequently be considered nondestructive upon accumulation of sufficient data to indicate that the test is nondestructive. The accumulation of data from five repetitions of the specified test on the same sample of product, without significant evidence of cumulative degradation in any device in the sample, is considered sufficient evidence that the test is nondestructive for the device of that manufacturer. Any test specified as a 100 percent screen shall be considered nondestructive for the stress level and duration or number of cycles applied as a screen.

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4.8 Nondestructive tests. Unless otherwise demonstrated, the following MIL-STD-750 tests are classified as nondestructive:

METHOD NUMBER	TEST
1001	Barometric pressure
1022	Resistance to solvents
1026,1027	Steady-state life
1031,1032	High temperature life (nonoperating)
1038,1039,1040	Burn-in screen
1042 (Condition A,B, and C)	Burn-n/life test for power MOSFETs
1051 (100 cycles or less)	Thermal shock (temperature cycling
1071	Hermetic seal tests
2006	Constant acceleration
2016	Shock
2026	Solerability (if the original lead finish is unchanged and if the maximum allowable number of reworks is not exceeded.)
2052	PIND test
2056	Vibration, variable frequency
2066	Physical dimensions
2069,2070,2072,2073,2074	Internal visual (pre-cap)
2071	External visual
2076	Radiographic inspection
2081	Forward instability shock test (FIST)
2082	Backward instability shock test (BIST)
3101	Thermal impedance testing of diodes
3103	Thermal impedance measurements for IGBTs
3104	Thermal impedance measurements for GaAs
3051,3052,3053 (with limited supply voltage)	Safe operating area (SOA) (condition A for method 3053)
3131	Thermal resistance (emitter to base forward voltage, emitter-only switching method)
4066	Surge current
4081	Thermal resistance of lead mounted diode (forward voltage, switching method)

When the junction temperature exceeds the device maximum rated junction temperature for any operation or test (including electrical stress test), these tests shall be considered destructive except under transient surge or nonrepetitive fault conditions or approved accelerated screening when, it may be desirable to allow the junction temperature to exceed the rated junction temperature. The feasibility shall be determined on a part by part basis and in the case where it is allowed adequate sample testing shall be performed to provide the proper reliability safeguards.

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4.9 Laboratory suitability. Prior to processing any semiconductor devices intended for use in any military system or sub-system, the facility performing the test(s) must be audited by the Defense Electronics Supply Center, Sourcing and Qualification Division (DESC-ELST) and be granted written Laboratory Suitability status for each test method to be employed. Processing of any devices by any facility without Laboratory Suitability status for the test methods used shall render the processed devices nonconforming.

5. DETAILED REQUIREMENTS (NOT APPLICABLE)

6. NOTES

6.1 International standardization agreement. Certain provisions of this standard are the subject of international standardization agreement. When amendment, revision, or cancellation of this standard is proposed which will affect or violate the international agreement concerned, the preparing activity will take appropriate reconciliation action through international standardization channels, including departmental standardization offices, if required.

Custodians:
Navy - EC
Army - ER
Air Force - 17
NASA - NA

Review activities:
Army - AR, ER, MI
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Preparing activity:
DLA - EC

(Project 5961-1451)

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Numerical index of test methods

Method no.	Title
	Environmental tests (1000 series).
*1001.2	Barometric pressure (reduced).
*1011.1	Immersion.
*1015.1	Steady-state primary photocurrent irradiation procedure (electron beam).
1016.1	Insulation resistance.
1017.1	Neutron irradiation.
1018	Internal water-vapor content.
1019.4	Steady-state total dose irradiation procedure.
*1020.2	Electrostatic discharge sensitivity (ESDS) classification.
*1021.3	Moisture resistance.
1022.5	Resistance to solvents.
1026.5	Steady-state operation life.
1027.3	Steady-state operation life (sample plan).
1031.5	High-temperature life (nonoperating).
1032.2	High-temperature (nonoperating) life (sample plan).
1036.3	Intermittent operation life.
1037.2	Intermittent operation life (sample plan).
*1038.4	Burn-in (for diodes, rectifiers, and zeners).
1039.4	Burn-in (for transistors).
1040	Burn-in (for thyristors (controlled rectifiers)).
1041.3	Salt atmosphere (corrosion).
1042.3	Burn-in and life test for power MOSFET's or insulated gate bipolar transistors (IGBT).
*1046.3	Salt spray (corrosion).
1048	Blocking life.
1049	Blocking life (sample plan).
1051.5	Temperature cycling (air to air).
1054.1	Potted environment stress test.
1055.1	Monitored mission temperature cycle.
1056.7	Thermal shock (liquid to liquid).
1061.1	Temperature measurement, case and stud.
1066.1	Dew point.
*1071.6	Hermetic seal.
	Mechanical characteristics tests (2000 series).
2005.2	Axial lead tensile test.
2006	Constant acceleration.
2016.2	Shock.
2017.2	Die attach integrity.
2026.10	Solderability.
2031.2	Soldering heat.
2036.4	Terminal strength.
*2037	Bond strength.
2046.1	Vibration fatigue.
2051.1	Vibration noise.
2052.2	Particle impact noise detection (PIND) test.
2056	Vibration, variable frequency.
2057.1	Vibration, variable frequency (monitored).
2066	Physical dimensions.
2068	External visual for nontransparent, glass-encased, double plug, noncavity, axial leaded diodes.
*2069.1	Pre-cap visual, power MOSFET's.
2070.1	Pre-cap visual microwave discrete and multichip transistors.
2071.3	Visual and mechanical examination.
*2072.6	Internal visual transistor (pre-cap) inspection.
2073	Visual inspection for die (semiconductor diode).
*2074.4	Internal visual inspection (discrete semiconductor diodes).
2075	Decap internal visual design verification.

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Numerical index of test methods - Continued.

Method no.	Title
	Mechanical characteristics tests (2000 series) - Continued.
*2076.3	Radiography.
2077.3	Scanning electron microscope (SEM) inspection of metallization.
2081	Forward instability, shock (FIST).
2082	Backward instability, vibration (BIST).
2101	DPA procedures for diodes.
2102	DPA procedures for wire bonded devices.
	Electrical characteristics tests for bipolar transistors (3000 series).
3001.1	Breakdown voltage, collector to base.
3005.1	Burnout by pulsing.
3011.2	Breakdown voltage, collector to emitter.
3015	Drift.
3020	Floating potential.
3026.1	Breakdown voltage, emitter to base.
3030	Collector to emitter voltage.
3036.1	Collector to base cutoff current.
3041.1	Collector to emitter cutoff current.
3051	Safe operating area (continuous dc).
3052	Safe operating area (pulsed).
3053	Safe operating area (switching).
3061.1	Emitter to base cutoff current.
3066.1	Base emitter voltage (saturated or nonsaturated).
3071	Saturation voltage and resistance.
3076.1	Forward-current transfer ratio.
3086.1	Static input resistance.
3092.1	Static transconductance.
	Circuit-performance and thermal resistance measurements (3100 series).
3101.3	Thermal impedance testing of diodes.
3103	Thermal impedance measurements for insulated gate bipolar transistor (delta gate-emitter on voltage method).
3104	Thermal impedance measurements of GaAs MOSFET's (constant current forward-biased gate voltage method).
*3105.1	Measurement method for thermal resistance of a bridge rectifier assembly.
3126	Thermal resistance (collector-cutoff-current method).
3131.2	Thermal impedance measurements for bipolar transistors (delta base-emitter voltage method).
3132	Thermal resistance (dc forward voltage drop, emitter base, continuous method).
3136	Thermal resistance (forward voltage drop, collector to base, diode method).
3141	Thermal response time.
3146.1	Thermal time constant.
3151	Thermal resistance, general.
3161	Thermal impedance measurements for vertical power MOSFET's (delta source-drain voltage method).
3181	Thermal resistance for thyristors.
	Low frequency tests (3200 series).
3201.1	Small-signal short-circuit input impedance.
3206.1	Small-signal short-circuit forward-current transfer ratio.
3211	Small-signal open-circuit reverse-voltage transfer ratio.
3216	Small-signal open-circuit output admittance.
3221	Small-signal short-circuit input admittance.
3231	Small-signal short-circuit output admittance.
3236	Open circuit output capacitance.
3240.1	Input capacitance (output open-circuited or short-circuited).
3241	Direct interterminal capacitance.

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Method no.	Title
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3246.1	Noise figure.
3251.1	Pulse response.
3255	Large signal power gain.
3256	Small signal power gain.
3261.1	Extrapolated unity gain frequency.
3266	Real part of small-signal short circuit input impedance.
	High frequency tests (3300 series)
3301	Small-signal short-circuit forward-current transfer-ratio cutoff frequency.
3306.3	Small-signal short-circuit forward-current transfer ratio.
3311	Maximum frequency of oscillation.
3320	RF power output, RF power gain, and collector efficiency.
	Electrical characteristics tests for MOS field-effect transistors (3400 series)
3401.1	Breakdown voltage, gate to source.
3403.1	Gate to source voltage or current.
3404	MOSFET threshold voltage.
3405.1	Drain to source on-state voltage.
3407.1	Breakdown voltage, drain to source.
3411.1	Gate reverse current.
3413.1	Drain current.
3415.1	Drain reverse current.
3421.1	Static drain to source on-state resistance.
3423	Small-signal, drain to source on state resistance.
3431	Small-signal, common-source, short-circuit, input capacitance.
3433	Small-signal, common-source, short-circuit, reverse-transfer capacitance.
3453	Small-signal, common-source, short-circuit, output admittance.
3455	Small-signal, common-source, short-circuit, forward transadmittance.
3457	Small-signal, common-source, short-circuit, reverse transfer admittance.
3459	Pulse response (FET).
3461	Small-signal, common-source, short-circuit, input admittance.
3469	Repetitive unclamped inductive switching.
3470.2	Single pulse unclamped inductive switching.
3471.1	Gate charge.
3472.2	Switching time test.
3473.1	Reverse recovery time (t_{rr}) and recovered charge (Q_{rr}) for power MOSFET (drain-to-source) and power rectifiers with $t_{rr} \leq 100$ ns.
3474.1	Safe operating area for power MOSFET's or insulated gate bipolar transistors.
3475.1	Forward transconductance (pulsed dc method) of power MOSFET's or insulated gate bipolar transistors.
3476	Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors.
3477.1	Measurement of insulated gate bipolar transistor total switching losses and switching times.
3478.1	Power transistor electrical dose rate test method.
3479	Short circuit withstand time.
3490	Clamped inductive switching safe operating area for MOS gated power transistors.
	Electrical characteristics tests for Gallium Arsenide transistors (3500 series)
3501	Breakdown voltage, drain to source.
3505	Maximum available gain of a GaAs FET.
3510	1 dB compression point of a GaAs FET.
3570	GaAs FET forward gain (Mag S21).
3575	Forward transconductance.

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Numerical index of test methods - Continued.

Method no.	Title
	Electrical characteristics tests for diodes (4000 series).
4000	Condition for measurement of diode static parameters.
4001.1	Capacitance.
4011.4	Forward voltage.
4016.3	Reverse current leakage.
4021.2	Breakdown voltage (diodes).
4022	Breakdown voltage (voltage regulators and voltage-reference diodes).
4023	Scope display.
*4026.3	Forward recovery voltage and time.
*4031.4	Reverse recovery characteristics.
4036.1	"Q" for voltage variable capacitance diodes.
4041.2	Rectification efficiency.
4046.1	Reverse current, average.
4051.3	Small-signal reverse breakdown impedance.
4056.2	Small-signal forward impedance.
4061.1	Stored charge.
4066.4	Surge current.
4071.1	Temperature coefficient of breakdown voltage.
4076.1	Saturation current.
4081.2	Thermal resistance of lead mounted diodes (forward voltage, switching method).
	Electrical characteristics tests for microwave diodes (4100 series)
4101.3	Conversion loss.
4102	Microwave diode capacitance.
4106	Detector power efficiency.
4111.1	Figure of merit (current sensitivity).
4116.1	IF impedance.
4121.2	Output noise ratio.
4126.2	Overall noise figure and noise figure of the IF amplifier.
4131.1	Video resistance.
4136.1	Standing wave ratio (SWR).
4141.1	Burnout by repetitive pulsing.
4146.1	Burnout by single pulse.
4151	Rectified microwave diode current.
	Electrical characteristics tests for thyristors (controlled rectifiers) (4200 series)
4201.2	Holding current.
4206.1	Forward blocking current.
4211.1	Reverse blocking current.
4216	Pulse response.
4219	Reverse gate current.
4221.1	Gate-trigger voltage or gate-trigger current.
4223	Gate-controlled turn-on time.
4224	Circuit-commutated turn-off time.
4225	Gate-controlled turn-off time.
4226.1	Forward "on" voltage.
4231.2	Exponential rate of voltage rise.
	Electrical characteristics tests for tunnel diodes (4300 series)
4301	Junction capacitance.
4306.1	Static characteristics of tunnel diodes.
4316	Series inductance.
4321	Negative resistance.
4326	Series resistance.
4331	Switching time.

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b. A new sample of devices shall be selected and subjected to the next lower voltage step used. Each device shall be tested using three positive and three negative pulses using each of the pin combinations shown in table 1020-II. A minimum of one-second delay shall separate the pulses.

c. The sample devices shall be electrically tested to group A, subgroup II applicable (room temperature dc parameters).

d. If one or more of the devices fail, the testing of 3.3b. and 3.3c. shall be repeated at the next lower voltage step used.

e. If none of the devices fail, record the failure threshold determined in 3.3a. Note the highest step passed, and use it to classify the device according to table 1020-III.

TABLE 1020-II. Junction polarities for ESD conditions test.

Device type	Junction/polarity
Bipolar transistor (NPN)	E+ to B-
Bipolar transistor (PNP)	E- to B+
Junction FET's (N-channel)	G+ to S-
Junction FET's (P-channel)	G- to S+
MOSFET's (N- or P-channel)	G to S (both polarities)
Gate protected FET's (P-channel)	G to S (both polarities)
Rectifiers (include hot carrier and schottky)	A- to K+
Thyristors	G to K (both polarities)
Unijunctions	G to B1 (both polarities)
Darlingtons	E to B (both polarities)
Small signal diodes	A to K (both polarities)

3.4 Pin combinations to be tested.

Using table 1020-II, select the terminal to be used for the ESD tests.

TABLE 1020-III. Device ESD failure threshold classification.

Class 1	0 volt to 1,999 volts
Class 2	2,000 volts to 3,999 volts
Class 3	4,000 volts to 15,999 volts
Nonsensitive	Above 15,999 volts

3.5 Classification criteria.

Devices which fail the post test electrical at +25°C of group A, subgroup 2 of the detail specification shall be considered class 1 devices.

All devices subjected to this test shall be considered destroyed and shall not be shipped for use in any application.

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4. Summary. The following details shall be specified in the applicable purchase order or contract, if other than specified herein.

a. Post test electricals.

b. Special additional or substitute pin combinations, if applicable.

c. Sample size, if other than three devices.

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METHOD 2037

BOND STRENGTH

1. Purpose. The purpose of this test is to measure bond strengths to determine compliance with specified requirements of the applicable detail specification. This test may be applied to wire-to-die or clip-to-die bond, wire-to-package lead bond, or the wire-to-substrate bond inside the package of wire or clip connected discrete devices bonded by soldering, thermocompression, ultrasonic or related techniques.

2. Apparatus. The apparatus for this test shall consist of suitable equipment for applying the specified force required to cause bond failure. A measurement of the applied stress in grams force (gf) at the point of failure shall be provided by equipment capable of measuring stresses up to and including 10 gf with an accuracy of ±0.25 gf, stresses between 10 and 50 gf with an accuracy of ±0.5 gf, and stresses exceeding 50 gf with an accuracy of 5 percent of indicated value.

3. Procedure. The test shall be conducted using the test conditions specified. All bond pulls shall be counted and the specified sampling, acceptance and added sample provisions shall be observed, as applicable. Unless otherwise specified, the sample plan specified for the bond strength test shall determine the minimum sample size in terms of the minimum number of pulls to be accomplished rather than the number of complete devices in the sample (e.g., wires for test condition A, bonds for test condition B, and clips for test condition C). Where there is any adhesive, encapsulant, or other material used on the die to increase the apparent bond strength, the bond strength test shall be performed prior to application or, for post seal tests, the material shall be removed. Unless nondestructive limits are specified, all bond pulls shall be to destruction.

3.1 Test conditions.

3.1.1 Test condition A: Wire pull, double bond. This test is normally employed for internal bonds at the die or substrate and the lead posts of discrete devices. Under this condition, both bonds are tested simultaneously by inserting a hook under the lead wire and, with the device clamped, applying the pulling force at mid-point of the wire span. The force shall be applied in the upward direction tending to cause a lift-off separation of the bond from the die and within 5° of perpendicular to: (1) the plane of the die or substrate or, (2) to a straight line between the two bonds. When a failure occurs, the force causing the failure and the failure category shall be recorded.

3.1.2 Test condition B: Wire pull, single bond (not recommended for wire diameters less than .005 inch (0.125 mm)). This test is employed when it is desired to test the wire bonds separately at the die or substrate and lead post or when, due to device construction, condition A is inappropriate. Product acceptance is based on testing an equal number of both bonds. When testing die and post bonds separately, the wire shall be cut to provide two ends accessible for pull testing both die and post bonds. In the case of short wire runs, it may be necessary to cut the wire close to one termination in order to allow pull at the opposite termination. The free end of the wire shall be gripped in a suitable device and simple pulling action applied. When the wire exits from the top of the die bond (ball or nailhead bonds), the force shall be applied in a direction that is within 5° of normal to the surface of the die or substrate. When the wire exits from the side of the bond (die or lead post), the force shall be applied at an angle equal to or greater than 45° to the surface of the die. When failure occurs, the force causing the failure and failure category shall be recorded.

3.1.3 Test condition C: Clip pull. This test is employed for internal clips at the die or substrate and the lead posts of discrete devices. The pull is applied by inserting a hook under the clip as close to the die attachment point as practical with the device clamped and the pulling force applied approximately in a direction within 5° of normal to the die or substrate. When a failure occurs, the force causing the failure and the failure category shall be recorded.

3.2 Failure criteria. Any bond pull which results in a separation under an applied stress less than that indicated in table 2036.1 as the required minimum bond strength for the indicated test condition, composition, and construction shall constitute a failure.

3.2.1 Failure category.

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3.2.1.1 Failure categories for wire bonds. Failure categories for wire bonds are as follows:

a. Wire break at neckdown point (reduction of cross section due to bonding process).

b. Wire break at point other than neckdown.

c. Failure in bond (interface between wire and metallization at die).

d. Failure in bond (interface between wire and plating or metallization) at package post, substrate, or other than at the die.

e. Lifted metallization from die.

f. Lifted metallization or plating from substrate or package post.

g. Fracture of die.

h. Fracture of substrate.

3.2.1.2 Failure categories for clips. Failure categories for clip are as follows:

a. Failure in bond (interface between clip and metallization) at die.

b. Lifted metallization at die.

c. Separation of clip from package post.

d. Fracture of die.

The stress required to achieve separation and the category of the separation or failure shall be recorded.

3.3 Procedure in the event of production sampling failure (unencapsulated devices). If a sample contains more than the allowed number of defects, the machine(s) from which the sample was taken shall not be allowed to produce additional JAN product until a sample has been tested and passed. All devices bonded on the machine(s) that produced the defective(s) since the last acceptable sample inspection will either be rejected or subjected to a 100 percent non-destructive bond pull at a force of one-half the minimum specified bond pull limit for the particular size wire (see table 2037-I or figure 2037-1). A non-destructive pull force of $X - 30\sigma/2$ may be substituted for this value provided $\sigma \leq 0.2$ X. The statistical data for this shall be obtained from actual pull data from the last full acceptable days production. X is the average pull strength and σ is the standard deviation. If 99.999 percent pure aluminum annealed wire is used, the divisor in the equation shall be changed to three and the sentence above will then read "one-third the minimum specified bond pull limit." This procedure shall not be used if the defectives resulted from die fracture since this may indicate damage to the die which cannot be screened by non-destructive testing.

4. Summary. The following details shall be specified in the detail specification:

a. Test condition letter (see 3.).

b. Minimum bond strength, if other than as specified in 3.2 or details of required strength distributions, if applicable.

c. LTPD or number and selection of bond pulls to be tested on each device, and number of devices, if other than 10.

d. Requirements for reporting of separation forces and failure categories, when applicable (see 3.2.1).

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METHOD 1001.2

BAROMETRIC PRESSURE (REDUCED)

1. Purpose. The purpose of this test is to check the device capabilities under conditions simulating the low pressure encountered in the nonpressurized portions of aircraft in high altitude flight.

2. Apparatus. The apparatus used for the barometric-pressure test shall consist of a vacuum pump and a suitable sealed chamber having means for visual observation of the specimen under test when necessary. A suitable pressure indicator shall be used to measure the simulated altitude in feet in the sealed chamber.

3. Procedure. The specimens shall be mounted in the test chamber as specified and the pressure reduced to the value indicated in one of the following test conditions, as specified. Previous references to this method do not specify a test condition; in such cases, test condition B shall be used. While the specimens are maintained at the specified pressure, and after sufficient time has been allowed for all entrapped air in the chamber to escape, the specimens shall be subjected to the specified test.

Test condition	Pressure - Maximum		Altitude	
	Inches of mercury	Millimeters of mercury	Feet	Meters
A - - - - - - -	8.88	226.00	30,000	9,144
B - - - - - - -	3.44	87.00	50,000	15,240
C - - - - - - -	1.31	33.00	70,000	21,336
D - - - - - - -	0.315	8.00	100,000	30,480
E - - - - - - -	0.043	1.09	150,000	45,720
F - - - - - - -	17.300	439.00	15,000	4,572
G - - - - - - -	9.436×10^{-8}	2.40×10^{-6}	656,000	200,000

In addition the following is required:

a. Twenty minutes before and during the test, the test temperature shall be +25°C ±3°C.

b. The specified voltage shall be applied and monitored over the range from atmospheric pressure to the specified minimum pressure and returned so that any device malfunctions, if they exist, will be detected.

4. Failure criteria. A device which exhibits arc-overs, harmful coronas, or any other defect or deterioration that may interfere with the operation of the device shall be considered a failure.

5. Summary. The following conditions must be specified in the detail specification:

a. Voltage (see 2.).

b. Minimum pressure (see 2.).

METHOD 1011.1

IMMERSION

1. Purpose. This test is performed to determine the effectiveness of the seal of component parts. The immersion of the part under evaluation into liquid at widely different temperatures subjects it to thermal and mechanical stresses which will readily detect a defective terminal assembly, or a partially closed seam or molded enclosure. Defects of these types can result from faulty construction or from mechanical damage such as might be produced during physical or environmental tests. The immersion test is generally performed immediately following such tests because it will tend to aggravate any incipient defects in seals, seams, and bushings which might otherwise escape notice. This test is essentially a laboratory test condition, and the procedure is intended only as a measurement of the effectiveness of the seal following this test. The choice of fresh or salt water as a test liquid is dependent on the nature of the component part under test. When electrical measurements are made after immersion cycling to obtain evidence of leakage through seals, the use of a salt solution instead of fresh water will facilitate detection of moisture penetration. This test provides a simple and ready means of detection of the migration of liquids. Effects noted can include lowered insulation resistance, corrosion of internal parts, and appearance of salt crystals. The test described is not intended as a thermal-shock or corrosion test, although it may incidentally reveal inadequacies in these respects.

2. Procedure. The test consists of successive cycles of immersions, each cycle consisting of immersion in a hot bath of fresh (tap) water at a temperature of 65°C +5°C,-0°C (149°F +9°F, -0°F) followed by immersion in a cold bath. The number of cycles, duration of each immersion, and the nature and temperature of the cold bath shall be as indicated in the applicable test condition listed in table 1011-1, as specified.

Test Condition	Number of cycles	Duration of each immersion (Minutes)	Immersion bath (cold)	Temperature of cold bath (°C)
A - - - - - -	2	15	Fresh (tap) water	25, +10, -5
B - - - - - -	2	15	Saturated solution of sodium chloride and water.	25, +10, -5
C - - - - - -	5	60	Saturated solution of sodium chloride and water.	0 ± 3

The transfer of specimens from one bath to another shall be accomplished as rapidly as practicable. After completion of the final cycle, specimens shall be thoroughly and quickly washed and all surfaces wiped or air-blasted clean and dry.

3. Measurements. Unless otherwise specified, measurements shall be made at least 4 hours, but not more than 24 hours, after completion of the final cycle. Measurements shall be made as specified.

4. Summary. The following details are to be specifed in the individual specification:

a. Test condition letter (see 2).

b. Time after final cycle allowed for measurements, if other than that specified (see 3).

c. Measurements after final cycle (see 3).

METHOD 1015.1

STEADY-STATE PRIMARY PHOTOCURRENT IRRADIATION PROCEDURE (ELECTRON BEAM)

1. Purpose. This test procedure establishes the means for measuring the steady-state primary photocurrent (I_{PH}) enerated in semiconductor devices when these devices are exposed to ionizing radiation. In this test method, the test device is irradiated in the primary electron beam of a linear accelerator (LINAC).

1.1 Definitions. The following definitions shall apply for this test method.

1.1.1 Primary photocurrent (I_{PH}). The flow of excess charge carriers across a P-N junction due to ionizing radiation creating electron-hole pairs in the vicinity of the P-N junction.

1.1.2 Measurement interferences. A current measured in the test circuits that does not result from primary photocurrent (see appendix).

2. Apparatus.

2.1 Ionizing pulse source. The ionizing pulse shall be produced by an electron LINAC. The ionizing pulse shall have dose rate variations within ±15 percent of nominal during the pulse and shall consist of electrons with an energy equal to or greater than 10 MeV.

2.2 Pulse recording equipment. Pulse recording equipment shall be provided that will display and record both the photocurrent and the pulse-shape monitor signal. It may consist of oscilloscopes with recording cameras, appropriate digitizing equipment, or other approved recording equipment. The equipment shall have an accuracy and resolution of five percent of the pulse width and maximum amplitude of the ionizing source.

2.3 Test circuits. One of the following test circuits shall be selected, radiation-shielded, and close enough to the DUT in order to meet the requirements of 3.2.

2.3.1 Resistor sampling circuits. The resistor sampling circuits shall be as shown on figure 1015-1.

2.3.2 Current transformer circuit. The current transformer circuit shall be as shown on figure 1015-2.

2.4 Irradiation pulse-shape monitor. One of the following devices shall be used to develop a signal proportional to the dose rate delivered to the DUT. Any time constants which degrade the linear response of the monitor signal shall be less than 10 percent of the beam pulse width. The dose rate at the monitor shall be proportional to the dose rate at the DUT and the variation from proportionality shall not exceed ±3 percent.

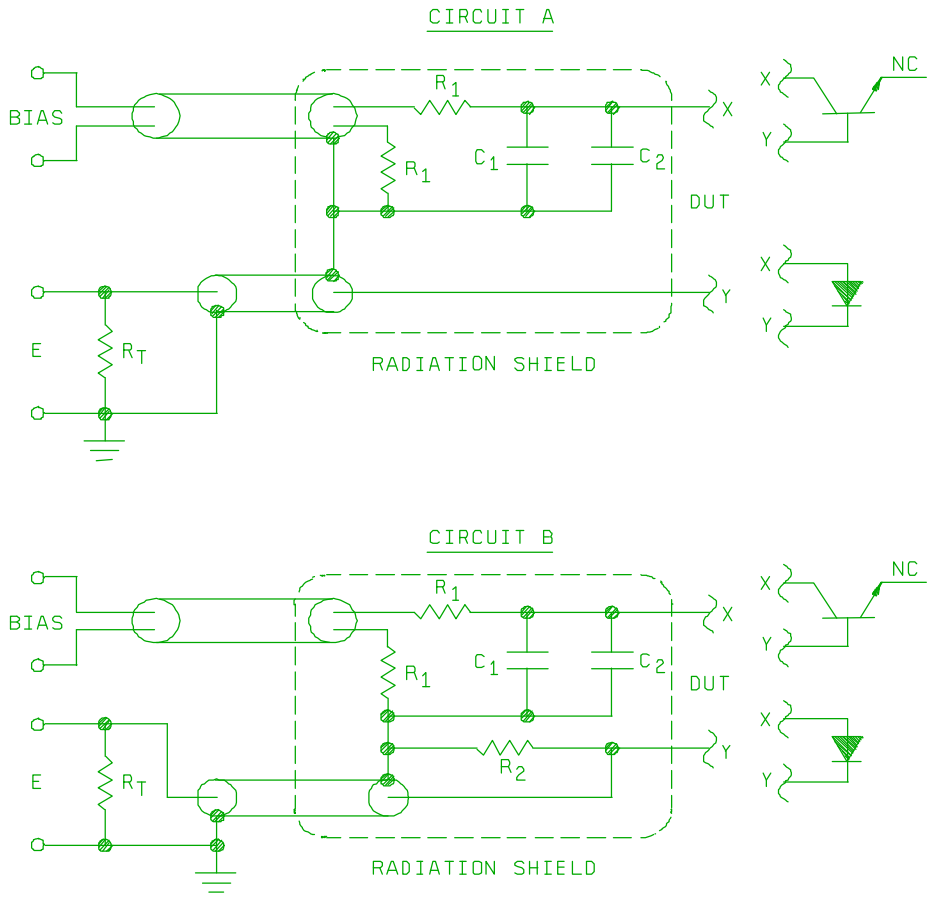
2.4.1 Signal diode. The signal diode selected shall have a response that is linear within ±5 percent of the dose rate over the selected irradiation range. Depending on the sensitivity of the diode, it may be positioned at a point within the beam from the ionizing source at which it will remain in the linear region. The signal diode shall be placed in one of the test circuits described in 2.3, and it shall be back biased at not more than fifty percent of the diode breakdown voltage.

2.4.2 P-type-intrinsic-N-type (P-I-N) diode. A P-I-N diode shall be used as stated in 2.4.1.

2.4.3 Current transformer. A transformer with a hollow central axis that shall be mounted around the output of the ionizing source.

2.4.4 Secondary-emission monitor. The secondary-emission monitor shall consist of a thin foil mounted in a chamber evacuated to ≤.134 Pa (0.01 mmHg) which is located in the path of the beam from the ionizing source. The foil shall be biased negatively with respect to ground, or shielded with positively biased grids.

2.5 Dosimeter. The dosimeter shall be used to calibrate the output of the pulse-shape monitor in terms of dose rate. The dosimeter type shall be a commercial thermoluminescent detector (TLD), thin calorimeter or other system as specified. The dosimetry measurement technique shall be accurate to ±20 percent.



NOTES:

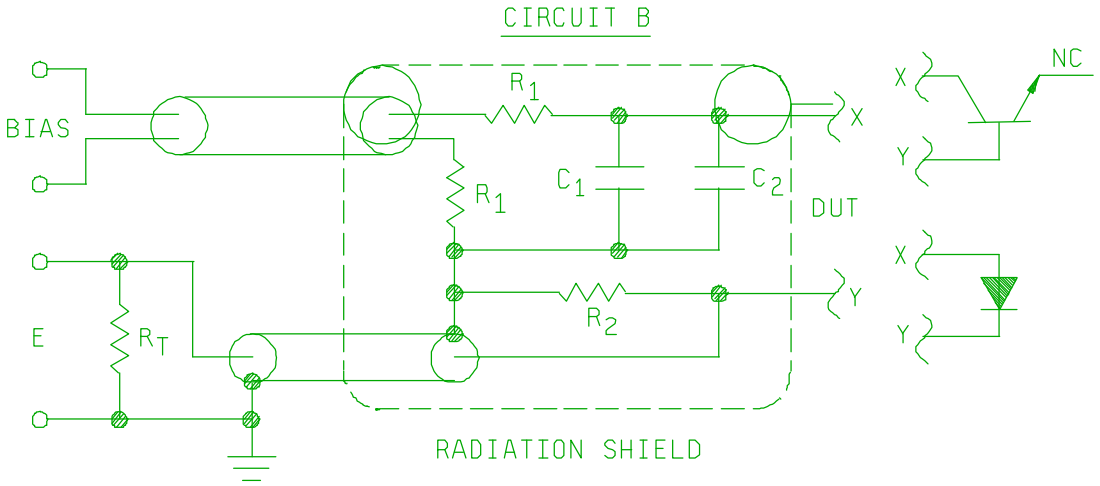
1. R_1 = 1,000 Ω, 5 percent.
2. R_2 = 5 Ω, 1 percent.
3. C_1 = 15 μF, 5 percent.
4. C_2 = .01 μF, 5 percent.
5. R_T = Characteristic termination for coaxial cable.
6. Circuit B shall be used for large photocurrents (those for which more than 10 percent of the bias appears across resistor R_T in circuit A).
7. Photocurrent for circuit A:

$$I_{PH} = \frac{\text{Steady-state signal } (E)}{\text{Cable termination } (R_T)}$$

8. Photocurrent for circuit B:

$$I_{PH} = \frac{[\text{Steady-state signal } (E)][\text{Cable termination } (R_T) + R_2]}{[\text{Cable termination}(R_T)][R_2]}$$

FIGURE 1015-1. Resistor sampling circuits.



NOTES:

1. R_1 = 1,000 Ω, 5 percent.
2. C_1 = 15 μF, 5 percent.
3. C_2 = .01 μF, 5 percent.
4. R_T = Characteristic termination for coaxial cable.
5. Photocurrent calculation:

$$I_{PH} = \frac{\textit{Steady - state signal (E)}}{\textit{Sensitivity of current transformer}}$$

FIGURE 1015-2. Current transformer circuit.

3. Procedure.

3.1 General. The test facility shall select a test fixture and pulse shape monitor. The test fixture and monitor shall be aligned with the beam from the ionizing source. In addition, any shielding, collimation, or beam scattering equipment shall be properly positioned. If repositioning of any equipment or the test circuit is required to accomplish the device testing, the repositioning shall be demonstrated to be reliable and repeatable.

3.2 Test circuit check-out. The ionizing source shall be pulsed either with an empty device package or without the DUT in the test circuit and with all required bias applied. The ionizing source shall be adjusted to supply the dose rate required for this test. The recorded current from the pulse recording equipment shall be no more than 10 percent of the steady-state photocurrent expected to be measured for this test (see 3.4.3). If this condition is not met, see appendix.

3.3 Ionizing source calibration. Mount the selected dosimeter in place of the DUT. Pulse the ionizing source, record the pulse-shape monitor signal, and determine the radiation dose measured by the dosimeter. Calculate a dose rate factor as follows:

$$Doseratefactor = \frac{Measureddosimeterdose[rad(Si)]}{Integratedpulseshapemonitorsignal(voltsxseconds)}$$

This measurement shall be repeated five times, and the average of the six dose rate factors obtained shall be the dose rate factor used for the test. One dosimeter may be used repetitively if the dose is read for each pulse.

3.4 Device test.

3.4.1 Mounting. Mount the DUT in the beam from the ionizing source and connect it to the rest of the test circuit. The bias applied shall be as specified in the device specification; or if not specified, the bias shall be fifty percent of the specified breakdown voltage of the DUT.

3.4.2 Dose rate. Either adjust the ionizing source beam current or use an alternate method (i.e., scatterers or a different sample location) to obtain the specified dose rate ±20 percent. Pulse the ionizing source and record the pulse-shape monitor signal and the photocurrent signal from the DUT.

3.4.3 Calculate photocurrent. The steady-state photocurrent shall be calculated as expressed on the figure selected for the test circuit in 2.3.

3.4.4 Verify test circuit. Check the current recorded in the test circuit in 3.2 and verify that the value of the current does not exceed 10 percent of the photocurrent recorded in 3.4.3.

3.5 Test circuit checkout. Repeat the device test (see 3.4) for each dose rate that is required by the device specification. The calibration (see 3.3) shall be performed for each dose rate to be tested. The test circuit checkout (see 3.2) shall be performed when a new device type is tested or when any change is made in the position of the test circuit or DUT supporting structure.

4. Summary. The following conditions shall be specified in the detail specification:

a. The pulse width requirements of the ionizing pulse source. (The pulse width must exceed the semiconductor minority lifetime by at least a factor of 2.)

b. The bias applied to the device (see 3.4.1).

c. The irradiation dose rate(s) applied (see 3.4.2).

d. When required, any total dose restrictions.

e. When required, a description of the placement of the device in the beam with respect to the junction.

f. When required, for multi-junction devices, the device terminals that are to be monitored.

g. When required, the procedure for approval of the test facility and dosimetry.

APPENDIX

MEASUREMENT INTERFERENCES

The following problems commonly arise when electronics are tested in a radiation environment. Most of these interferences are present when the test circuit is irradiated under bias with the DUT removed.

1. Air ionization.

The irradiation pulse can ionize the air around the test circuit and provide a spurious conduction path. The air ionization contribution to the signal is proportional to the applied bias. The effect of air ionization is minimized by reducing the circuit components exposed to the beam pulse, by coating exposed leads with a thick nonconducting layer or by performing the test in a vacuum.

2. Secondary emission.

The beam pulse irradiating any electrical lead or component can cause a net charge to enter or leave the exposed surfaces. This spurious current alters the measured photocurrent. Secondary emission effects are reduced by minimizing the circuit components exposed to the direct beam.

3. Perturbed irradiation field.

Any material exposed to the beam pulse will scatter and modify the incident radiation of the beam. A nearby DUT or dosimeter will then be exposed to a noncharacterized and unexpected form of radiation. These field perturbations are reduced by minimizing the mass of the structure supporting the DUT and the dosimeter that is exposed to the beam. All materials should have a low atomic number; e.g., plastics and aluminum.

4. RF pickup.

The ionizing pulse source discharges large amounts of electromagnetic energy at the same time the photocurrent is being measured. Good electrical practice is necessary to eliminate resonant structure, noise pick-up on signal cables, common mode pick-up, ground loops, and similar interferences.

METHOD 1021.3

MOISTURE RESISTANCE

1. Purpose. The moisture resistance test is performed for the purpose of evaluating, in an accelerated manner, the resistance of component parts and constituent materials to the deteriorative effects of the high-humidity and heat conditions typical of tropical environments. Most tropical degradation results directly or indirectly from absorption of moisture vapor and films by vulnerable insulating materials, and from surface wetting of metals and insulation. These phenomena produce many types of deterioration, including corrosion of metals; constituents of materials; and detrimental changes in electrical properties. This test differs from the steady-state humidity test and derives its added effectiveness in its employment of temperature cycling, which provides alternate periods of condensation and drying essential to the development of the corrosion processes and, in addition, produces a "breathing" action of moisture into partially sealed containers. Increased effectiveness is also obtained by use of a higher temperature, which intensifies the effects of humidity. The test includes a low-temperature subcycle that acts as an accelerant to reveal otherwise undiscernible evidences of deterioration since stresses caused by freezing moisture tend to widen cracks and fissures. As a result, the deterioration can be detected by the measurement of electrical characteristics (including such tests as voltage breakdown and insulation resistance) or by performance of a test for sealing. Provision is made for the application of a polarizing voltage across insulation to investigate the possibility of electrolysis, which can promote eventual dielectric breakdown. This test also provides for electrical loading of certain components, if desired, in order to determine the resistance of current-carrying components, especially fine wires and contacts, to electrochemical corrosion. Results obtained with this test are reproducible and have been confirmed by investigations of field failures. This test has proved reliable for indicating those parts which are unsuited for tropical field use.

2. Apparatus. The apparatus used for the moisture resistance test shall include temperature-humidity chambers capable of maintaining the cycles and tolerance described on figure 1021-1 and electrical test equipment capable of performing the measurements in 3.6 and 4.

3. Procedure. Specimens shall be tested in accordance with 3.2 through 3.7 inclusive, and figure 1021-1. Specimens shall be mounted in a manner that will expose them to the test environment.

3.1 Initial conditioning. Unless otherwise specified and prior to mounting specimens for the moisture resistance test, the device leads shall be subjected to a bending stress, initial conditioning in accordance with test condition E of method 2036. Where the specific sample devices being subjected to the moisture resistance test have already been subjected to the required initial conditioning, as part of another test employing the same sample devices, the lead bend need not be repeated.

3.2 Initial measurements. Prior to step 1 of the first cycle, the specified initial measurements shall be made at room ambient conditions, or as specified. When specified, the initial conditioning in a dry oven (see figure 1021-1) shall precede initial measurements and the initial measurements shall be completed within 8 hours after removal from the drying oven.

3.3 Number of cycles. Specimens shall be subjected to 10 continuous cycles, each as shown on figure 1021-1. In the event of no more than one unintentional test interruption (power interruption or equipment failure) prior to the completion of the specified number of cycles (except for the last cycle) the cycle shall be repeated and the test may continue. Unintentional interruptions occurring during the last cycle require a repeat of the cycle plus an additional uninterrupted cycle. Any intentional interruption, or any unintentional interruption of greater than 24 hours requires completion of missing cycles plus one additional cycle.

3.4 Subcycle of step 7. During at least 5 of the 10 cycles, a low temperature subcycle shall be performed. At least 1 hour but not more than 4 hours after step 7 begins, the specimens shall be either removed from the humidity chamber, or the temperature of the chamber shall be reduced, for performance of the subcycle. Specimens during the subcycle shall be conditioned at -10°C +2°C, -5°C, with humidity not controlled, for 3 hours minimum as indicated on figure 1021-1. When a separate cold chamber is not used, care should be taken to assure that the specimens are held at -10°C +2°C, -5°C for the full period. After the subcycle, the specimens shall be returned to 25°C at 80 percent RH minimum and kept there until the next cycle begins.

3.5 Applied voltage. During the moisture resistance test as specified on figure 1021-1, when specified (see 4), the device shall be biased in accordance with the specified bias configuration which should be chosen to maximize the voltage differential between chip metallization runs or external terminals, minimize power dissipation and to utilize as many terminals as possible to enhance test results.

3.6 Conditions (see figure 1021-1). The rate of change of temperature in the chamber is unspecified; however, specimens shall not be subject to the radiant heat from the chamber conditioning processes. Unless otherwise specified, the circulation of air in the chamber shall be at a minimum cubic rate per minute equivalent to five times the volume of the chamber. The steady-state temperature tolerance is ±2°C of the specified temperature at all points within the immediate vicinity of the specimens and at the chamber surfaces. Specimens weighing 25 pounds or less shall be transferred between temperature chambers in less than 2 minutes.

3.7 Final measurements. Following step 6 of the final cycle (or step 7 if the subcycle of 3.3 is performed during the tenth cycle), devices shall be conditioned for 24 hours at room ambient conditions after which either an insulation resistance test in accordance with method 1016, or the specified 25°C electrical end-point measurements shall be performed. Electrical measurements may be made during the 24 hour conditioning period. However, any failures resulting from this testing shall be counted, and any retesting of these failures later in the 24 hour period for the purpose of obtaining an acceptable result is prohibited. No other test (e.g., seal) shall be performed during the 24 hour conditioning period. The insulation resistance test or the alternative 25°C electrical end-point measurements shall be completed within 48 hours after removing the devices from the chamber. When the insulation resistance test is performed, the measured resistance shall be no less than 10 MΩ and the test shall be recorded and data submitted as part of the end-point data. If the package case is electrically connected to the die substrate by design, the insulation resistance test shall be omitted and the specified 25°C electrical end-point measurements shall be completed within 48 hours after removal of the device from the chamber. A visual examination and any other specified end-point electrical parameter measurements (see 4.c) shall also be performed.

3.8 Failure criteria. No device shall be acceptable that exhibits:

a. Specified markings which are missing in whole or in part, faded, smeared, blurred, shifted, or dislodged to the extent that they are not legible. This examination shall be conducted with normal room lighting and with a magnification of 1X to 3X.

b. Evidence of corrosion over more than five percent of the area of the finish or base metal of any package element (i.e., lid, lead, or cap) or any corrosion that completely crosses the element when viewed with a magnification of 10X to 20X.

c. Leads missing, broken, or partially separated.

d. Corrosion formations which bridge between leads or between leads and metal case.

e. Electrical end-point or insulation resistance test failures.

NOTE: The finish shall include the package and entire exposed lead area from meniscus to the lead tip (excluding the sheared off tip itself) and all other exposed metal surfaces.

4. Summary. The following details shall be specified in the applicable acquisition document:

a. Initial measurements and conditions, if other than room ambient (see 3.1).

b. Applied voltage, when applicable (see 3.5), and bias configuration, when required. This bias configuration shall be chosen in accordance with the following guidelines:

(1) Only one supply voltage (V) either positive or negative is required, and an electrical ground (GND) or common terminal. The magnitude of V will be the maximum such that the specified absolute maximum ratings are not exceeded and test conditions are optimized.

(2) Unless otherwise specified, all normally specified voltage terminals and ground leads shall be connected to GND.

(3) Unless otherwise specified, all data inputs shall be connected to V. The polarity and magnitude of V is chosen to minimize internal power dissipation and current flow into the device. Unless otherwise specified, all extender inputs shall be connected to GND.

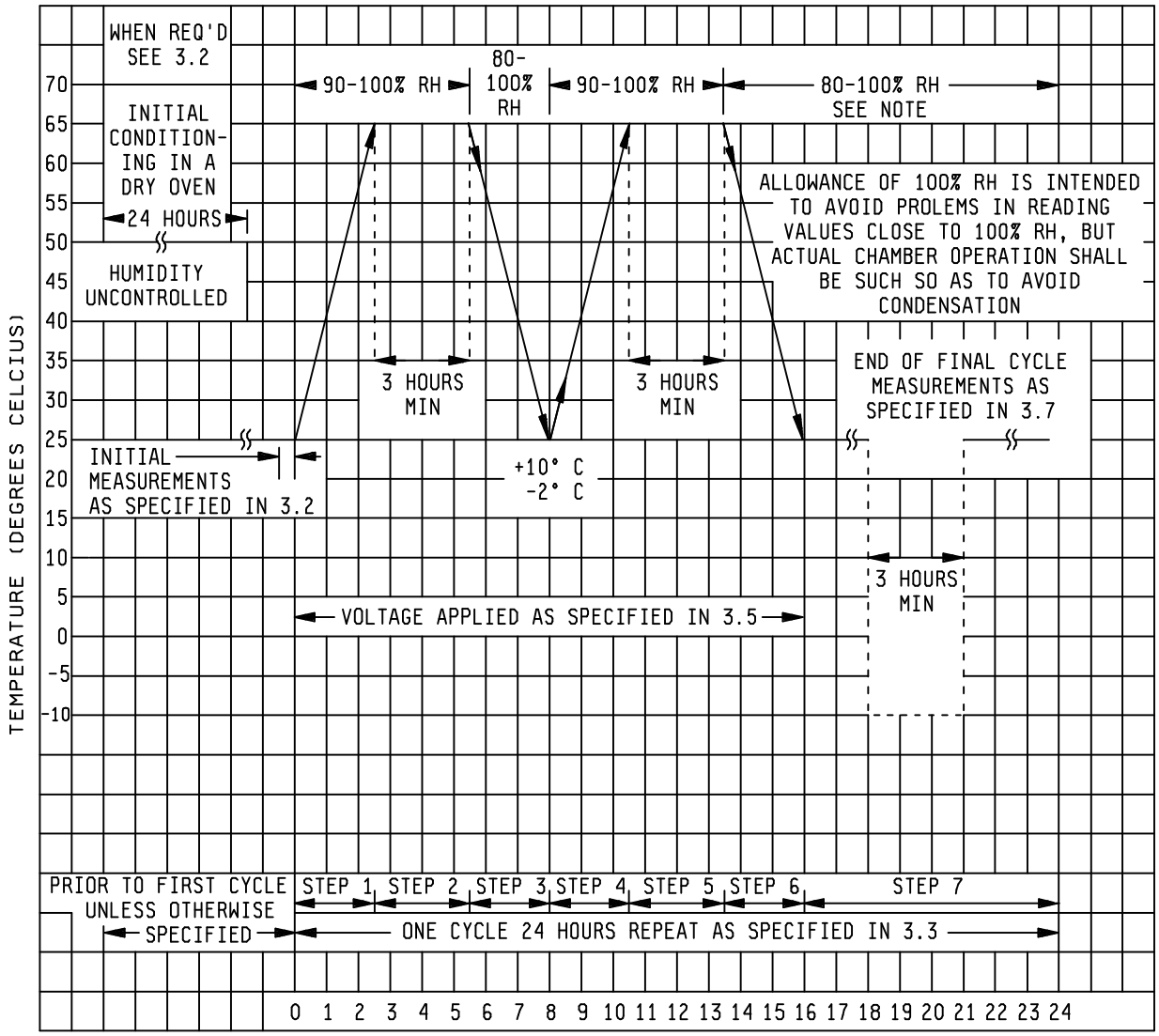
(4) All additional leads (e.g. clock, set, reset, outputs) considered individually, shall be connected to V or GND, whichever minimizes current flow.

(5) Leads with no internal connection shall be biased to V or GND whichever is opposite to an adjacent lead.

c. Final measurements (see 3.7). Final measurements shall include all electrical characteristics and parameters which are specified as end-point electrical parameters.

d. Number of cycles, if other than 10 (see 3.3).

e. Conditioning in dry oven before initial measurements, if required (see 3.2).



NOTE: The subcycle of step 7 (See 3.4) shall be performed for a minimum of 5 of the 10 cycles. Humidity is uncontrolled for the -10°C portion of step 7.

FIGURE 1021-1. Graphical representation of moisture-resistance test.

METHOD 1038.4

BURN-IN (FOR DIODES, RECTIFIERS, AND ZENERS)

1. Purpose. This test is performed to eliminate marginal devices or those with defects resulting from manufacturing aberrations that are evidenced as time and stress dependent failures. Without the burn-in, these defective devices would be expected to result in early lifetime failures under normal use conditions. It is the intent of this test to operate the semiconductor device at specified conditions to reveal electrical failure modes that are time and stress dependent.

a. HTRB screens for mobile or temperature activated impurities within (and without) the device's passivation layers. It is equally effective on most device types including diodes, rectifiers, zeners, and transient voltage suppressors.

b. SSOP, when properly specified, simulates actual device operation but with accelerated conditions. Some of the elements of HTRB are combined with screening for die bond integrity. It is effective on some device types including diodes, rectifiers, and zeners. The conditions used for zeners provide the desired HTRB screen concurrently with the SSOP screen.

2. Mounting. Unless otherwise specified in the detail specification, mounting shall be in accordance with the following.

2.1 Test condition A, HTRB. The method of mounting is usually optional for high temperature bias since little power is dissipated in the device. (Devices with normally high reverse leakage current may be mounted to heat sinks to prevent thermal run-away conditions.)

2.2 Test condition B, SSOP.

a. Devices with leads projecting from the body (e.g., axial) shall be mounted by their leads at least .375 inch (9.73 mm) from the body or lead tabulation.

b. Unless otherwise specified, devices designed for case mounting (e.g., stud, flange, and disc) shall be mounted by the stud or case according to the design specifications for the package. Care must be exercised to avoid stressing or warping of the package. Thermally conductive compounds may optionally be used provided that they are removed afterwards and do not leave a residue on the package.

c. Surface mount types shall be held by their electrical terminations.

3. Procedure. The semiconductor device shall be subjected to the burn-in at the temperature and for the time specified herein or on the detail specification. Pre-burn-in measurements shall be made as specified. The failure criteria shall be as specified in the appropriate detail specification. If measurements cannot be performed within the specified time, the devices shall be subjected to the same test conditions for a minimum of 24 additional hours before test measurements are performed.

3.1 Test condition A, HTRB. Unless otherwise specified, HTRB is performed with the cathode positively biased at an artificially elevated temperature for 48 hours minimum. These conditions apply to both rectifiers and to avalanche and zener voltage regulators.

a. The junctions of rectifiers shall be reverse biased at 50 to 80 percent in accordance with figure 1038-1 of their rated working peak reverse voltage; avalanche and zener voltage regulators, when specified, shall be reverse biased at 80 percent of their minimum avalanche or zener voltages except when voltage exceeds 2,500, see figure 1038-1. The reverse bias shall be a dc bias with less than 20 percent ripple except where rectified (pulsating) dc is permitted. The ambient or case test temperature shall be as specified (normally +150°C for silicon devices) (see figure 1038-1).

b. At the end of the high-temperature test time, as specified, the ambient temperature shall be lowered. The test voltage shall be maintained on the devices until a case temperature of +30°C ±5°C is attained. Testing shall be completed within 24 hours after the removal of voltage. After removal of the bias voltage, no other voltage shall be applied to the device before taking the post HTRB reverse current measurement. Post HTRB measurements shall be taken as specified.

Uni-directional transient voltage suppressors shall be treated as avalanche and zener voltage regulators for the purposes of conducting HTRB.

Bi-directional transient voltage suppressors shall be treated as two discrete avalanche or zener voltage regulators (when specified) with each polarity taking turns receiving HTRB and post HTRB testing. Post HTRB testing of one must be completed before reversing the device and commencing HTRB with opposite polarity bias voltage. The second polarity may be achieved either electrically or by mechanically reversing the devices.

3.2 Test condition B, steady-state operating power. Unless otherwise specified, the devices shall be subjected to the maximum rated test conditions for a minimum of 96 hours. The test temperature shall be as specified. Unless otherwise specified, post burn-in readings shall be taken within 96 hours. If ambient temperature is specified, it shall comply with the general requirements for HTRB or burn-in of this specification (see 4.5). The following indicates the test conditions to be specified for each of the three types of power burn-in tests:

a. Rectifying test. Unless otherwise specified, average rectified current, peak reverse voltage, frequency, and temperature (case, junction, or ambient) are as specified in the detail specification.

b. Forward bias test. Unless otherwise specified, forward current and temperature (case or junction) are as specified in the detail specification.

c. Voltage regulator (zener) test. Unless otherwise specified, voltage regulator diode current and temperature (case or junction) are as specified in the slash drawing. At the end of the test time, the power level shall be reduced to five percent of the operating level. If the ambient is artificially elevated, it shall also be reduced to room temperature. The object is to let the devices cool down under bias. When the junction or case temperature has stabilized to below +50°C, the bias may be removed and the devices tested within 96 hours after removal of reverse bias. No other voltage may be applied to the devices until completion of electrical test.

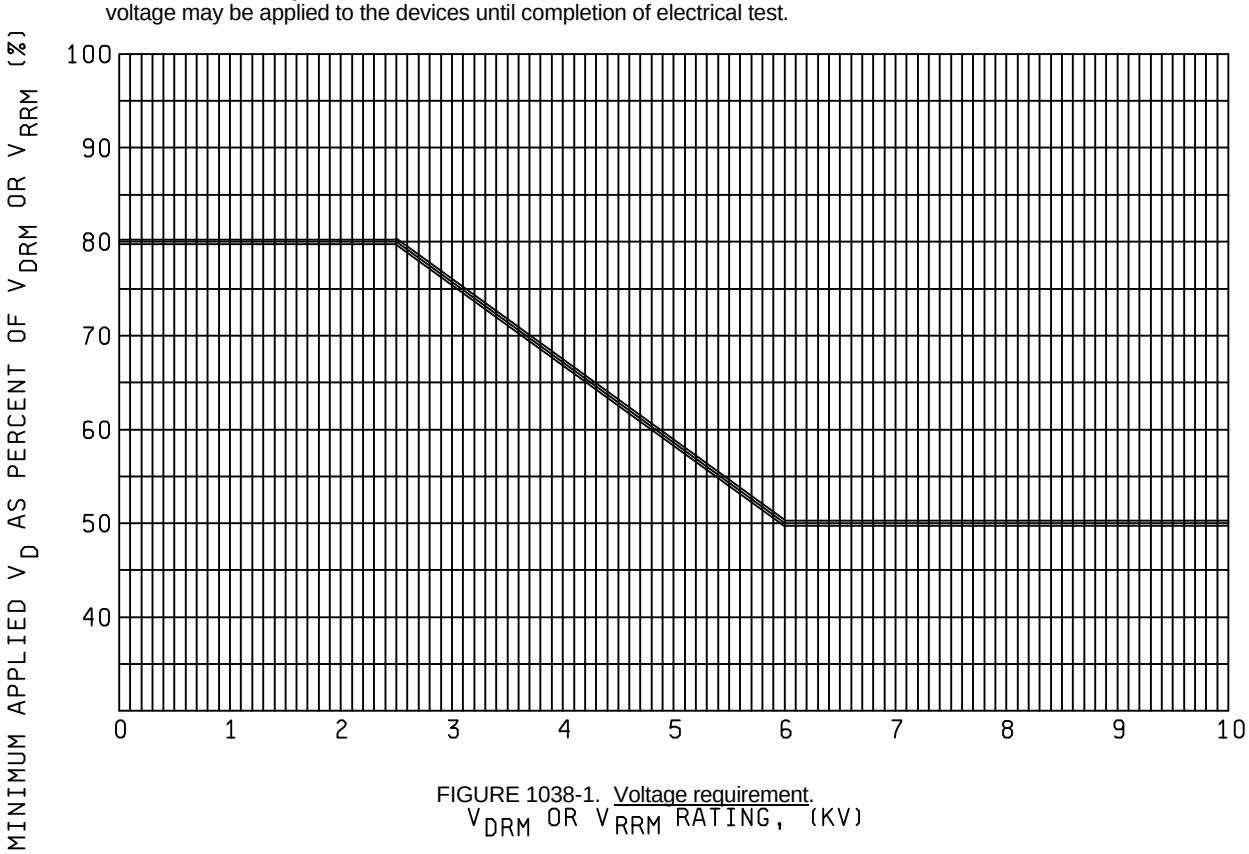


FIGURE 1038-1. Voltage requirement.

4. Summary. The test condition letter (A or B) and the following details shall be specified in the applicable detail specification.

4.1 Test condition A, HTRB.

a. Test temperature (see 3.1).

b. Test conditions (see 2.1 and 3.1).

c. Test time (see 3.1).

d. Preburn-in and post burn-in measurements (see 3. and 3.1).

e. Time for completion of post burn-in measurements, if other than 24 hours (see 3.1).

f. Criteria for failure (see 3.).

4.2 Test condition B, steady-state operating power.

a. Test temperature (see 3.2).

b. Test conditions (see 2.2 and 3.2).

c. Burn-in time if other than 96 hours (see 3.2).

d. Pre-burn-in and post burn-in measurements (see 3. and 3.2).

e. Time for completion of post burn-in measurements, if other than 96 hours (see 3.2).

f. Criteria for failure (see 3.).

METHOD 1046.3

SALT SPRAY (CORROSION)

1. Purpose. This test is proposed as an accelerated laboratory corrosion test simulating the effects of seacoast atmosphere on devices. This test can also be used to detect the presence of free iron contaminating the surface of another metal, by inspection of the corrosion products.

2. Apparatus. Apparatus used in the salt-spray test shall include the following:

a. Exposure chamber with racks for supporting specimens.

b. Salt-solution reservoir with means for monitoring an adequate level of solution.

c. Means for atomizing the salt solution, including suitable nozzles and compressed-air supply.

d. Chamber-heating means and control.

e. Means for humidifying the air at a temperature above the chamber temperature.

2.1 Chamber. The chamber and all accessories shall be made of material which will not affect the corrosiveness of the fog, such as glass, hard rubber, or plastic. Wood or plywood should not be used because they are resiniferous. Materials should not be used if they contain formaldehyde or phenol in their composition. In addition, all parts which come in contact with test specimens shall be of materials that will not cause electrolytic corrosion. The chamber and accessories shall be so constructed and arranged that there is no direct impinging of the spray or dripping of the condensate on the specimens, so that the spray circulates freely about all specimens to the same degree, and so that no liquid which has come in contact with the test specimens returns to the salt-solution reservoir. The chamber shall be properly vented to prevent pressure build up and allow uniform distribution of salt spray. The discharge end of the vent shall be protected from strong drafts which can cause strong air current in the chamber.

2.2 Atomizers. The atomizer of atomizers used shall be of such design and construction as to produce a finely divided, wet dense fog. Atomizing nozzle shall be made of material which does not react with the salt solution.

2.3 Air supply. The compressed air entering the atomizers shall be free from all impurities such as oil and dirt. Means shall be provided to humidify and warm the compressed air as required to meet the operating conditions. The air pressure shall be suitable to produce a finely divided dense fog with the atomizer or atomizers used. To insure against clogging the atomizers by salt deposition, the air should have a relative humidity of 95 to 98 percent at the point of release from the nozzle. A satisfactory method is to pass the air in very fine bubbles through a tower containing heated water. The temperature of the water should be 95°F (35°C) and often higher. The permissible temperature increased with increasing volume of air and with decreasing heat insulation of the chamber and temperature of its surroundings. It should not exceed a value above which an excess of moisture is introduced into the chamber (for example, 110°F (43.3°C) at an air pressure of 12 pounds per square inch), or a value which makes it impossible to meet the requirement for operating temperature.

2.4 Salt solution. The salt-solution concentration shall be 5 percent by weight. The salt used shall be sodium chloride containing on the dry basis of more than 0.1 percent of sodium iodide, and not more than 0.5 percent of total impurities. The 5-percent solution shall be prepared by dissolving 5 ±1 parts by weight of salt in 95 parts by weight of distilled or other water. Distilled or other water used in the preparation of solutions shall contain nor more than 200 parts per million of total solids. The solution shall be kept free from solids by filtration using a filter similar to that shown on figure 1046-1, and located in the salt solution reservoir in a manner such as that illustrated on figure 1046-2. The solution shall be adjusted to and maintained at a specific gravity in accordance with figure 1046-3. The pH shall be maintained between 6.5 and 7.2 when measured at temperature between 93°F and 97°F (33.9°C and 36.1°C). Only dilute cp grade hydrochloric acid or sodium hydroxide shall be used to adjust the pH. The pH measurement shall be made electrometrically using a glass electrode with a saturated potassium-chloride bridge or by a colorimetric method such as bromothymol blue, provided the results are equivalent to those obtained with the electrometric method.

2.5 Filter. A filter fabricated of noncorrosive materials similar to that shown on figure 1046-1 shall be provided in the supply line and immersed in the reservoir in a manner such as shown on figure 1046-2.

2.6 Preparation of specimens. Specimens shall be given a minimum of handling, particularly on the significant surfaces, and shall be prepared for test immediately before exposure. Unless otherwise specified, uncoated metallic or metallic-coated specimens shall be thoroughly cleaned of oil, dirt, and grease as necessary until the surface is free from water break. The cleaning methods shall not include the use of corrosive solvents nor solvents which deposit wither corrosive or protective films, nor the use of abrasives other than a paste of pure magnesium oxide. Specimens having an organic coating shall not be solvent cleaned. Those portions of specimens which comes in contact with the support and, unless otherwise specified in the case of coated specimens or samples, cut edges and surfaces not required to be coated, shall be protected with a suitable coating of wax or similar substance impervious to moisture.

3. Procedure. The following exceptions shall apply:

a. At the conclusion of the test, the device will be dried for 24 hours at +40°C ±5°C before the examination. A device with illegible marking, evidence (when examined without magnification) of flaking or pitting of the finish or corrosion that will interfere with the application of the device shall be considered a failure.

b. Unless otherwise specified, salt solution shall be 20 percent by weight.

3.1 Location of specimens. Unless otherwise specified, flat specimens and, where practicable, other specimens shall be supported in such a position that the significant surface is approximately 15° from the vertical and parallel to the principal direction of horizontal flow of the fog through the chamber. Other specimens shall be positioned so as to insure most uniform exposure. Whenever practicable, the specimens shall be supported from the bottom or from the side. When specimens are suspended from the top, suspension shall be by means of glass or plastic hooks or wax string; if plastic hooks are used, they shall be fabricated of material which is nonreactive to the salt solution such as Lucite. The used of metal hooks is not permitted. Specimens shall be positioned so that they do not contact each other, so that they do not shield each other from the freely settling fog, and so that corrosion products and condensate from one specimen do not fall upon another.

3.2 Operating conditions.

3.2.1 Temperature. The test shall be conducted with a temperature in the exposure zone maintained at 95°F +2°F, -3°F (35°C +1.1°C, -1.7°C). Satisfactory methods for controlling the temperature accurately are by housing the apparatus in a properly controlled constant-temperature room, by thoroughly insulating the apparatus and preheating the air to the proper temperature prior to atomization, and by jacketing the apparatus and controlling the temperature of the water or of the air used. The use of immersion heaters for the purpose of maintaining the temperature within the chamber is prohibited.

3.2.2 Atomization. The conditions maintained in all parts of the exposure zone shall be such that a suitable receptacle placed at any point in the exposure zone will collect from 0.5 to 3.0 milliliters of solution per hour for each 80 square centimeters of horizontal collecting area (10 centimeters diameter) based on an average run of at least 16 hours. The 5-percent solution thus collected shall have a sodium-chloride content of from 4 to 6 percent (specific gravity) in accordance with figure 1046-3 when measured at a temperature between 93°F and 97°F (33.9°C and 36.1°C). At least two clean fog-collecting receptacles shall be used, one placed near any nozzle and one placed as far as possible from all nozzles. Receptacles shall be fastened so that they are no shielded by specimens and so that no drops of solution from specimens or other sources will be collected. The specific gravity and quantity of the solution collected shall be checked following each salt-spay test. Suitable atomization has been obtained in boxes having a volume of less than 12 cubic feet with the following conditions:

a. Nozzle pressure of from 12 to 18 pounds per square inch.

b. Orifices of from 0.02 to 0.03 inch in diameter.

c. Atomization of approximately 3 quarts of the salt solution per 10 cubic feet of box volume per 24 hours.

When using large-size boxes having a volume considerably in excess of 12 cubic feet, the above conditions may have to be modified in order to meet the requirements for operating conditions.

3.3 Length of test. The length of the salt-spray test shall be that indicated in one of the following test conditions, as specified:

Test condition		Length of test
A	- - - - - - - -	96 hours
B	- - - - - - - -	48 hours

Unless otherwise specified, the test shall be run continuously for the time indicated or until definite indication of failure is observed, with no interruption except for adjustment of the apparatus and inspection of the specimen.

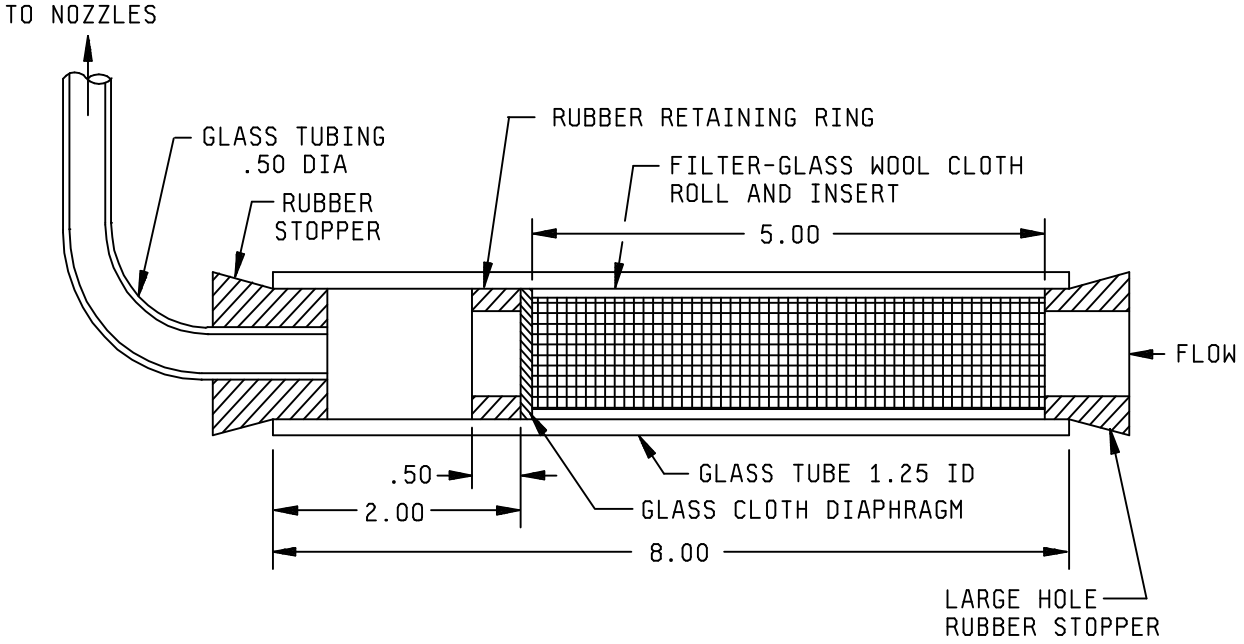
4. Measurements. At the completion of the exposure period, measurements shall be made as specified. To aid in examination, specimens shall be prepared in the following manner, unless otherwise specified: Salt deposits shall be removed by a gentle wash or dip in running water not warmer than 100°F (37.8°C) and a light brushing, using a soft-hair brush or plastic-bristle brush.

5. Summary. The following details are to be specified in the individual specification:

a. Special mounting and details, if applicable (see 3.1)

b. Test condition letter (see 3.3)

c. Measurements after exposure (see 4).



Inches	Millimeters
0.50	12.70
1.25	31.75
2.00	50.80
5.00	127.00
8.00	203.20

FIGURE 1046-1. Salt solution filter.

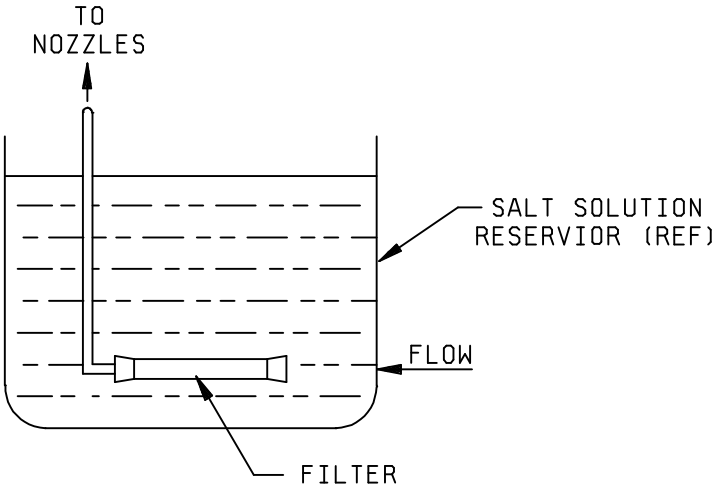


FIGURE 1046-2. Location of salt solution filter.

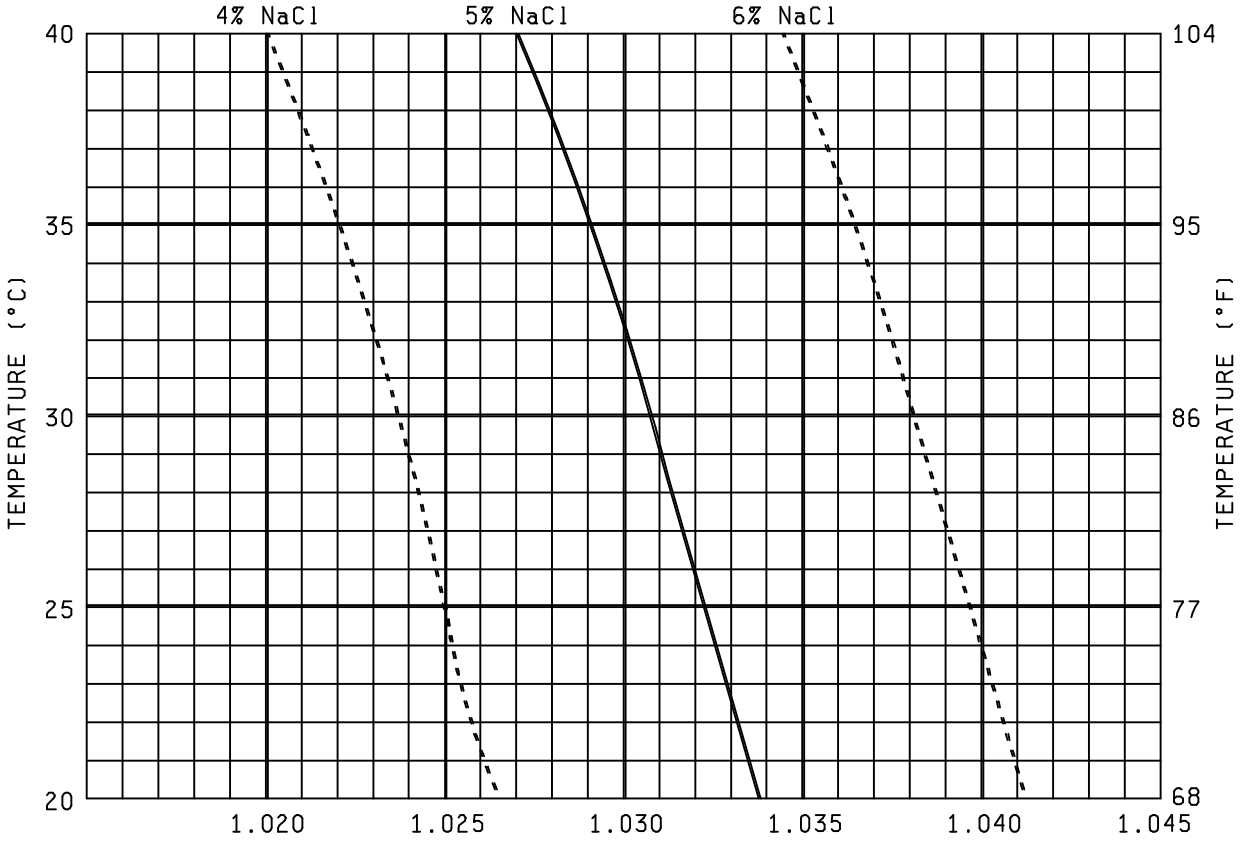


FIGURE 1046-3. Variations of specific gravity of salt (NaCl) solution with temperature.

METHOD 2069.1

PRE-CAP VISUAL, POWER MOSFET'S

1. Purpose. The purpose of this inspection is to verify the construction and quality of workmanship in the assembly process to the point of pre-cap inspection. These various inspections and tests are intended to verify compliance with the requirements of the applicable detail specification.

2. Apparatus. The apparatus for this inspection shall consist of the following:

a. Optical equipment capable of the specified magnification(s).

b. Adequate fixturing for handling the devices being inspected without causing damage.

c. Adequate covered storage and transportation containers to protect devices from mechanical damage and environmental contamination.

d. Any visual standards (e.g., drawings, photographs) necessary to enable the inspector to make objective decisions as to the acceptability of devices being inspected.

3. Procedure.

3.1 General. The devices shall be examined in a suitable sequence of observations with the specified magnification range to determine compliance with the requirements of this document and the applicable detail specification.

a. Sequence of inspection. The order in which criteria are presented is not a required order of inspection and may be varied at the discretion of the manufacturer.

b. Inspection control. Within the time interval between visual inspection and preparation for sealing, devices shall be stored in a controlled environment (an environment in which air-borne particles and relative humidity are controlled). The use of a positive pressure inert gas environment, such as dry nitrogen, shall satisfy the requirement of storing in a controlled environment. Unless a cleaning operation is performed prior to sealing, devices inspected in accordance with this specification shall be inspected in a class 100,000 environment in accordance with FED-STD-209. The maximum allowable relative humidity shall not exceed 65 percent. Devices shall be in clean covered containers when transferred through any uncontrolled environment.

c. Magnification. Low magnification inspection shall be performed with either a monocular, binocular or stereo microscope and the inspection performed with any appropriate angle, with the device under suitable illumination. High magnification may be used to verify a discrepancy which has first been noted at low magnification.

(1) High magnification inspection shall be performed within the range of 100X to 400X.

(2) Low magnification shall be performed within the range of 30X to 100X.

3.2 Bonding inspection (low magnification). This inspection and criteria shall be the required inspection for the bond type(s) and location(s) to which they are applicable when viewed from above (see figures 2069-1 and 2069-2). (Wire tail is not considered part of the bond when determining physical bond dimensions.) No device shall be acceptable which exhibits any of the following defects.

3.2.1 Gold ball bonds.

a. Gold ball bonds where the ball bond diameter is less than 2.0 times or greater than 5.0 times the bonding wire diameter.

b. Gold ball bonds where the wire exit is not completely within the periphery of the ball.

c. Gold ball bonds where the exiting wire is not within boundaries of the bonding pad.

d. Any visible intermetallic formation at the periphery of any gold ball bond.

3.2.2 Wedge bonds.

a. Ultrasonic/thermasonic wedge bonds that are less than 1.2 times or greater than 3.0 times the wire diameter in width, or are less than 1.5 times or greater than 3.0 times the wire diameter in length, before cutoff, as viewed from above.

b. Thermocompression wedge bonds that are less than 1.2 times or greater than 3.0 times the wire diameter in width or are less than 1.5 times or greater than 3.0 times the wire diameter in length.

3.2.3 Tailless bonds (crescent).

a. Tailless bonds that are less than 1.2 times or greater than 5.0 times the wire diameter in width, or are less than 0.5 times or greater than 3.0 times the wire diameter in length.

b. Tailless bonds where the bond impression does not cover the entire width of the wire.

3.2.4 General (gold ball, wedge and tailless). As viewed from above, no device shall be acceptable which exhibits any of the following defects:

a. Bonds on the die where less than 75 percent of the bond is within the unglassivated bonding pad area (except where due to geometry, the bonding pad is smaller than the bond, the criteria shall be 50 percent).

b. Wire bond tails that extend over and make contact with any metallization not covered by glassivation and not connected to the wire.

c. Wire bond tails that exceed two wire diameters in length at the die bonding pad or four wire diameters in length at the package or post.

d. Bonds on the package post that are not bonded entirely on the flat surface of the post top.

e. A bond on top of another bond, bond wire tail, or residual segment of lead wire. An ultrasonic wedge bond alongside a previous bond where the observable width of the first bond is reduced less than .25 mil is considered acceptable.

f. Bonds placed so that the separation between bond and adjacent unglassivated die metallization not connected to it, is less than 1.0 mil.

g. Rebonding.

h. Gold bonds where less than 50 percent of the bond is located within an area that is free of eutectic melt.

3.2.5 Internal lead wires. This inspection and criteria shall be required inspection for the location(s) to which they are applicable when viewed from above. No device shall be acceptable that exhibits any of the following defects:

a. Any wire that comes closer than one wire diameter to unglassivated operating metallization, another wire (common wires excluded), package post, unpassivated die area of opposite polarity, or any portion of the package of opposite polarity including the plane of the lid to be attached (except by design, but in no case should the separation be less than 0.25 mil). (Within a 5.0 mil spherical radial distance from the perimeter of the bond on the die surface, the separation shall be greater than 1.0 mil.)

b. Nicks, tears, bends, cuts, crimps, scoring, or neckdown in any wire that reduces the wire diameter by more than 25 percent, except in bond deformation area.

c. Missing or extra lead wires.

d. Bond lifting or tearing at interface of pad and wire.

e. Any wire which runs from die bonding pad to package post and has no arc or stress relief.

f. Wires which cross other wires, except common connectors, except by design, in which case the clearance shall be 1.0 mil minimum.

g. Wire(s) not in accordance with bonding diagram (unless allowed in design documentation, for tuning purposes).

h. Kinked wires (an unintended sharp bend) with an interior angle of less than 90 degrees or twisted wires to an extent that stress marks appear.

i. Wire (ball bonded devices) not within 10° of the perpendicular to the surface of the chip for a distance of greater than 0.5 mil before bending toward the package post or other termination point.

3.3 Package conditions (low magnification). No device shall be acceptable which exhibits any of the following defects.

3.3.1 Foreign material on die surface. All foreign material or particles may be blown off with a nominal gas blow (approximately 20 psig) or removed with a soft camel hair brush. The device shall then be inspected for the following criteria:

a. Loosely attached conductive particles (conductive particles which are attached by less than one-half of their largest dimension) that are large enough to bridge the narrowest unglassivated active metal spacing (silicon chips or any opaque material shall be included as conductive particles).

b. Liquid droplets, chemical stains, or photoresist on the die surface that bridge any combination of unglassivated metallization or bare silicon areas, except for unused cells.

c. Ink on the surface of the die that covers more than 25 percent of a bonding pad area (or interferes with bonding) or that bridges any combination of unglassivated metallization or bare silicon areas, except for unused cells.

3.3.2 Die mounting.

a. Die to header mounting material which is not visible around at least three sides or 75 percent of the die perimeter. Wetting criteria is not required if the devices pass an approved die attached evaluation test.

b. Any balling of the die mounting material which does not exhibit a fillet when viewed from above.

c. Any flaking of the die mounting material.

d. Any die mounting material which extends onto the die surface or extends vertically above the top surface of the die and interferes with bonding.

3.3.3 Die orientation.

a. A die which is not oriented or located in accordance with the applicable assembly drawing of the device.

b. Die is visibly tipped or tilted (more than 10°) with respect to the die attach surface.

3.3.4 Internal package defects (low magnification inspection) (applicable to headers, bases, caps, and lids). As an alternative to 100 percent visual inspection of lids and caps in accordance with the criteria of 3.3.1a, the lids or caps may be subjected to a suitable cleaning process and quality verification procedure approved by the qualifying activity, provided the lids or caps are subsequently held in a controlled environment until capping or preparation for seal.

a. Any header or post plating which is blistered, flaked, cracked, or any combination thereof.

b. Any conductive particle which is attached by less than one-half of the longest dimension.

c. A bubble or a series of interconnecting bubbles in the glass surrounding the pins which are more than one-half the distance between the pin and body or pin-to-pin.

d. Header posts which are severely bent.

e. Any glass, die, or other material greater than one mil in its major dimension which adheres to the flange or side of the header and would impair sealing.

f. Any stain, varnish, or header discoloration which appears to extend under a die bond or wire bond.

g. For isolated stud packages:

(1) Any defect or abnormality causing the designed isolating paths between the metal island to be reduced to less than 50 percent of the design separation.

(2) A crack or chip-out in the substrate.

3.3.5 Carrier defects ((e.g., BeO, alumina) substrate).

a. Any chip-out in the carrier material.

b. Carrier metallization which is smeared or is obviously not uniform in metallization design pattern to the extent that there is less than 50 percent of the original design separation, or 0.5 mil whichever is less, between operating pads, paths, lid mounting metallization, edges, or any combination thereof.

c. Any crack in the BeO or operating metallization that would affect hermetic seal or die mounting metallization. (Tooling marks or cold form interface lines are not cracks and are not cause for rejection.)

d. Any metallization lifting, peeling, or blistering (on the carrier surface).

e. Any attached conductive foreign material which bridges any combination of metallization paths, leads, or active circuit elements.

f. A scratch or void in the metallization which exposes the substrate anywhere along its length and leaves less than 75 percent of the original metal width undisturbed.

NOTE: Occasionally package metallization is intentionally burnished or scratched, in areas which require wire bond attachment, to improve surface bondability; such conditions are not cause for rejection. Burnished or scratched areas must satisfy the criteria of 3.3.4b.

g. Excessive scratches in carrier metallization due to abuse in handling or processing.

h. Any staple, bridge, or clip with solder joint which exhibits less than 50 percent wetting around the section that is attached to the package.

i. Any header post(s) which are not perpendicular within 10° of the horizontal plane of the header.

j. Any lead attach eutectic or solder which extends across greater than 50 percent of the design separation gap between metallization pads.

3.3.6 Presence of extraneous matter. Extraneous matter (foreign particles) shall include, but not be limited to:

a. Any foreign particle, loose or attached, greater than .003 inch (0.08 mm) or of any lesser size which is sufficient to bridge nonconnected conducting elements of the device.

b. Any wire tail extending beyond its normal end by more than two diameters at the semiconductor die pad or by more than four wire diameters at the package post (see figure 2069-3).

c. Any burr on a post (header lead) greater than .003 inch (0.08 mm) in its major dimension or of such configuration that it may break away.

d. Excessive semiconductor die bonding material buildup. A semiconductor die shall be mounted and bonded so that it is not tilted more than 10° from mounting surface. The bonding agent that accumulates around the perimeter of the semiconductor die and touches the side of the semiconductor die shall not accumulate to a thickness greater than that of the semiconductor die (see figures 2069-4 and 2069-5). Where the bonding agent is built up but is not touching the semiconductor die, the build up shall not be greater than twice the thickness of the semiconductor die. There shall be no excess semiconductor die bonding material in contact with the active surface of the semiconductor die or any lead or post, or separated from the main bonding material area (see figure 2069-6).

e. Flaking on the header or posts or anywhere inside the case.

f. Extraneous ball bonds anywhere inside case, except for attached bond residue when rebonding is allowed.

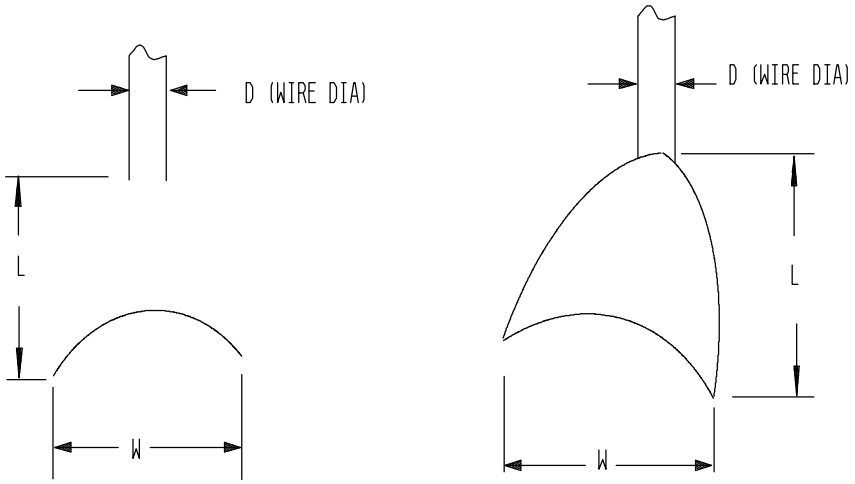
4. Summary. The following details shall be specified in the applicable detail specification:

a. Exceptions or additions to the inspection method.

b. Where applicable, any conflicts with approved circuit design topology or construction.

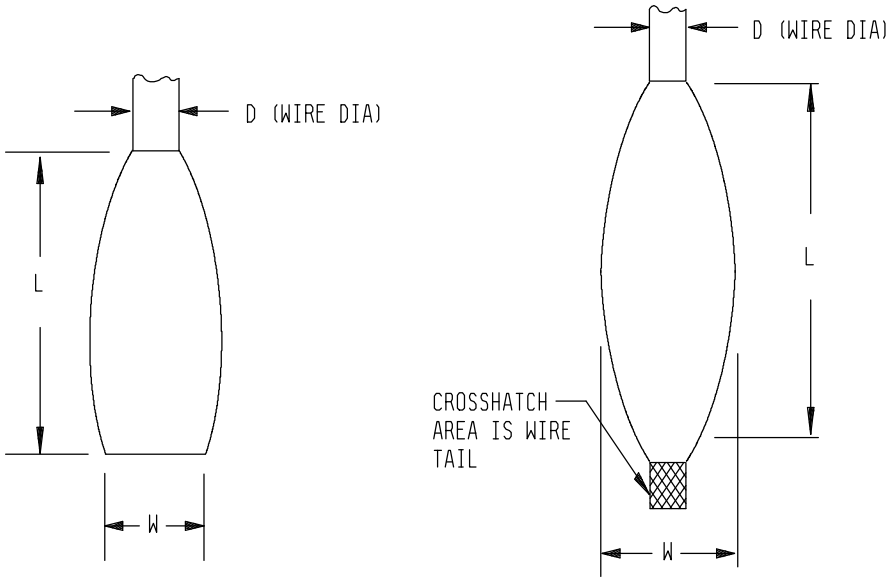
c. Where applicable; gauges, drawings, and photographs that are to be used as standards for operator comparison.

d. When applicable, specific magnification.



A. Tailless or crescent.

NOTES:
1. 1.2 D ≤ W ≤ 5.0 D (width).
2. 0.5 D ≤ L ≤ 3.0 D (length).



B. Wedge.

Ultrasonic

NOTES:
1. 1.0 D ≤ W ≤ 3.0 D (width)
2. 1.5 D ≤ L ≤ 5.0 D (length)

Thermocompression

NOTES:
1. 1.2 D ≤ W ≤ 3.0 D (width)
2. 1.5 D ≤ L ≤ 5.0 D (length)

FIGURE 2069-1. Bond dimensions.

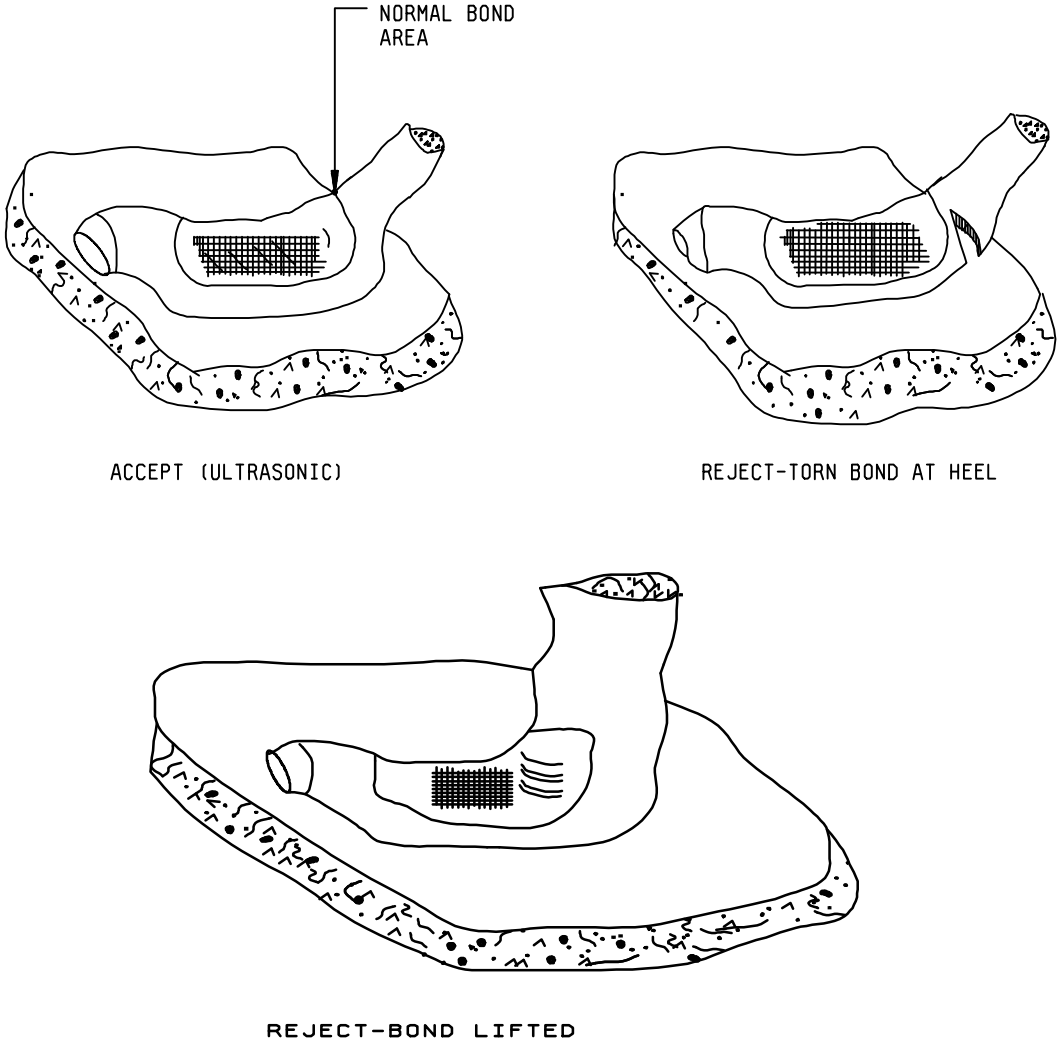
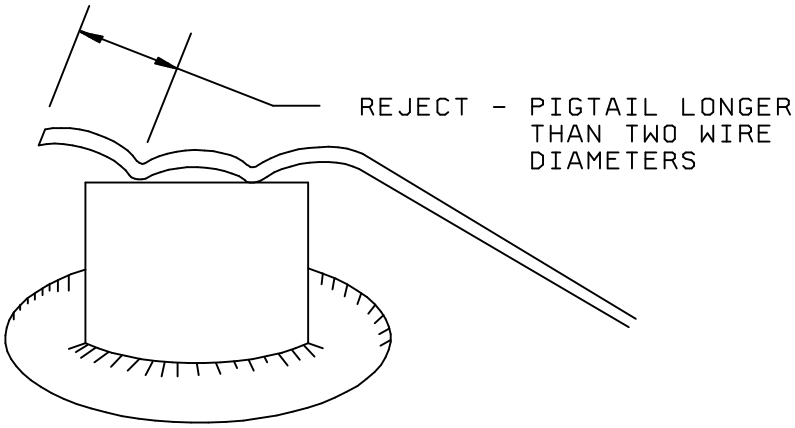
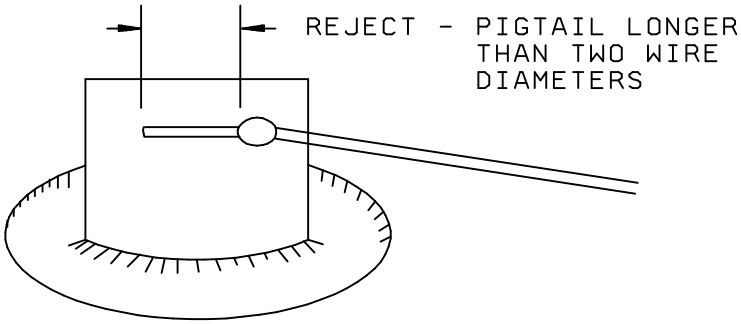


FIGURE 2069-2. Lifted/torn bonds.





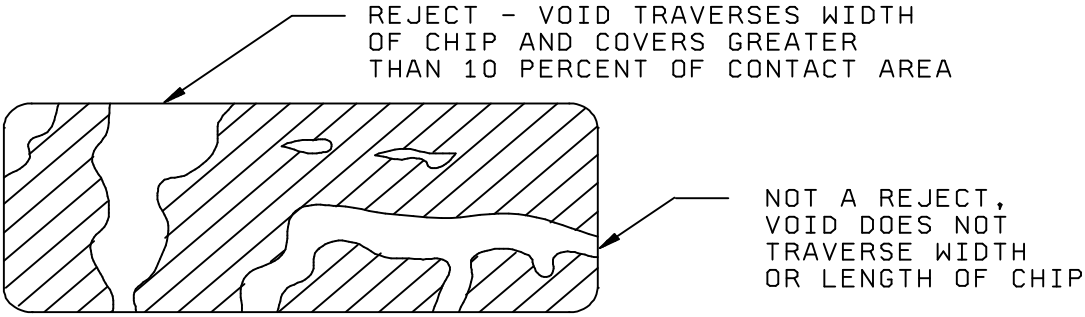


FIGURE 2069-3. Acceptable and unacceptable voids and excessive pigtails.

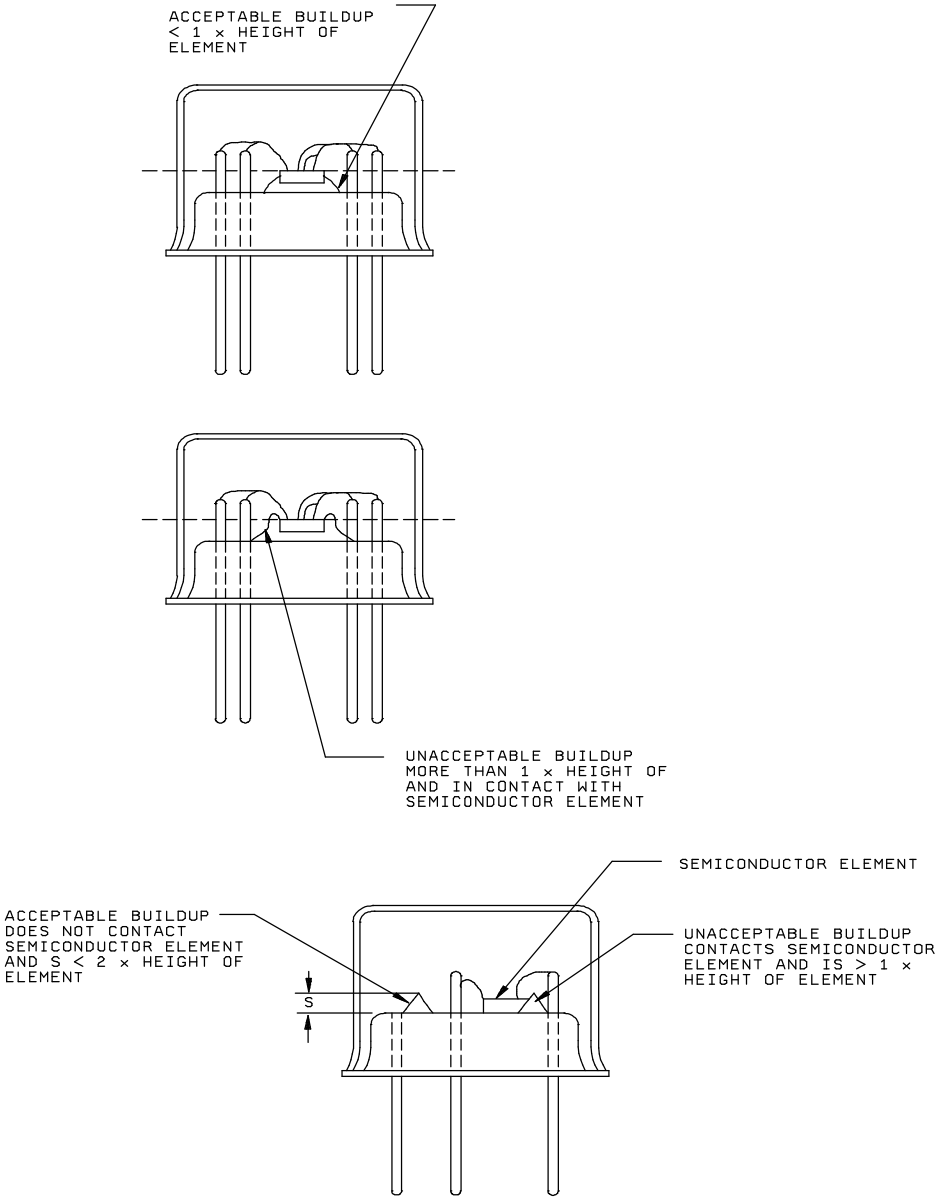


FIGURE 2069-4. Acceptable and unacceptable bonding material build-up.

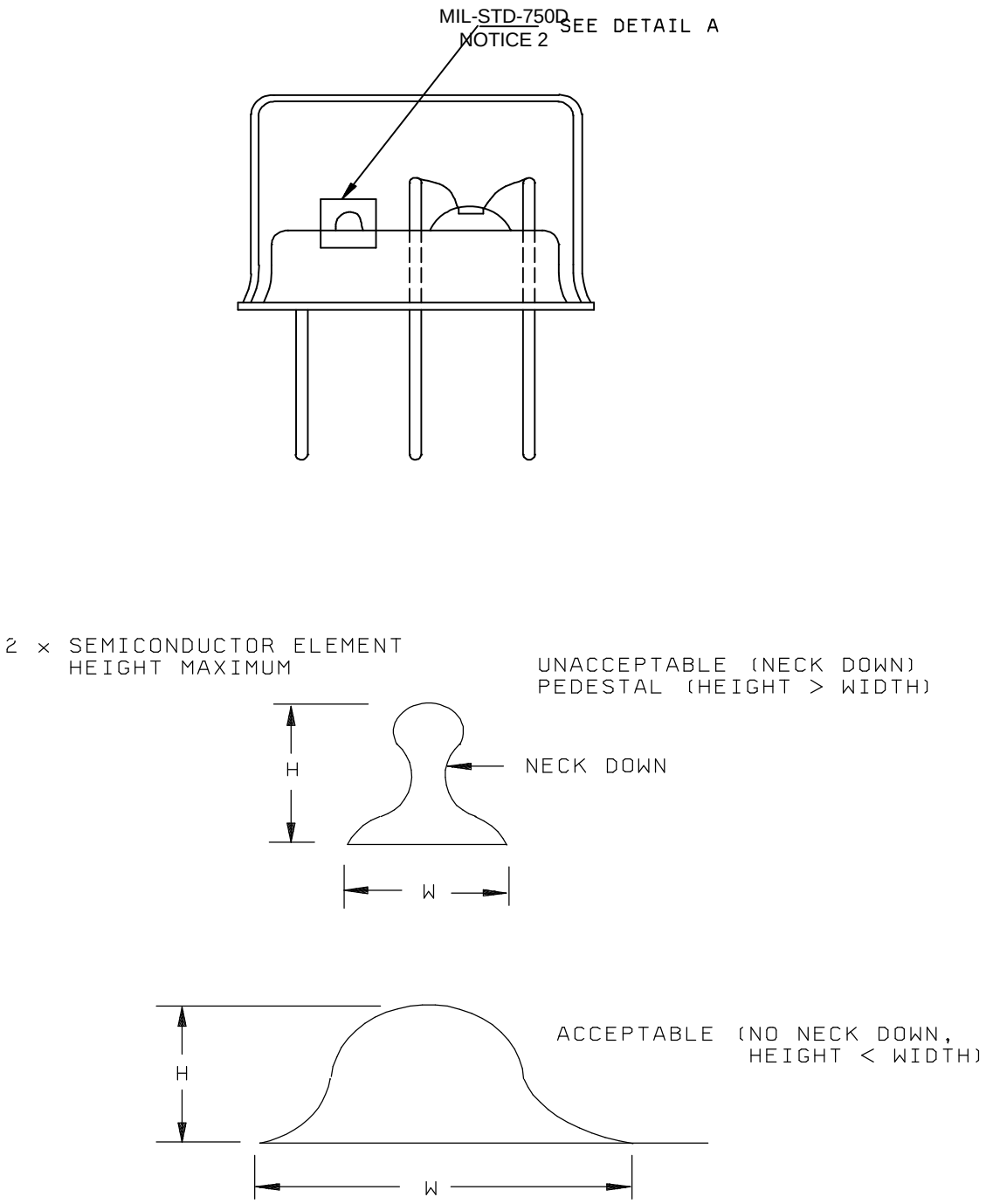
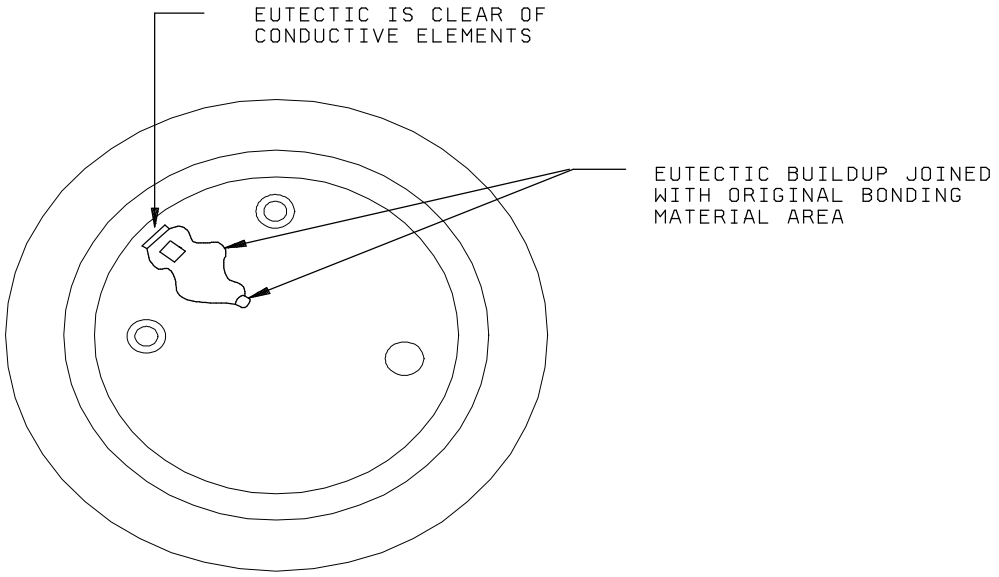
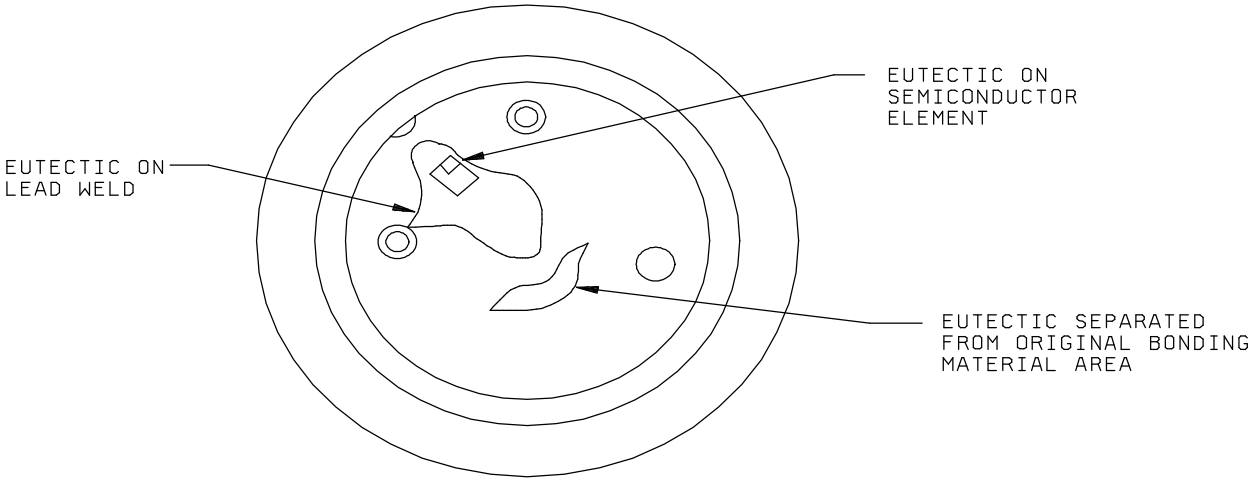


FIGURE 2069-5. Extraneous bonding material build-up.



ACCEPTABLE



UNACCEPTABLE

FIGURE 2069-6. Acceptable and unacceptable excess material.

METHOD 2072.6

INTERNAL VISUAL TRANSISTOR (PRE-CAP) INSPECTION

1. Purpose. The purpose of this inspection is to verify the construction and workmanship of bipolar transistors, field effect transistors (FET), discrete monolithic, multichip, and multijunction devices excluding microwave and selected RF devices. This test will be performed prior to capping or encapsulation to detect those devices with internal defects that could lead to failures in normal application and verify compliance with the requirements of the applicable detail specification.

2. Apparatus. The apparatus for this inspection shall consist of the following:

a. Optical equipment capable of the specified magnifications.

b. Light sources of sufficient intensity to adequately illuminate the devices being inspected.

c. Adequate fixturing for handling the devices being inspected without causing damage.

d. Adequate covered storage and transportation containers to protect devices from mechanical damage and environmental contamination.

e. Any visual standards (drawings and photographs) necessary to enable the inspector to make objective decisions as to the acceptability of the devices being examined.

3. Definitions.

3.1 Glassivation. The top layer of transparent insulating material that covers the active circuit area metallization, but excluding bonding pads.

3.2 Passivation. Silicon oxide, nitride, or other insulating material that is grown or deposited directly on the die prior to the deposition of any metal.

4. Procedure.

4.1 General. The device shall be examined in a suitable sequence of observations within the specified magnification range to determine compliance with the requirements of the applicable detail specification and the criteria of the specified test condition. If a specified visual inspection requirement is in conflict with the topology or construction of a specific device design, alternate inspection criteria may be included in the detail specification. Any alternate inspection criteria contained in the detail specification shall take precedence over the criteria of this test method. Any criteria of this test method intended for a specific device process or technology has been indicated. Where applicable, unused cells shall not be subjected to internal visual criteria.

a. Sequence of inspection. The order in which criteria are presented is not a required order of examination and may be varied at the discretion of the manufacturer. Visual criteria specified in 4.1.1, 4.1.2, 4.1.3, and 4.1.7, may be examined prior to die attachment with reexamination at low or high magnification after die attachment for these criteria. Visual criteria specified in 4.1.6.2 and 4.1.6.3 may be examined prior to lead wire bonding without reexamination after bonding.

b. Inspection control. Within the time interval between visual inspection and preparation for sealing, devices shall be stored in a controlled environment (one which controls airborne particle count and relative humidity). The use of an inert gas environment, such as dry nitrogen shall satisfy the requirements for storing in a controlled environment. Devices examined in accordance with this test method shall be inspected and stored in a class 100,000 environment, in accordance with FED-STD-209, except that the maximum allowable relative humidity shall not exceed 65 percent.

If devices are subjected to a high temperature bake (>+100°C) immediately prior to sealing, the humidity control is not required. Unless a cleaning operation is performed prior to sealing, devices shall be in covered containers when transferred from one controlled environment to another.

c. Magnification. High magnification inspection shall be performed perpendicular to the die surface with normal incident illumination. Low magnification inspection shall be performed with either a monocular, binocular, or stereo microscope, and the inspection performed within any appropriate angle, with the device under suitable illumination. The inspection criteria of 4.1.4 and 4.1.6.1 may be examined at "high magnification" at the manufacturer's option. High power magnification may be used to verify a discrepancy noted at a low power.

TABLE 2072.1. Die magnification requirements.

Chip size 1/	High magnification	Low magnification
30 mils or less	100X to 200X	30X to 50X
31 to 61 mils	75X to 150X	30X to 50X
61 to 150 mils	35X to 120X	10X to 30X
Greater than 150 mils	25X to 75X	10X to 30X

1/ Length of shortest dimension.

d. Reinspection. Unless a specific magnification is required by the detail specification, when inspection for product acceptance or quality verification of the visual requirements herein is conducted subsequent to the manufacturer's successful inspection, the additional inspection may be performed at any magnification specified herein. If sampling is used rather than 100 percent reinspection, reevaluation of lot quality in accordance with the "Reevaluation of lot quality" of MIL-S-19500 shall be used.

e. Exclusions. If conditional exclusions have been allowed, specific instruction as to the location and conditions for which the exclusion can be applied shall be documented in the assembly inspection drawing.

4.1.1 Die metallization defects (high magnification). A die which exhibits any of the following defects shall be rejected.

4.1.1.1 Metallization, scratches, and voids exposing underlying material (see figure 2072-1).

a. A scratch or void that severs the innermost metallized guard ring.

b. Any die containing a void in the metallization at the bonding pad covering more than 25 percent of the pad area.

c. For devices with nonexpanded contacts and all power devices. Any scratch or void which isolates more than 25 percent of the total metallization of an active region from the bonding pad.

d. For all devices with expanded contacts. A scratch or void, whether or not underlying material is exposed, which leaves less than 50 percent undisturbed metal width in the metal connecting the pad and contact regions.

e. For expanded contacts with more than 10 contact regions. A scratch or void extending across more than 50 percent of the first half of any contact region (beginning at the bonding area) in more than 10 percent of the contact regions.

f. For expanded contacts with less than 10 contact regions. A scratch or void in the contact area which isolates more than 10 percent of the metallized area from the bonding pad.

4.1.1.2 Metallization corrosion. Any metallization which shows evidence of corrosion.

4.1.1.3 Metallization adherence. Any metallization which has lifted, peeled, or blistered.

4.1.1.4 Metallization probing. Criteria contained in 4.1.1.1 shall apply as limitations on probing damage.

4.1.1.5 Metallization bridging. Metallization bridging between two normally unconnected metallization paths which reduces the separation, such that a line of oxide is not visible (no less than 0.1 mil) when viewed at the prescribed high magnification.

4.1.1.6 Metallization alignment.

a. Except by design, contact window that has less than 50 percent of its area covered by continuous metallization.

b. A metallization path not intended to cover a contact window which is separated from the window by less than 0.1 mil.

c. Except by design, any misalignment to the extent that continuous passivation color cannot be seen (i.e., metallization crossing passivation).

4.1.2 Passivation and diffusion faults (high magnification). A device which exhibits any of the following defects (see figure 2072-2) shall be rejected:

a. Any diffusion fault that allows bridging between any two diffused areas, any two metallization strips, or any such combination not intended by design.

b. Any passivation fault including pinholes not covered by glassivation that exposes semiconductor material and allows bridging between any two diffused areas, any two metallization strips, or any such combination not intended by design.

c. Unless intended by design, a diffusion area which is discontinuous.

d. Except by design, an absence of passivation visible at the edge and continuing under the metallization causing an apparent short between the metal and the underlying material (closely spaced double or triple lines on the edges of the defect indicate that it may have sufficient depth to penetrate down to the silicon).

e. Except by design, any active junction not covered by passivation or glassivation.

f. Unless by design, a contact window in a diffused area which extends across a junction.

4.1.3 Scribing and die defects (high magnification). A device which exhibits any of the following defects (see figure 2072-3) shall be rejected:

a. Unless by design, less than 0.1 mil passivation visible between active metallization or bond pad periphery and the edge of the die.

b. Any chip-out or crack in the active area.

c. Except by design, die having attached portions of the active area of another die and which exceeds 10 percent of the area of the second die.

d. Any crack which exceeds 2.0 mils in length inside the scribe grid or scribe line that points toward active metallization or active area and extends into the oxide area.

e. Any chip-out that extends to within 1 mil of a junction.

f. Any crack or chip-out that extends under any active metallization area.

g. Any chip-out which extends completely through the guard ring.

4.1.4 Bond inspection (low magnification). This inspection and criteria shall be the required inspection for the bond type(s) and location(s) to which they are applicable when viewed from above (see figures 2072-4 and 2072-5). Wire tail is not considered part of the bond when determining physical bond dimensions. A device which exhibits any of the following defects shall be rejected.

4.1.4.1 Gold ball bonds.

a. Gold ball bonds on the die or package post where the ball bond diameter is less than 2.0 times or greater than 5.0 times the wire diameter.

b. Gold ball bonds where the wire exit is not completely within the periphery of the ball.

c. Gold ball bonds where the existing wire is not within the boundaries of the bonding pad.

d. Any visible intermetallic formation at the periphery of any gold ball bond.

4.1.4.2 Wedge bonds.

a. Ultrasonic wedge bonds on the die or package post that are less than 1.2 times or greater than 3.0 times the wire diameter in width, or are less than 1.5 times or greater than 5.0 times the wire diameter in length.

b. Thermocompression wedge bonds on the die or package post that are less than 1.2 times or greater than 3.0 times the wire diameter in width or are less than 1.5 or greater than 5.0 times the wire diameter in length.

4.1.4.3 Tailless bonds (crescent).

a. Tailless bonds on the die or package post that are less than 1.2 times or greater than 5.0 times the wire diameter in width, or are less than 0.5 times or greater than 3.0 times the wire diameter in length.

b. Tailless bonds where the bond impression does not cover the entire width of the wire.

4.1.4.4 General (gold ball, wedge, and tailless). As viewed from above, a device which exhibits any of the following defects shall be rejected:

a. Bonds on the die where less than 75 percent of the bond is within the unglassivated bonding pad area (except where due to geometry, the bonding pad is smaller than the bond, the criteria shall be 50 percent).

b. Wire bond tails that extend over and make contact with any metallization not covered by glassivation and not connected to the wire.

c. Wire bond tails that exceed two wire diameters in length at the bonding pad or four wire diameters in length at the package post.

d. Bonds on the package post that are not bonded entirely on the flat surface of the post top.

e. A bond on top of another bond.

f. Bonds placed so that the separation between bonds and adjacent unglassivated die metallization is less than 1.0 mil.

g. Bonds placed so that the separation between bonds and adjacent glassivated die metallization is less than 0.25 mil.

h. Bonds placed so that the separation between adjacent bonds is less than 0.25 mil. This criteria does not apply to designs which employ multiple bond wires in place of a single wire.

i. Bonds located where any of the bond is placed on an area containing die preform mounting material.

j. Repair on conductors by bridging or addition of bonding wire or ribbon.

k. For aluminum wires over 2.0 mils diameter, the bond width shall not be less than 1.0 times the wire diameter.

4.1.5 Internal lead wires (low magnification). This inspection and criteria shall be required inspection for the location(s) to which they are applicable when viewed from above. A device which exhibits any of the following defects shall be rejected:

a. Any wire that comes closer than two wire diameters or 5 mils, whichever is less, to unglassivated operating metallization, another wire (common wires and pigtails excluded) package post, unpassivated die area, or any portion of the package, including the plane of the lid to be attached. (Within a 5.0 mil spherical radial distance from the perimeter of the bond on the die surface, the separation can be 1.0 mil.)

b. Nicks, tears, bonds, cuts, crimps, scoring, or neckdown in any wire that reduces the wire diameter by more than 25 percent.

c. Missing or extra lead wires.

d. Bond lifting or tearing at interface of pad and wire (see figure 2072-5).

e. Any wire which runs from die bonding pad to package post and has no arc or stress relief.

f. Except in common connectors, wires which cross other wires.

g. Wire(s) not in accordance with bonding diagram.

h. Wire is kinked (unintended sharp bend) with an interior angle of less than 90° or twisted to an extent that stress marks appear.

i. Wire (ball bonded devices) not within 10° of the perpendicular to the surface of the chip for a distance of greater than 0.5 mil before bending toward the package post or other termination point.

j. Excessive lead burn at lead post weld.

k. Pigtail longer than 50 percent of post diameter.

l. A bow or loop between double bonds at post greater than four times wire diameter.

m. Excessive loops, bows, or sags in any wire such that it could short to another wire, to another pad, to another package post, to the die or touch any portion of the package.

n. When clips are used, solder fillets shall encompass at least 50 percent of the clip-to-die and post-to-clip periphery. There shall be no deformation or plating defects on the clip.

4.1.6 Package conditions (magnification as indicated). A device which exhibits any of the following defects shall be rejected.

4.1.6.1 Conductive foreign material on die surface. All foreign material or particles may be blown off with a nominal gas blow (approximately 20 psi (138 kPa)) or removed with a soft camel hair brush. The device shall then be inspected for the following criteria (low magnification):

a. Loosely attached foreign particles (conductive particles which are attached by less than one-half of their largest dimension) which are present on the surface of the die that are large enough to bridge the narrowest unglassivated active metal spacing (silicon chips shall be included as conductive particles).

b. Embedded foreign particles on the die that bridge two or more metallization paths or semiconductor junctions, or any combination of metallization or junction.

c. Liquid droplets, chemical stains, or photoresist on the die surface that bridge any combinations of unglassivated metal or bare silicon areas.

d. Except for unused cells, ink on the surface of the die that covers more than 25 percent of a bonding pad area or that bridges any combination of unglassivated metallization or bare silicon areas.

4.1.6.2 Die mounting (low magnification).

a. Die mounting material buildup that extends onto the top surface of the die or extends vertically above the top surface of the die and interferes with bonding.

b. Die to header mounting material which is not visible around at least three complete sides or 75 percent of the die perimeter. Wetting criteria is not required if the devices pass an approved electrical die attach evaluation test.

c. Any flaking of the die mounting material.

d. Any balling of the die mounting material which does not exhibit a fillet when viewed from above.

4.1.6.3 Die orientation.

a. Die is not located or orientated in accordance with the applicable assembly drawing of the device.

b. Die is visibly tipped or tilted (more than 10°) with respect to the die attach surface.

4.1.6.4 Internal package defects (low magnification inspection) (applicable to headers, bases, caps, and lids). As an alternative to 100 percent visual inspection of lids and caps in accordance with the criteria of 4.1.6.1a, the lids or caps may be subjected to a suitable cleaning process and quality verification procedure approved by the qualifying activity, provided the lids or caps are subsequently held in a controlled environment until capping or preparation for seal.

a. Any header or post plating which is blistered, flaked, cracked, or any combination thereof.

b. Any conductive particle which is attached by less than one-half of the longest dimension.

c. A bubble or a series of interconnecting bubbles in the glass surrounding the pins which are more than one-half the distance between the pin and body or pin-to-pin.

d. Header posts which are severely bent.

e. Any glass, die, or other material greater than 1.0 mil in its major dimension which adheres to the flange or side of the header and would impair sealing.

f. Any stain, varnish, or header discoloration which appears to extend under a die bond or wire bond.

g. For isolated stud packages:

(1) Any defect or abnormality causing the designed isolating paths between the metal island to be reduced to less than 50 percent of the design separation.

(2) A crack or chip-out in the substrate.

4.1.6.5 Presence of extraneous matter. Extraneous matter (foreign particles) shall include, but not be limited to:

a. Any foreign particle, loose or attached, greater than .003 inch (0.08 mm) or of any lesser size which is sufficient to bridge nonconnected conducting elements of the device.

b. Any wire tail extending beyond its normal end by more than two diameters at the semiconductor die pad or by more than four wire diameters at the package post (see figure 2072-6).

c. Any burr on a post (header lead) greater than .003 inch (0.08 mm) in its major dimension or of such configuration that it may break away.

d. Excessive semiconductor die bonding material buildup. A semiconductor die shall be mounted and bonded so that it is not tilted more than 10° from mounting surface. The bonding agent that accumulates around the perimeter of the semiconductor die and touches the side of the semiconductor die shall not accumulate to a thickness greater than that of the semiconductor die (see figures 2072-7 and 2072-8). Where the bonding agent is built up but is not touching the semiconductor die, the build up shall not be greater than twice the thickness of the semiconductor die. There shall be no excess semiconductor die bonding material in contact with the active surface of the semiconductor die or any lead or post, or separated from the main bonding material area (see figure 2072-9).

e. Flaking on the header or posts or anywhere inside the case.

f. Extraneous ball bonds anywhere inside case, except for attached bond residue when rebonding is allowed.

4.1.7 Glassivation and silicon nitride defects (high magnification). No device shall be acceptable that exhibits any of the following defects:

a. Glass crazing that prohibits the detection of visual criteria contained herein.

b. Any glassivation which has delaminated. (Lifting or peeling of the glassivation may be excluded from the criteria above, when it does not extend more than 1.0 mil distance from the designed periphery of the glassivation, provided that the only exposure of metal is adjacent to bond pads or of metallization leading from those pads.)

c. Except by design, two or more adjacent active metallization paths which are not covered by glassivation.

d. Unglassivated areas at the edge of bonding pad which expose silicon.

e. Glassivation which covers more than 25 percent of the design bonding pad area.

4.2 Post organic protective coating visual inspection. If devices are to be coated with an organic protective coating the devices shall be visually examined in accordance with the criteria specified in 4.1 prior to application of the coating. After the application and cure of the organic protective coating the devices shall be visually examined under a minimum of 10X magnification. Devices which exhibit any of the following defects shall be rejected:

a. Except by design, any unglassivated or unpassivated areas or insulating substrate which has incomplete coverage.

b. Open bubbles, cracks or voids in the organic protective coating.

c. A bubble or a chain of bubbles which covers two adjacent metallized surfaces.

d. Organic protective coating which has flaked or peeled.

e. Organic protective coating which is tacky.

f. Conductive particles which are embedded in the coating and are large enough to bridge the narrowest unglassivated active metal spacing (silicon chips shall be included as conductive particles).

g. A web of varnish (organic protective coating) that connects the wire with the header.

5. Summary. The following conditions shall be specified in the applicable detail specification:

a. Test conditions, exceptions, or additions to the test method.

b. Where applicable, any conflicts with approved circuit design topology or construction.

c. Where applicable, gauges, drawings, and photographs that are to be used as standards for operator comparison.

d. When applicable, specific magnification.

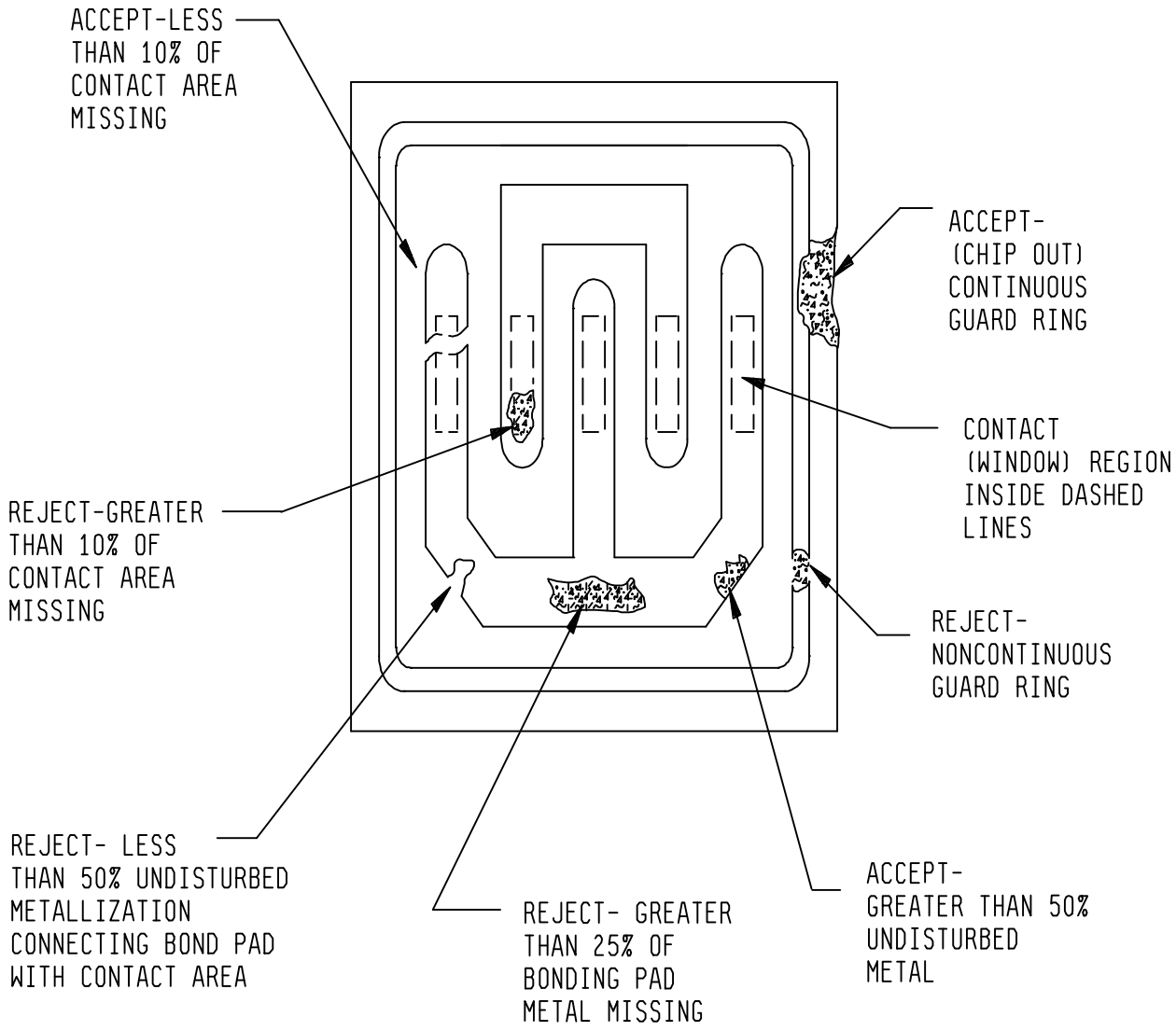
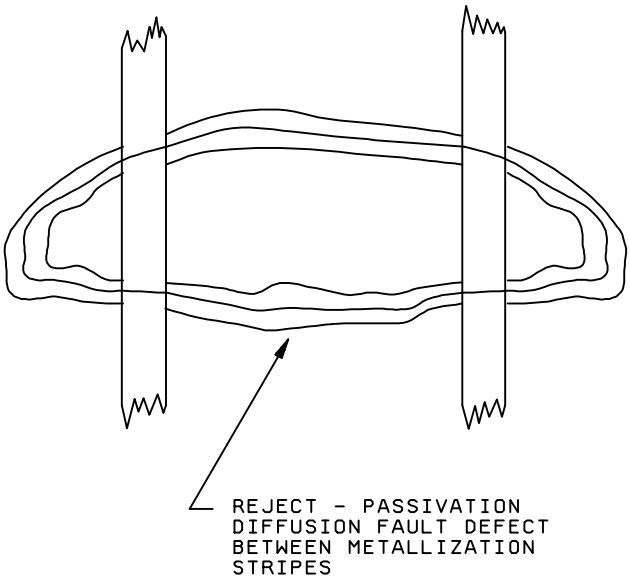


FIGURE 2072-1. Metallization scratches and voids (expanded contact).



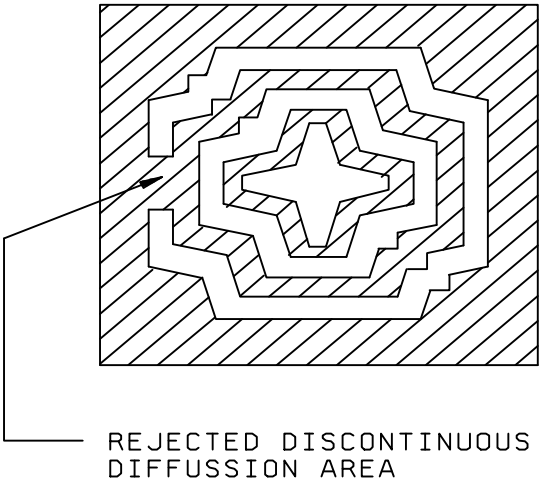
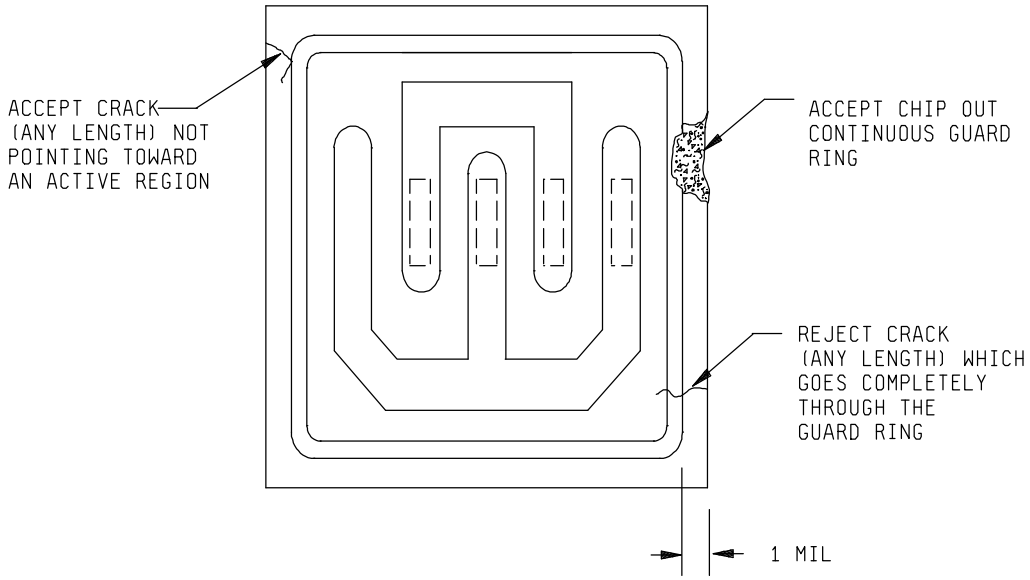
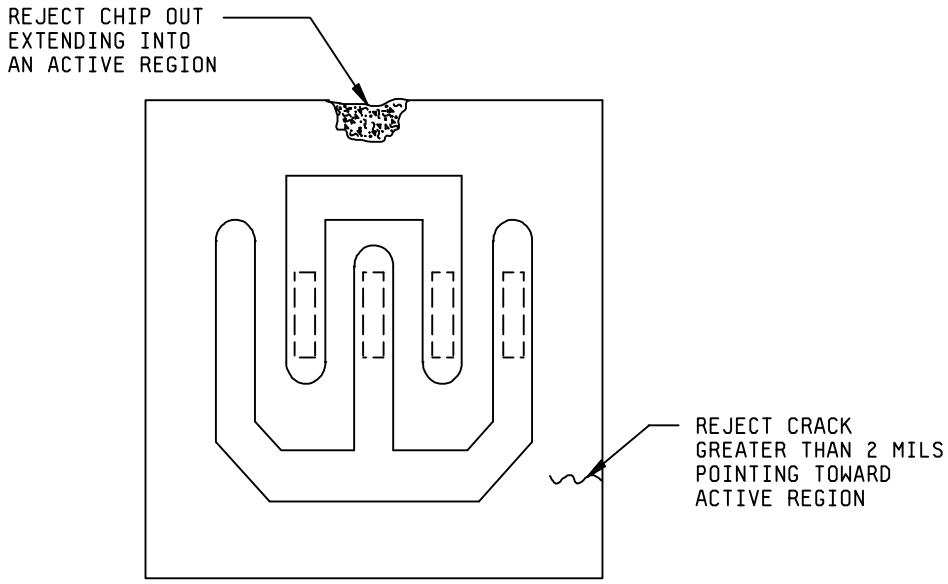


FIGURE 2072-2. Passivation and diffusion faults.

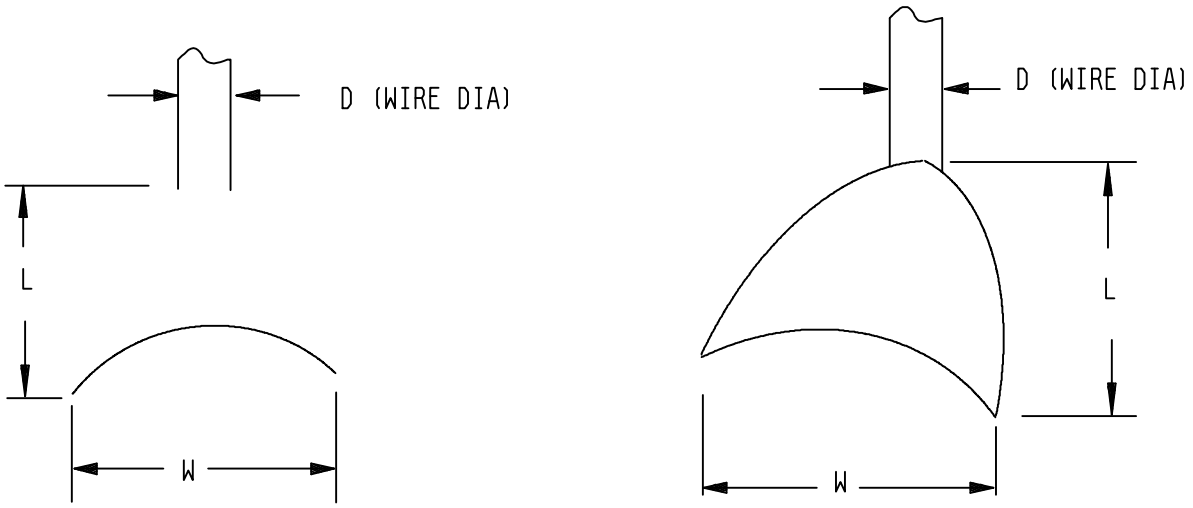


A. Die with guard ring.



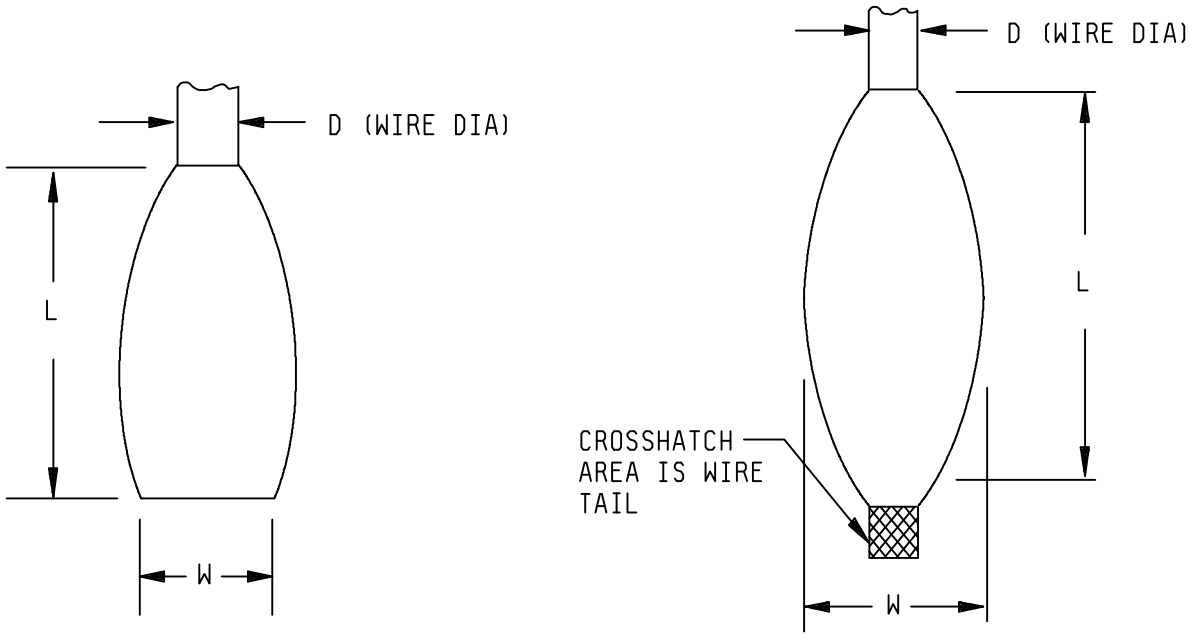
B. Die without guard ring.

FIGURE 2072-3. Cracks and chips.



A. Tailless or crescent.

NOTES:
1. 1.2.D ≤ W ≤ 5.0 D (width).
2. 0.5 D ≤ L ≤ 3.0 D (length).



B. Wedge.

Ultrasonic

NOTES:
1. 1.2 D ≤ W ≤ 3.0 D (width).
2. 1.5 D ≤ L ≤ 5.0 D (length).

Thermocompression

NOTES:
1. 1.2 D ≤ W ≤ 3.0 D (width).
2. 1.5 D ≤ L ≤ 5.0 D (length).

FIGURE 2072-4. Bond dimensions.

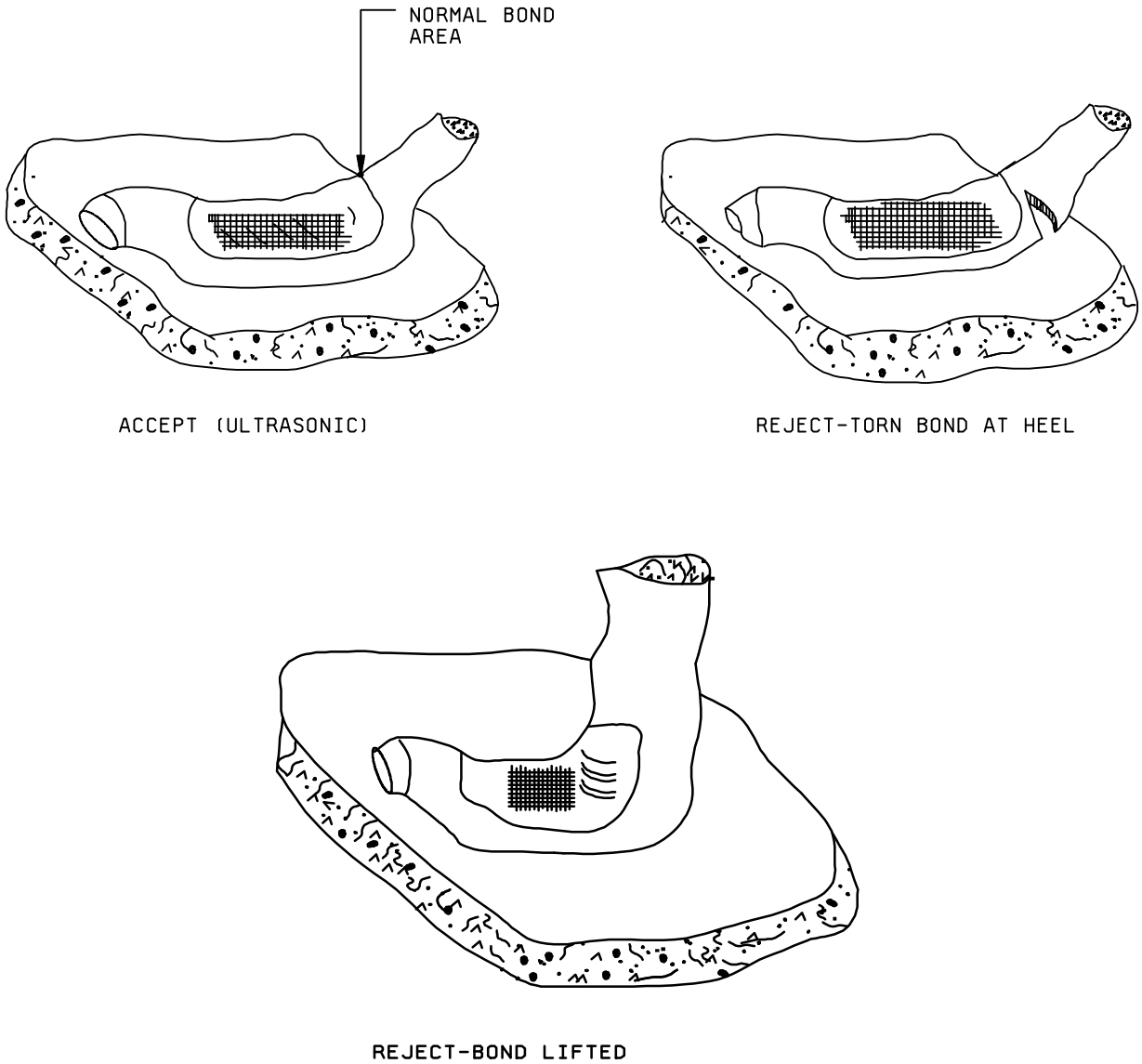
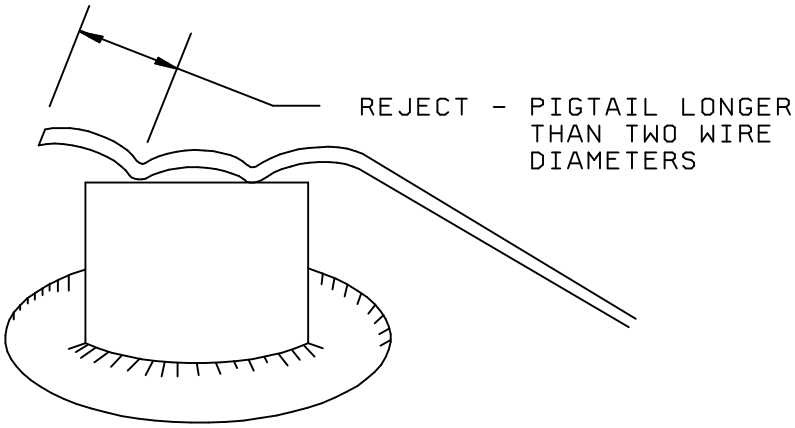
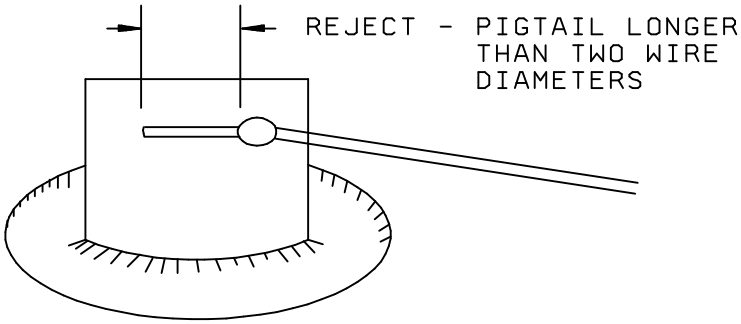


FIGURE 2072-5. Lift/torn bonds.





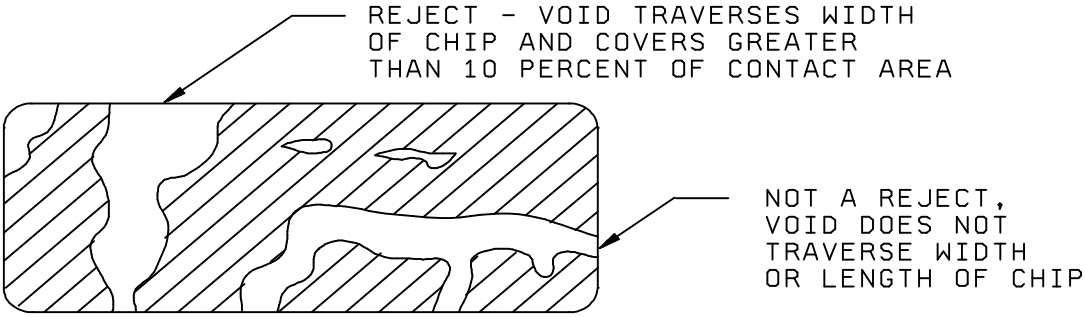


FIGURE 2072-6. Acceptable and unacceptable voids and excessive pigtails.

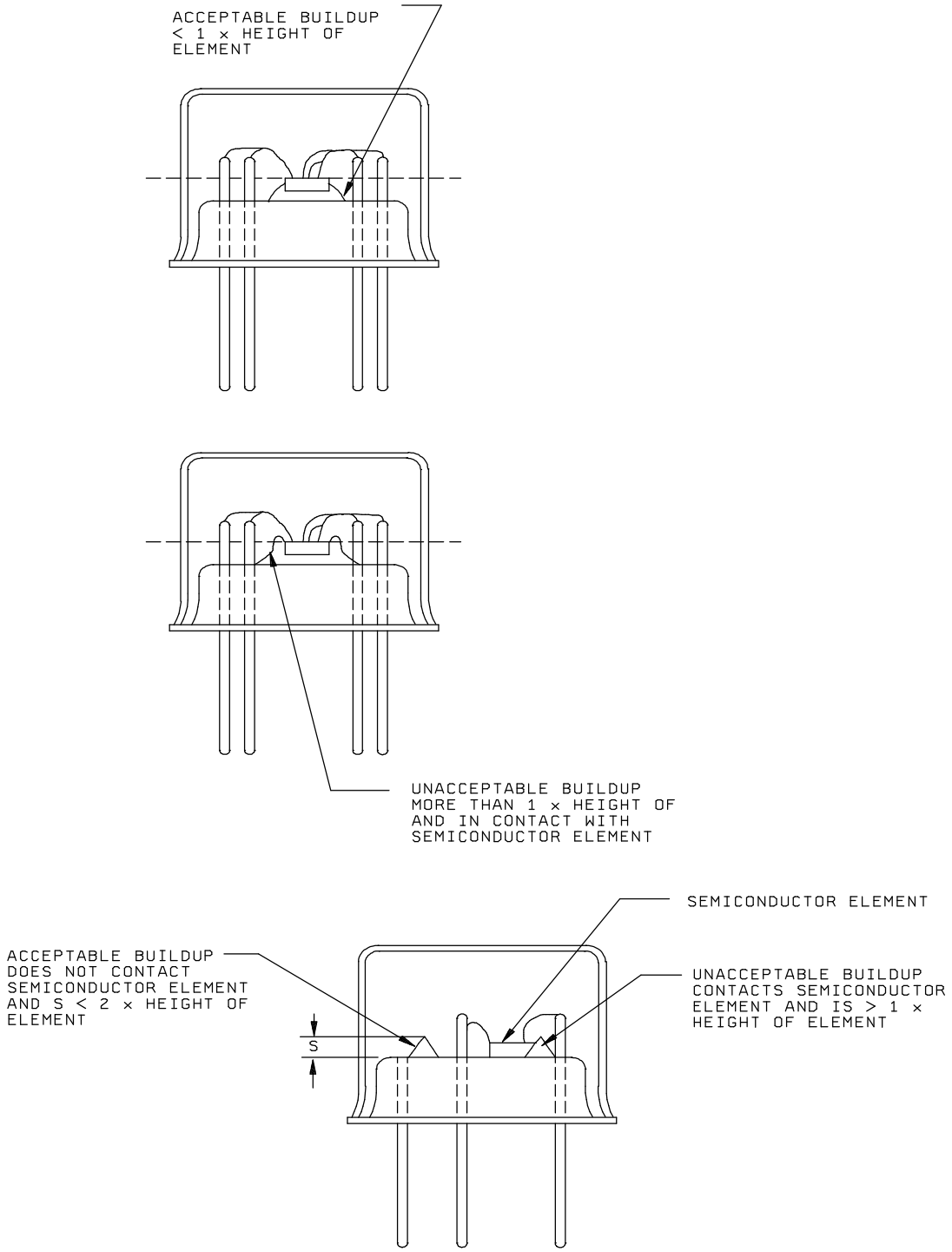
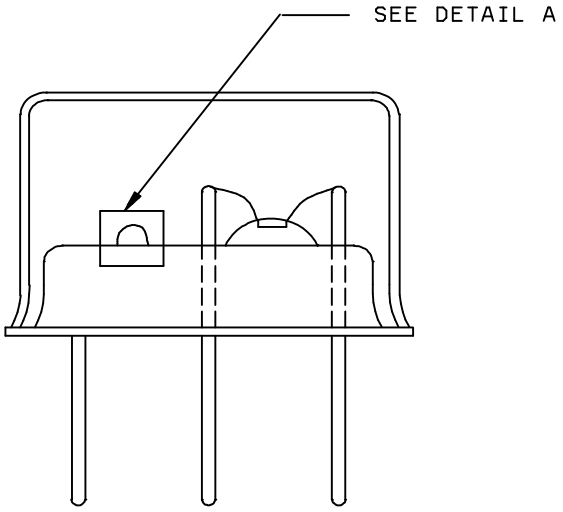
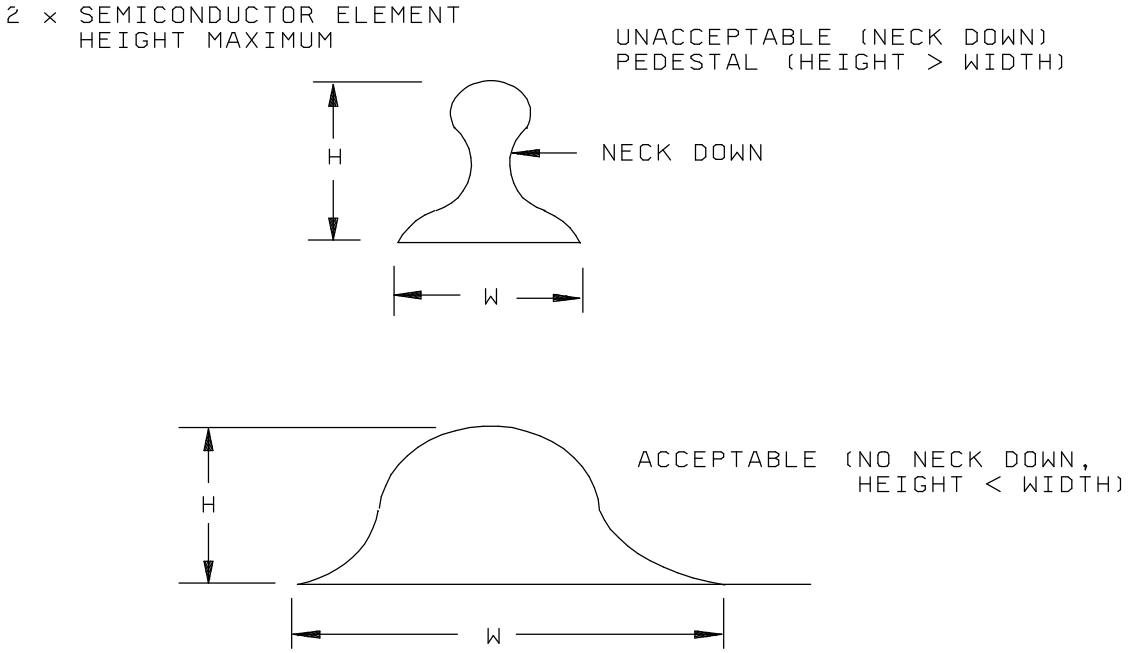


FIGURE 2072-7. Acceptable and unacceptable bonding material build-up.

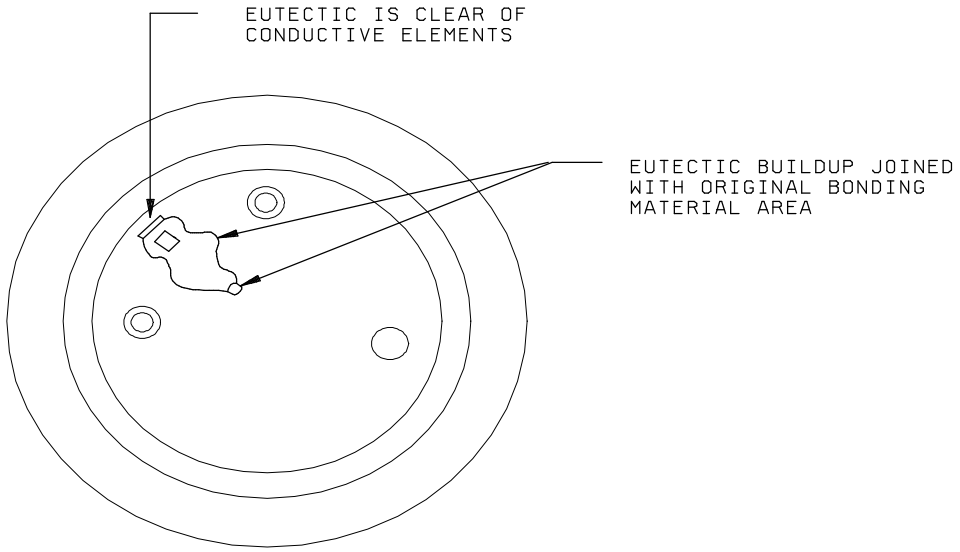




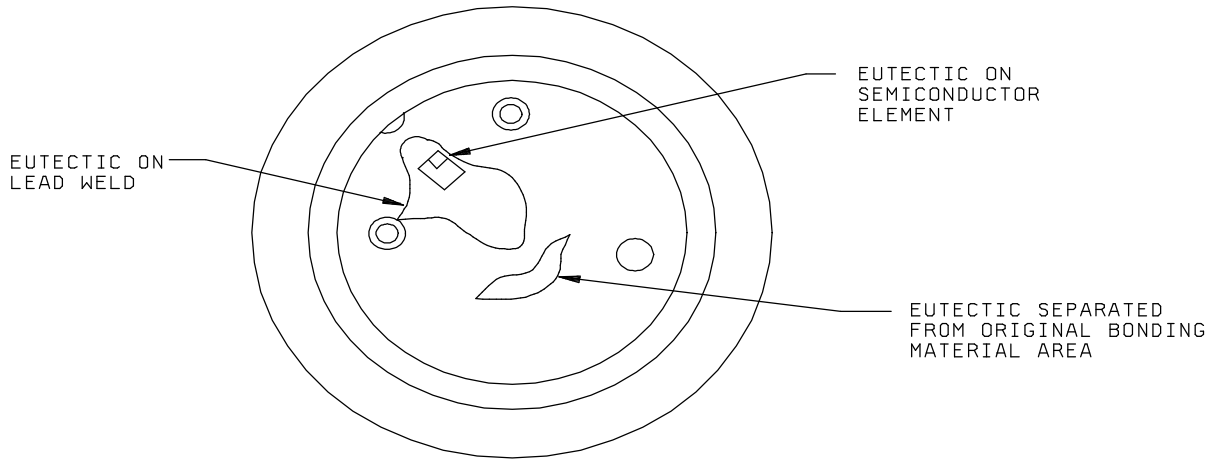
DETAIL A

NOTE: Die and wire are not necessarily visible.

FIGURE 2072-8. Extraneous bonding material build-up.



ACCEPTABLE



UNACCEPTABLE

FIGURE 2072-9. Acceptable and unacceptable excess material.

METHOD 2074.3

INTERNAL VISUAL INSPECTION (DISCRETE SEMICONDUCTOR DIODES)

1. Purpose. The purpose of this test is to check the materials, design, construction, and workmanship of discrete semiconductor diodes and other two-terminal semiconductor devices described herein. All tests shall be performed to detect and eliminate those devices with defects that could lead to device failures. Opaque glass type constructions shall be examined before encapsulation. (After encapsulation, see MIL-STD-750, method 2068). Metal can devices shall be examined before capping. (After capping or sealing, see MIL-STD-750, method 2071). Clear glass construction shall be examined after encapsulation.

2. Apparatus.

a. The apparatus for these tests shall include optical equipment and any visual standards (e.g., gauges, drawings, photographs) necessary to perform an effective examination and enable the operator to make objective decisions on the acceptability of the device being examined. Any necessary fixturing for handling devices during examination to promote efficient operation without damaging the units shall be provided.

b. A monocular, binocular, or stereo microscope capable of magnification from 20X minimum to 30X maximum, shall be used unless otherwise specified. The inspection shall be performed under suitable illumination.

3. Procedure. The devices shall be examined at the specified magnifications to determine compliance with the requirements of the applicable sections of this test method based on device construction. Examinations for transparent body devices may be performed anytime prior to body coating or painting. Axial lead devices shall be viewed at approximate right angles to their major axis while being rotated through 360°. For the time interval, if any, between visual inspection and package sealing, devices shall be stored, handled, and processed in a manner to avoid contamination and to preserve the integrity of the devices as inspected.

3.1 Small signal, computer, regulator, low power rectifiers, and microwave diodes.

3.1.1 Axial lead, transparent body, pressure contact design. The following examinations shall be made after encapsulation (C and S bend whisker).

3.1.1.1 Glass cracks and chips (see figure 2074-1). No cracks shall be allowed in the vicinity of the cavity. Any crack originating at either end of the package or crack that extends into the body of the glass toward the cavity more than 25 percent of the glass-to-glass or glass-to-metal seal length shall be cause for rejection. Any glass chip deep enough to expose the plug or lead surface and extending longitudinally into the glass-to-metal seal toward the cavity to reduce the effective seal length to less than one external lead diameter shall be cause for rejection.

3.1.1.2 Incomplete seal. All devices shall be inspected for glass-to-metal seal or glass-to-glass seal. Both seals shall be a minimum of one external lead diameter over the entire sealed portion (sealed interface).

3.1.1.3 Bubbles in seal. All devices shall be inspected for bubbles in the glass-to-metal or glass-to-glass seal. A series of bubbles that reduce the effective seal length to less than one external lead diameter shall be cause for rejection. Bubbles in the glass, but not effecting the glass-to-glass or glass-to-metal seal area, are not cause for rejection.

3.1.1.4 Glass package deformities (see figure 2074-2). Any glass envelope deformity equal to or greater than 75 percent of the external lead diameter shall be cause for rejection.

3.1.1.5 Extraneous matter. A device shall be rejected if there are unattached solder balls, semiconductor material, chips, flaked plating, or opaque material that is larger than the smallest distance between exposed active areas.

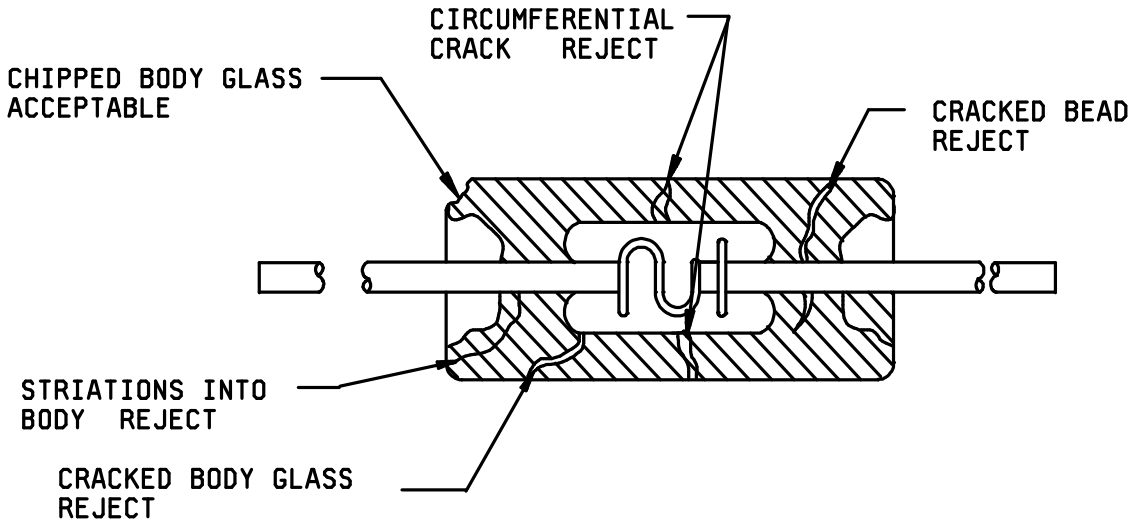


FIGURE 2074-1. Glass cracks and chips.

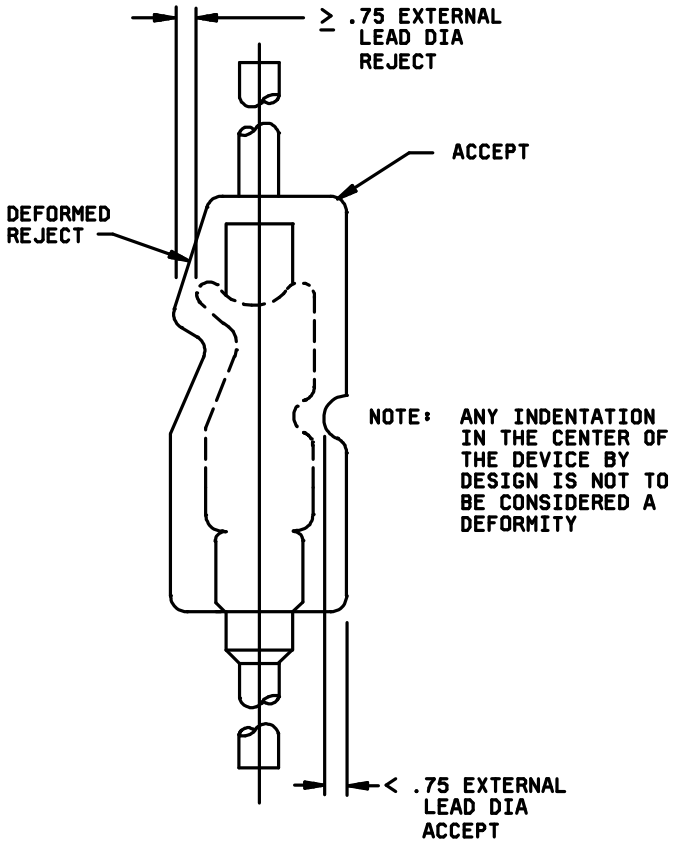


FIGURE 2074-2. Package deformities.

3.1.1.6 Solder protrusions (see figure 2074-3). All devices shall be inspected for solder protrusions. Any device with a protrusion that extends more than twice the smallest protrusion width shall be rejected.

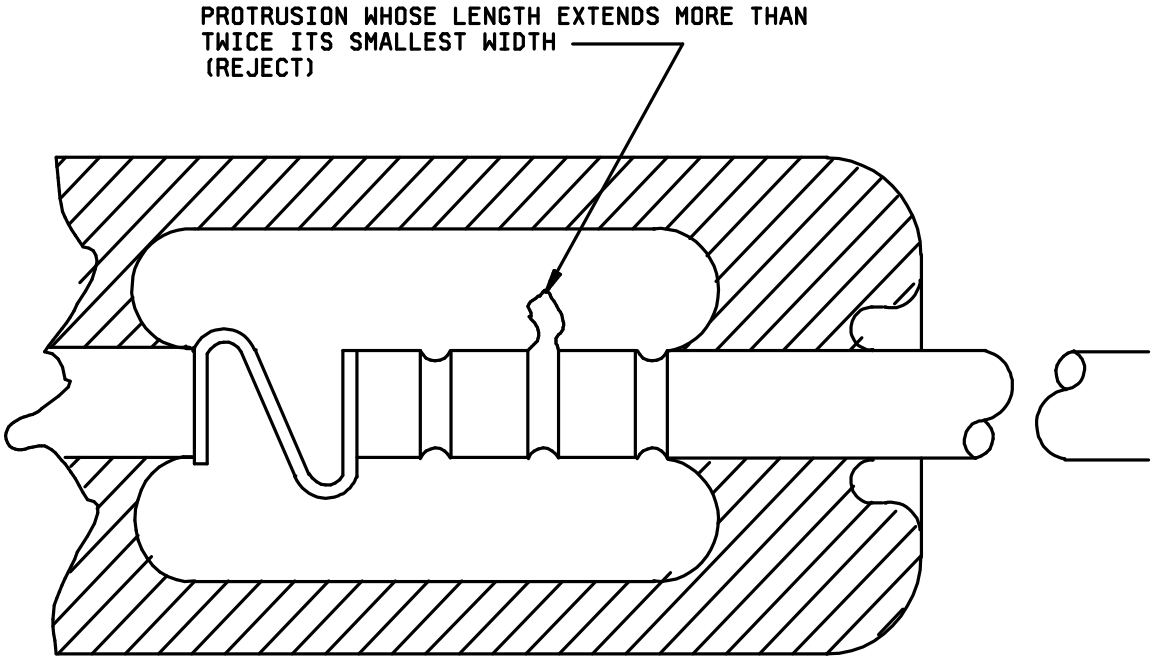


FIGURE 2074-3. Solder protrusions.

3.1.1.7 Pressure contact defects. The following misalignments or deformations shall be cause for rejection:

a. Whisker embedded within glass body wall (see figure 2074-4).

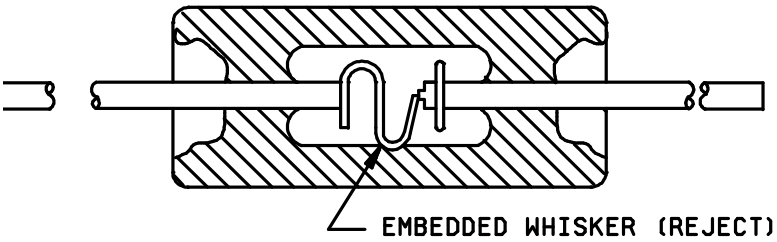


FIGURE 2074-4. Embedded whisker.

b. Toe contact between base of S or C spring and top surface of die caused by insufficient loading (see figure 2074-5).

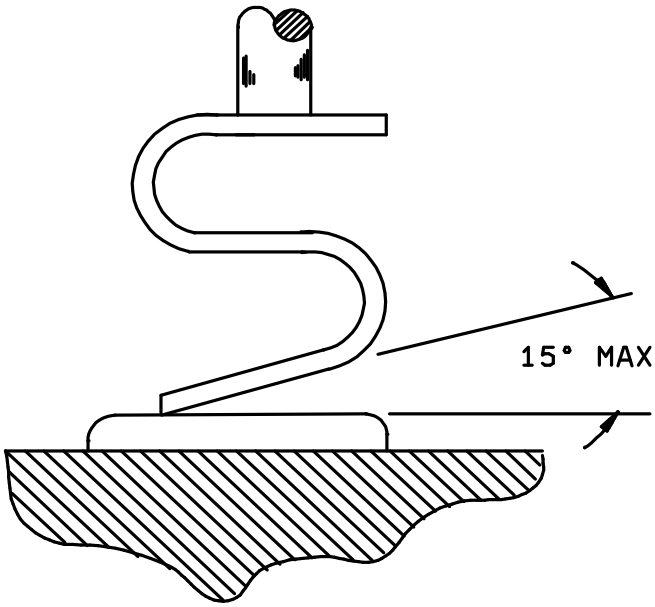


FIGURE 2074-5. Toe contact.

c. Toe contact on top surface of die (see figure 2074-6).

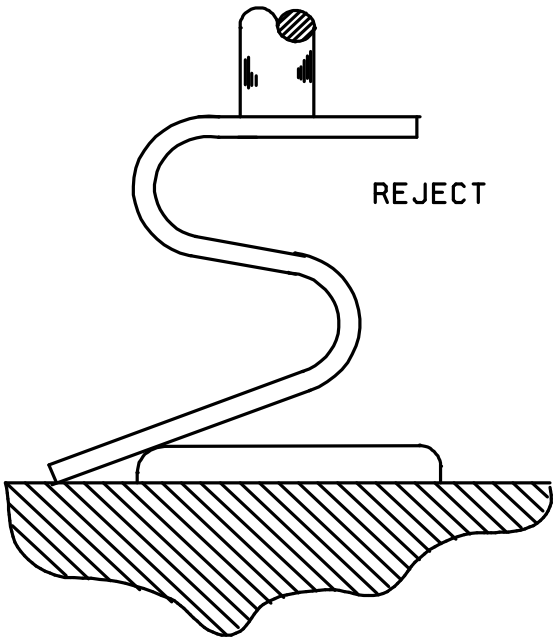


FIGURE 2074-6. Toe contact on top surface of die.

d. Heel contact between base of S or C spring and top surface of die (see figure 2074-7).

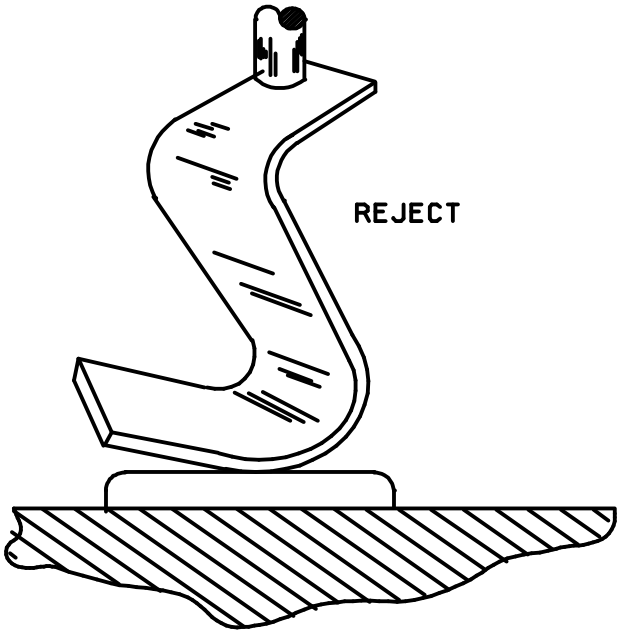


FIGURE 2074-7. Heel contact.

e. Point contact between base of S or C spring and top surface of die except by design (deformed or twisted whisker) (see figure 2074-8).

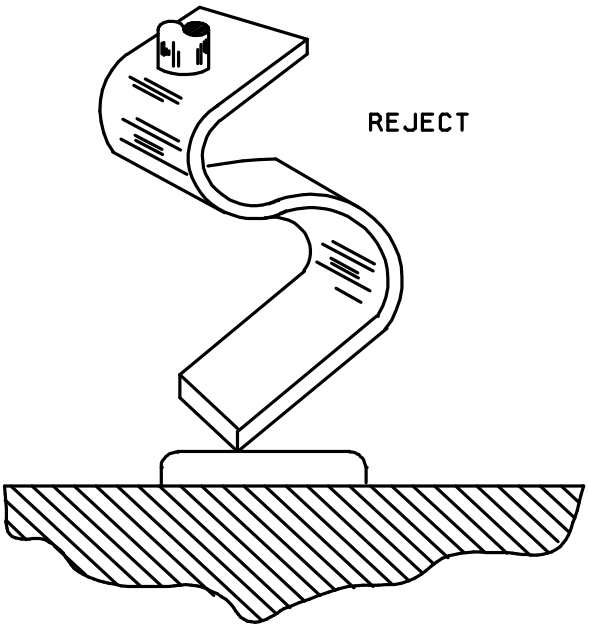
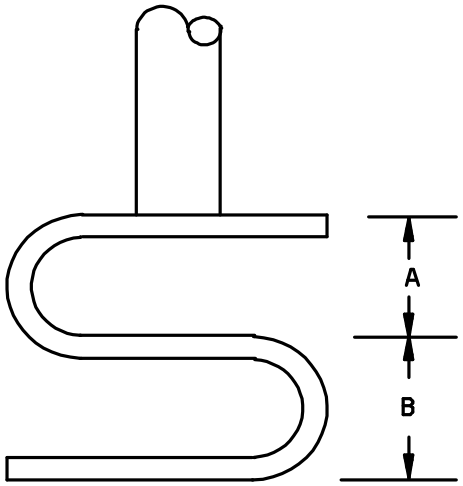


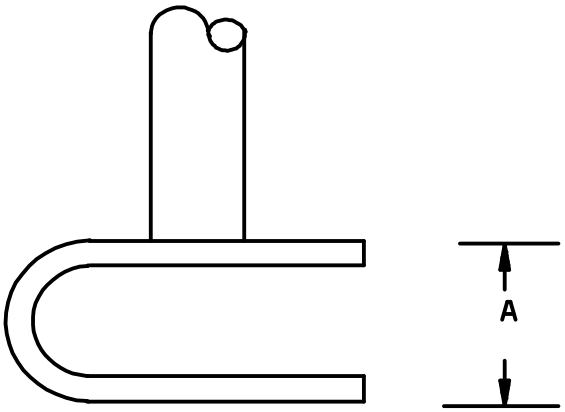
FIGURE 2074-8. Point contact.

f. Design compressed height (see figures 2074-9 and 2074-10). Either half of an S or C bend that is compressed so that any dimension is reduced to less that 50 percent of its design shall be rejected.



REJECT IF EITHER "A" OR "B" IS LESS THAN 50% OF ITS DESIGN COMPRESSED HEIGHT

FIGURE 2074-9. "S" whisker compressed height.



REJECT IF EITHER "A" IS LESS THAN 50% OF ITS DESIGN COMPRESSED HEIGHT

FIGURE 2074-10. "C" bend compressed height.

3.1.1.8 Whisker weld to post. Any device that exhibits weld splash or splatter (teardrop or balled) between whisker and post shall be rejected when it exceeds 25 percent of nominal lead diameter. The profile of the whisker weld to post shall not allow light penetration by more than 50 percent of lead diameter when using back lighting techniques.

3.1.1.9 Die to post or die to die contact area. Solder shall not be rough in appearance and shall be fused to a minimum of one-half the available bonding perimeter. Any solder overflow that touches the opposite surface of the die or dice shall be cause for rejection.

3.1.1.10 Die alignment (see figure 2074-11). A device shall be rejected if the die surface is not within 15° of being normal to the centerline of the mounting post.

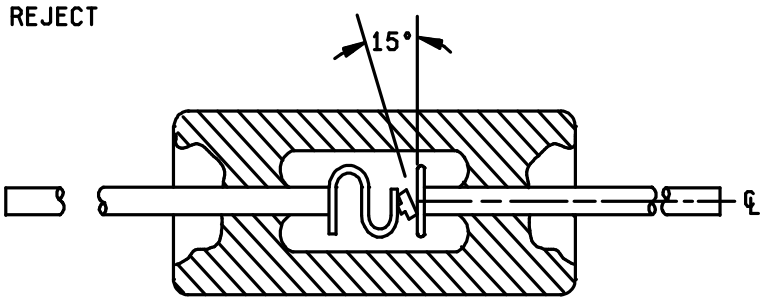


FIGURE 2074-11. Die alignment.

3.1.1.11 Lead alignment defects, (applicable to that portion of each lead within the glass envelope). A device lead which is either misaligned or bent so that it makes an angle with the principle device axis greater than 10° shall be rejected.

3.1.1.12 Multiple chip attachment defects. A multiple chip stack that tilts more than 10° from the principle axis of the device shall be cause for rejection.

3.1.2 Axial lead, metal body, solder contact design.

3.1.2.1 Examinations before capping.

a. Solder defects (see figures 2074-12 and 2074-13). Any device with a solder protrusion that extends more than twice the smallest protrusion width shall be rejected. Solder shall be smoothly formed from one element to another and shall be fused to a minimum of 50 percent of the perimeter between adjacent elements.

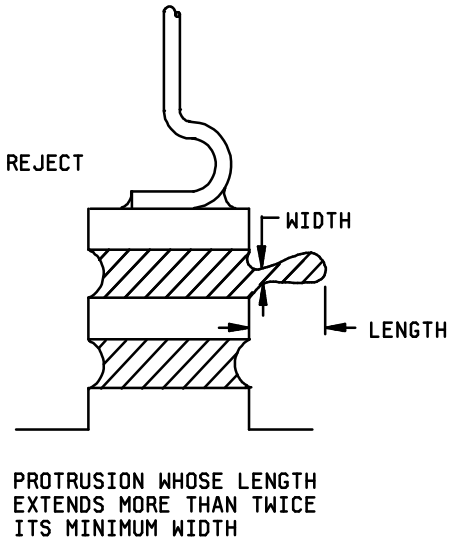


FIGURE 2074-12. Solder protrusion.

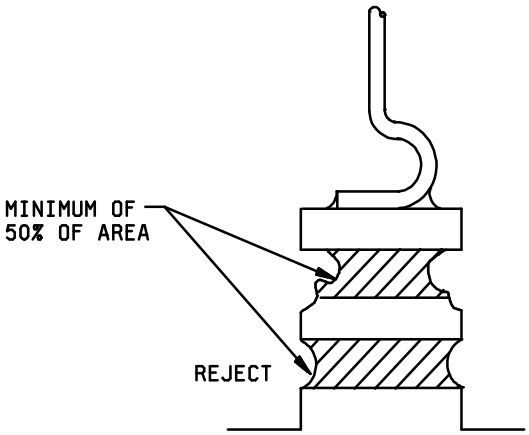


FIGURE 2074-13. Solder flow.

b. Alignment (see figure 2074-14). Any device whose element has its geometric center displaced more than 33 percent of its width from the die or die stack centerline shall be rejected.

c. Tilt (see figure 2074-15). Any element of a device that is tilted more than 10° from the mounting plane shall be cause for rejection.

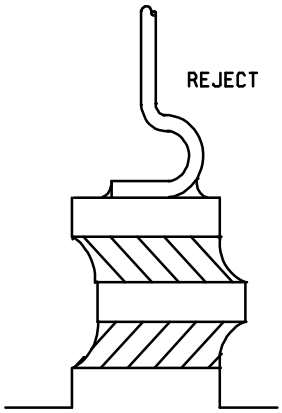


FIGURE 2074-14. Element alignment.

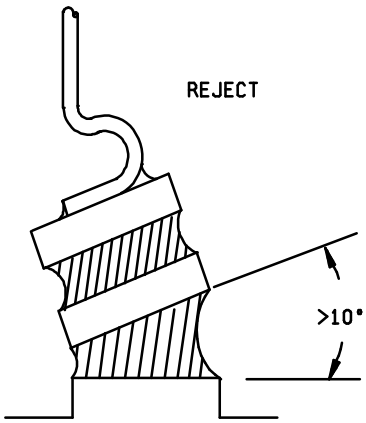


FIGURE 2074-15. Element tilt.

d. Die chipouts (see figure 2074-16). Any device die that exhibits chipouts extending more than 25 percent of the die width or to within 2 mils of the junction area shall be cause for rejection.

e. Die cracks (see figure 2074-17). Any die exhibiting cracks that reduce the total die area (or cracks extending into or across the junction area) to less than 75 percent of its original area shall be cause for rejection.

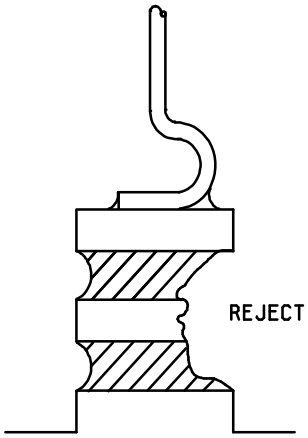


FIGURE 2074-16. Die chipout.

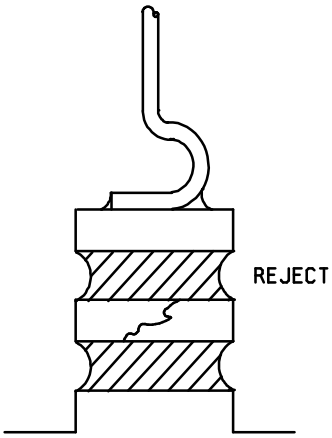


FIGURE 2074-17. Die cracks.

f. Extraneous matter. See 3.1.1.5.

3.1.3 Axial lead transparent body straight through lead to die contact (see figure 2074-18). All inspections for glass cracks, seals, bubbles, and deformities shall be as specified in 3.1.1.1 through 3.1.1.5. The following additional criteria shall be specified for the straight through construction after encapsulation but before body coating or painting.

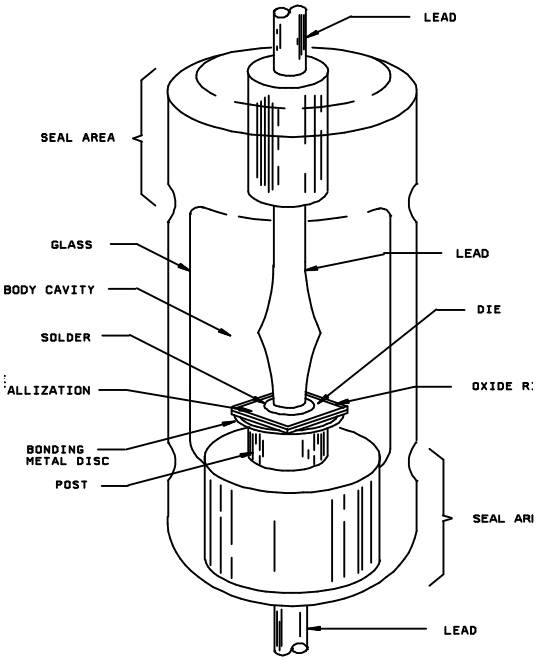


FIGURE 2074-18. Internal construction.

3.1.3.1 Die to post solder connection.

a. Solder voids (see figure 2074-19). A device shall be rejected if solder flow is less than 50 percent of the perimeter of the minimum available contact area of the post.

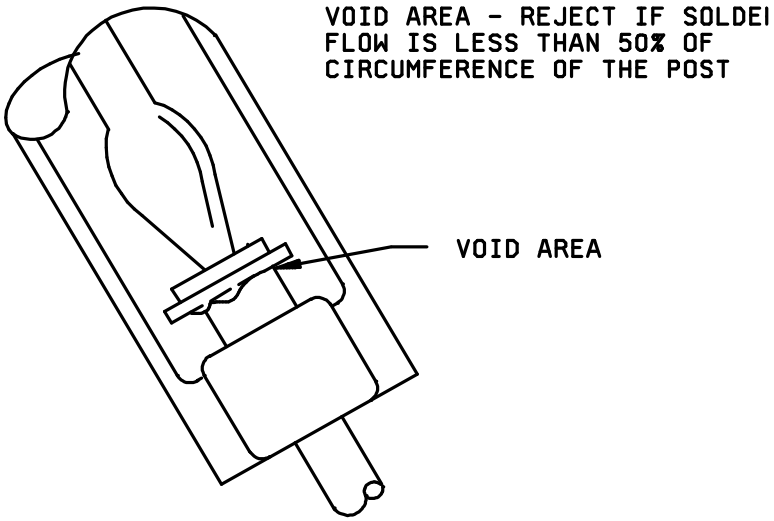


FIGURE 2074-19. Solder voids.

b. Solder overflow (see figure 2074-20). A device shall be rejected if any solder flow touches the opposite surface of the die.

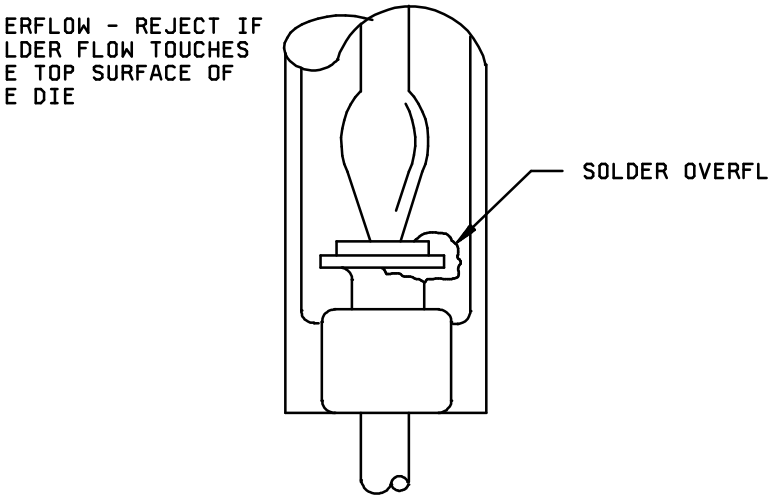


FIGURE 2074-20. Solder bridge.

3.1.3.2 Lead to die solder connection (see figure 2074-21). A device shall be rejected if more than 50 percent of the perimeter of the available contact area of the lead is void of solder.

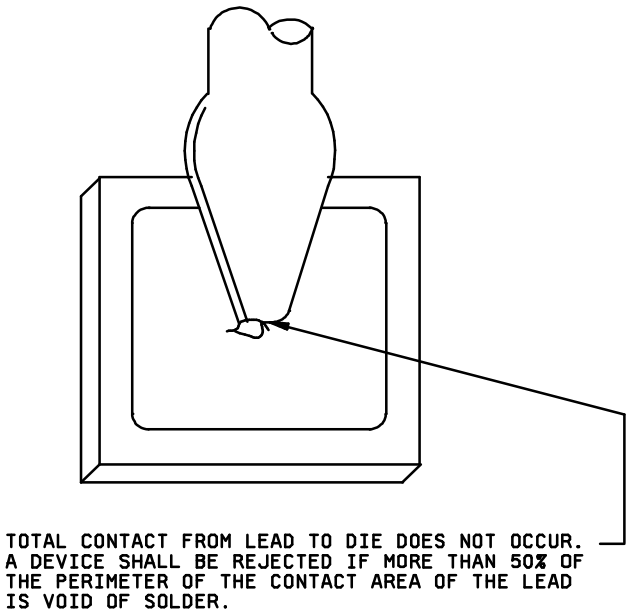


FIGURE 2074-21. Solder voids.

a. Solder overflow (see figure 2074-22). A device shall be rejected if solder flow extends beyond 50 percent of the distance from the metal to the outer edge of the oxide.

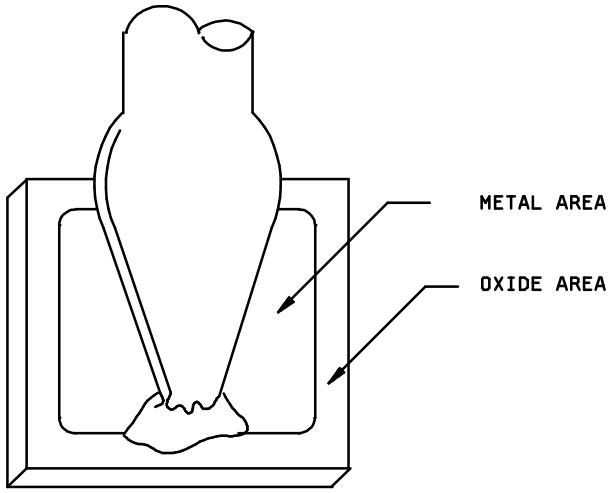


FIGURE 2074-22. Solder overflow.

b. Solder protrusion, slivers, and spikes (see figure 2074-23). A device shall be rejected if solder slivers and spikes are not securely attached to the main body. A securely attached sliver of spike is one having a cross sectional area greater at the area of attachment than anywhere else on the solder protrusion and having no necked down areas. Solder protrusions, slivers, and spikes whose length exceeds twice the smallest width of attachment shall be rejected.

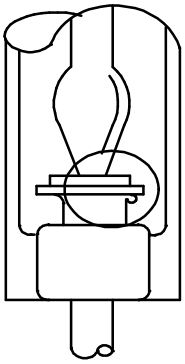


FIGURE 2074-23. Solder slivers and spikes.

c. Solder balls. A device shall be rejected if there are any insecurely attached solder balls. An insecurely attached solder ball is one whose major cross sectional area is more than twice the cross sectional area of the attachment.

3.1.3.3 Die to die solder connection (see figure 2074-24). A device shall be rejected if more than 50 percent of the perimeter of the available contact area of the die is void of solder.

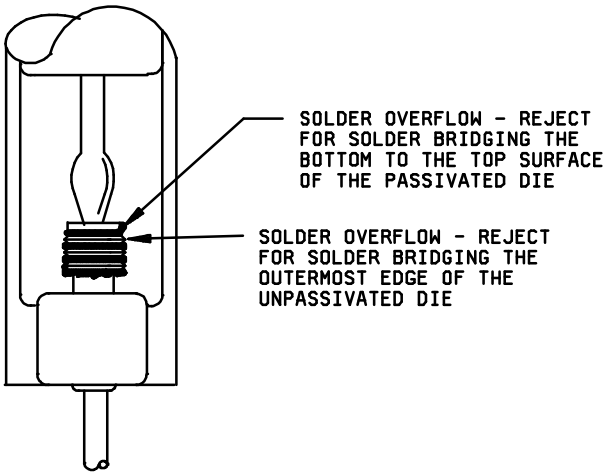


FIGURE 2074-24. Die to die solder connection.

3.1.4 Axial lead or MELF (where applicable), double plug, transparent body.

3.1.4.1 Glass cracks (see figure 2074-25). No cracks shall be allowed in the vicinity of the cavity or die. Any spiral or meniscus crack originating at either end of the package or glass that extends into the body of the glass toward the die more than 25 percent of the designed seal length shall be cause for rejection. Any chip deep enough to expose the plug surface and extending longitudinally into the glass toward the die more than 25 percent of the designed seal length shall be cause for rejection.

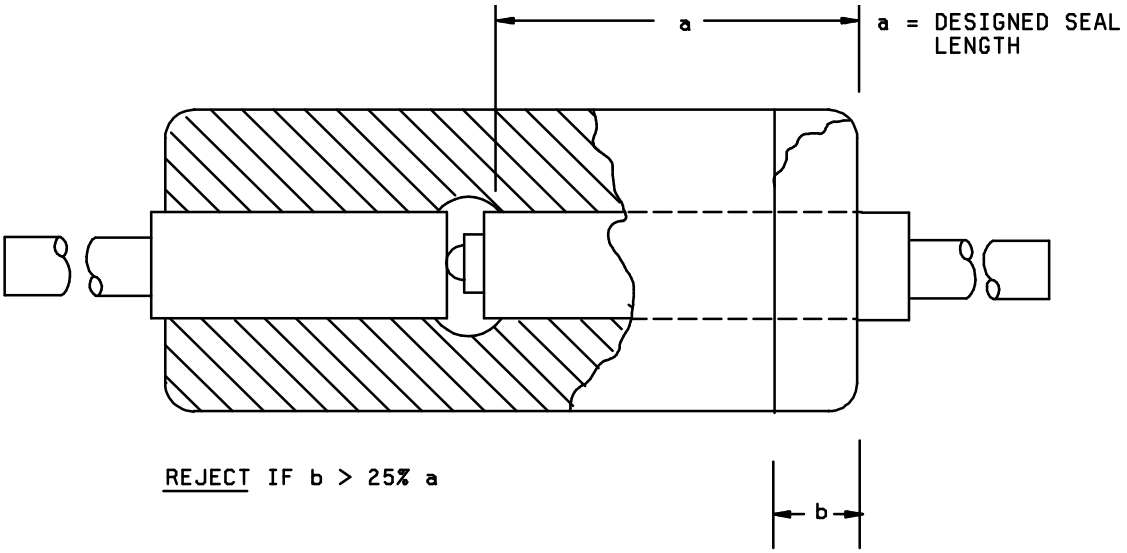


FIGURE 2074-25. Glass cracks.

3.1.4.2 High seal (see figure 2074-26). Any device which displays a glass case off center condition reducing the seal band of either plug by more than 25 percent of its designed length shall be cause for rejection.

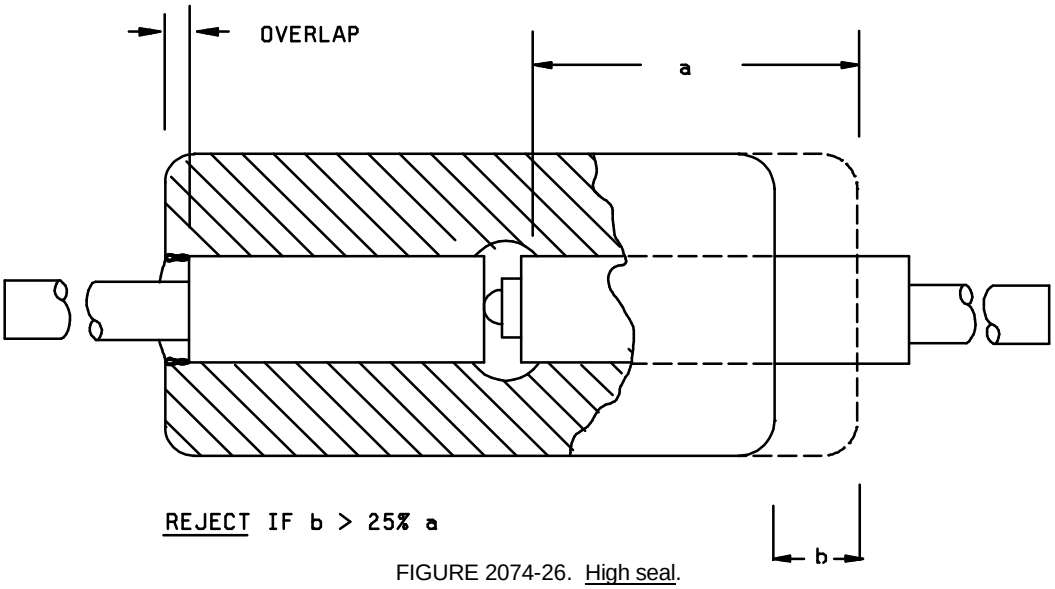
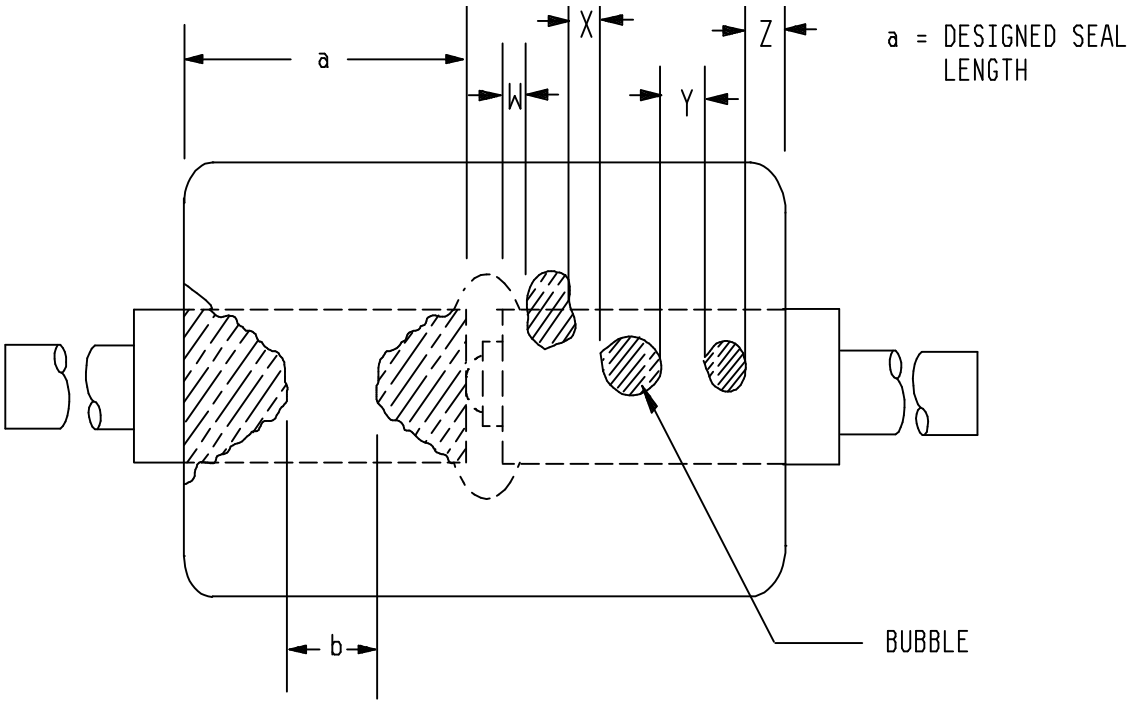


FIGURE 2074-26. High seal.

3.1.4.3 Low seal (see figure 2074-27). Any anomaly such as bubbles, plug blisters, separations, leaching, or undersealing that affects the combined seal length of either plug by allowing a sealing band less than 50 percent of the designed seal length on any package type shall be cause for rejection.



REJECT IF b < 50% a

REJECT IF W +X +Y +Z < 50% a

FIGURE 2074-27. Low seal.

3.1.4.4 Plug alignment (see figures 2074-28 and 2074-29). All devices shall be inspected for proper plug alignment. A plug displacement distance more than 25 percent of the diameter of the plug shall be cause for rejection. The plug shall not tilt to the degree that it touches the chip or is misaligned from the other plug axis more than 5°.

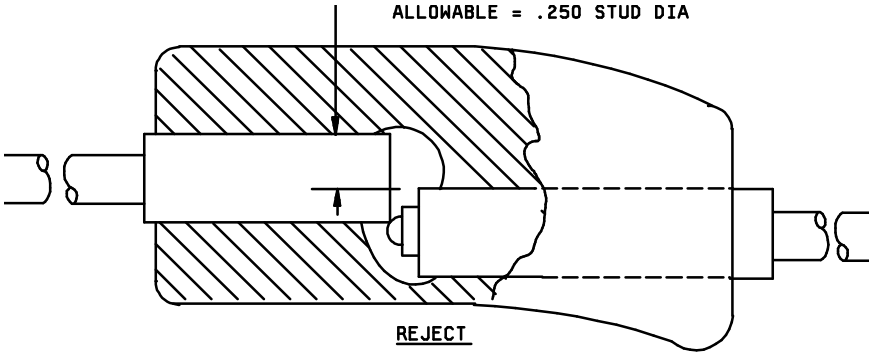


FIGURE 2074-28. Plug alignment.

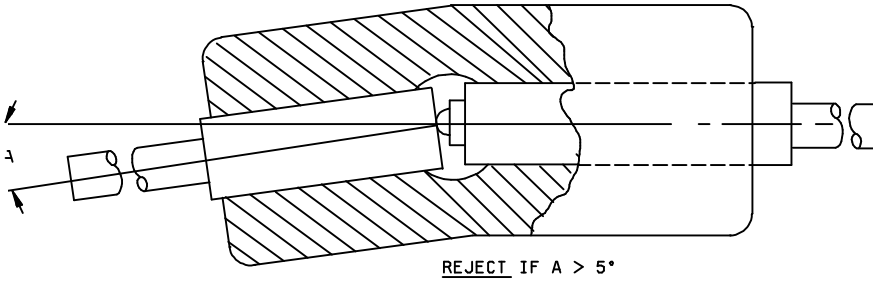


FIGURE 2074-29. Plug displacement.

3.1.4.5 Extraneous matter. A device shall be rejected if there are unattached solder balls, semiconductor material, chips, flaked plating, or opaque material that is larger than the smallest distance between exposed active areas.

3.1.4.6 Lead connections (see figure 2074-30). Lead to plug connections shall be inspected for incomplete welds. Any partial welds less than 75 percent of total weld area shall be cause for rejection.

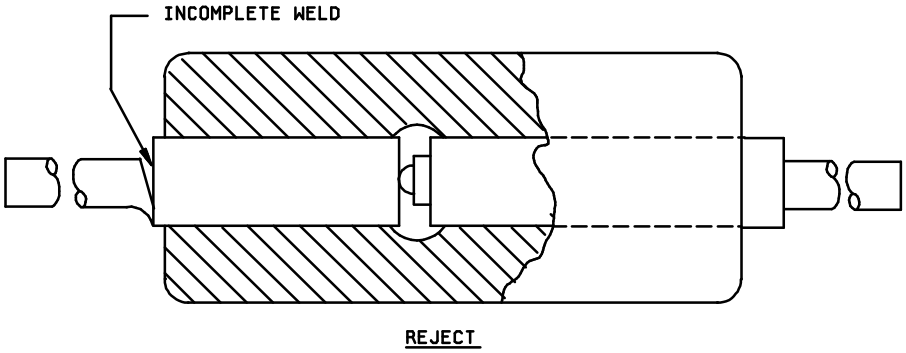


FIGURE 2074-30. Incomplete weld.

3.1.5 Axial lead, transparent body, point contact. All inspections for glass cracks, seals, bubbles, and deformities shall be as specified in 3.1.1.1 through 3.1.1.5. The following additional criteria shall be specified for the point contact construction after encapsulation but before body coating or painting.

3.1.5.1 Pressure contact defects. The following misalignments or deformities shall be cause for rejection:

a. Whisker touches glass body wall (see figure 2074-31).

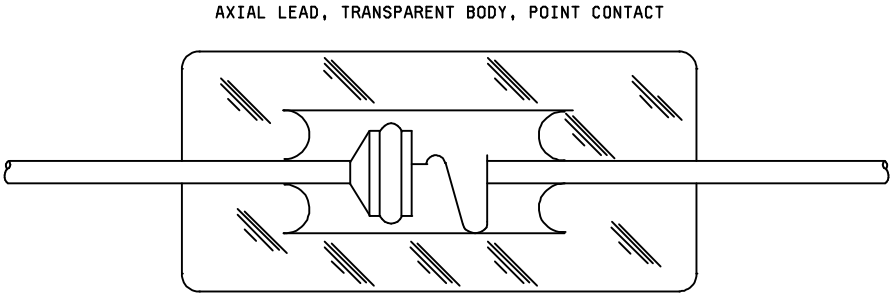


FIGURE 2074-31. Whisker touches glass body wall (reject).

b. Whisker loops touch one another (see figure 2074-32).

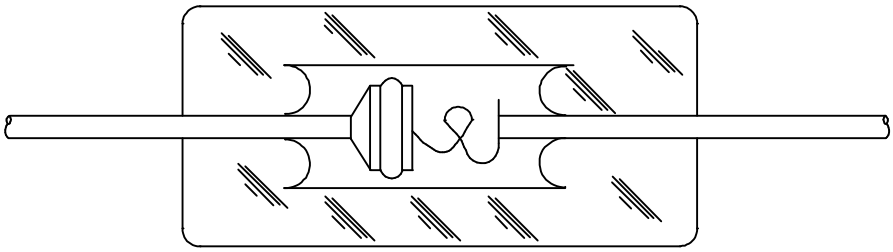


FIGURE 2074-32. Whisker loops touch one another (reject).

c. Whisker angle over 10° from normal (see figure 2074-33).

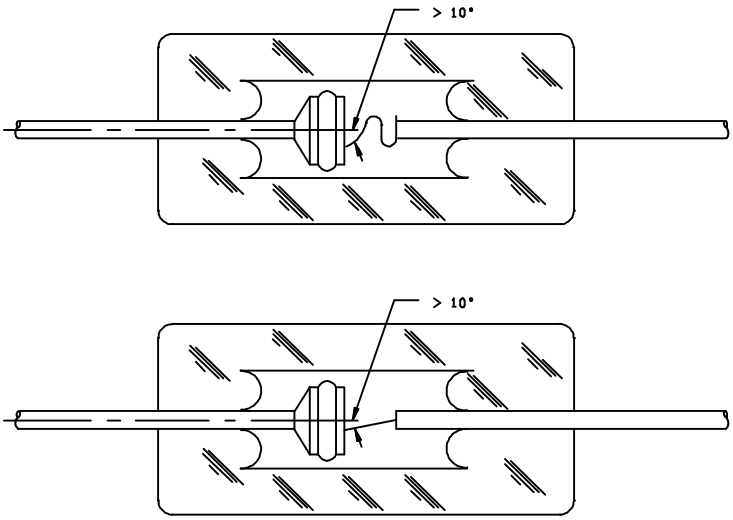


FIGURE 2074-33. Whisker angle over 10° from normal (reject).

3.1.5.2 Whisker weld to post. Any device that exhibits weld splash or splatter (tear dropped or balled) between whisker and post shall be rejected when it exceeds 25 percent of nominal lead diameter. The profile of whisker weld to the post shall not allow light penetration by more than 50 percent of lead diameter when using back lighting techniques.

3.1.5.3 Solder voids. A device shall be rejected if solder flow is less than 50 percent of the perimeter of the minimum available contact area of the die.

3.1.5.4 Die to post contact area. Solder shall be smoothly formed from one element to another and shall be fused to a minimum of one-half the available bonding area. Any solder overflow that touches the opposite surface of the die shall be cause for rejection.

3.1.5.5 Die alignment. A device shall be rejected if the die surface is not within 15° of being normal to the centerline of the mounting post.

3.1.5.6 Lead alignment defects (applicable to that portion of each lead within the glass envelope). A device whose lead is either misaligned or bent so that is makes an angle with the principle device axis greater than 10° shall be rejected.

3.1.5.7 Die touches glass package (see figure 2074-34). A device shall be rejected if the die touches the glass envelope.

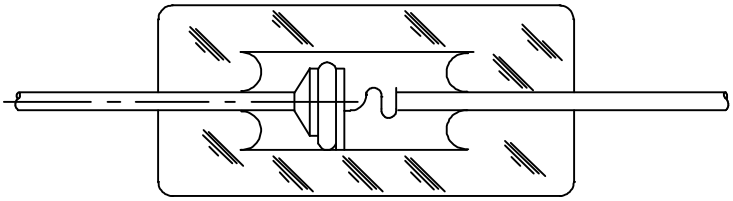


FIGURE 2074-34. Die touches glass package (reject).

3.2 Power rectifiers and regulators.

3.2.1 Axial lead double plug opaque body.

3.2.1.1 Die mounting and alignment. After bonding die to the heat sink, plugs, or leads, the following shall be inspected for defects:

a. Die geometry. A die shall be rejected if it is chipped or broken to the extent that 75 percent or less of the original surface remains.

b. Axial alignment of plugs and die. Plugs shall be aligned axially within one-eighth of the diameter of either plug.

c. Tilted die. A device shall be rejected if the die is tilted so that the die surface is greater than 5° from being perpendicular to the mounting post axis.

3.2.1.2 Die cracks. Any die exhibiting cracks that reduce the total die area (or cracks extending into or across the junction area) to less than 75 percent of its original area shall be cause for rejection.

3.2.1.3 Inadequate brazing. A device shall be rejected if less than 90 percent of the visible metallized surface (perimeter) is brazed to the heat sink or lead.

3.2.1.4 Flaking or loose material. No unattached solder, braze, or other bonding material shall extend from the plugs. Any blistering or peeling of plug surface shall be cause for rejection.

3.2.1.5 Extraneous matter. A device shall be rejected if there is any extraneous, particulate matter between the terminal plugs or on the plug surface. No foreign stains shall be permitted on plug surfaces.

3.2.2 Axial lead, double plug, transparent body. The inspections in 3.2.2.1 through 3.2.2.4 may be performed on a sealed device if all inspection criteria are clearly visible and detectable. After bonding the die to the heat sink, plugs, or leads, the following shall be inspected for defects.

3.2.2.1 Axial alignment of plugs and die. Plugs shall be aligned within one-eighth of the diameter of either plug.

3.2.2.2 Tilted die. A device shall be rejected if the die is tilted so that the die surface is greater than 5° from being perpendicular to the mounting post axis.

3.2.2.3 Inadequate brazing. A device shall be rejected if less than 90 percent of the visible metallized surface (perimeter) is brazed to the heat sink or lead.

3.2.2.4 Flaking or loose material. No unattached solder, braze, or other bonding material shall extend from the plugs. Any blistering or peeling of plug surface (cavity type) shall be cause for rejection. Any blistering or peeling of plug surface (non-cavity type) which reduces designed seal length to less than 25 percent shall be cause for rejection.

3.2.2.5 Extraneous matter. A device shall be rejected if there are unattached solder balls, semiconductor material, chips, flaked plating, or opaque material that is larger than the smallest distance between exposed active areas.

3.2.2.6 Cracks in glass. No cracks shall be allowed in the vicinity of the cavity. Any crack originating at either end of the package or crack that extends into the body of the glass toward the cavity more than 25 percent of the glass-to-glass or glass-to-metal seal length shall be cause for rejection. Any glass chip deep enough to expose the plug, or lead surface and extending longitudinally into the glass-to-metal seal toward the cavity to reduce the effective seal length to less than one external lead diameter shall be cause for rejection.

3.2.2.7 Glass bubbles. All devices shall be inspected for bubbles in the glass-to-metal or glass-to-glass seal. A series of bubbles that reduce the effective seal length to less than one external lead diameter shall be cause for rejection.

3.2.2.8 Encapsulant position. A device shall be rejected if the encapsulant covers less than 80 percent of the design plug surface.

3.2.3 Metal body devices. The following inspections shall be made prior to capping.

3.2.3.1 Die and lead assembly (see figures 2074-35 and 2074-36). The die and lead assembly shall be located on the base pedestal so that there is complete contact over the design contact area. The lead shall be free of nicks and scrapes that reduce the lead diameter by more than 5 percent. The die and lead assembly shall not be tilted more than 5° with respect to the base.

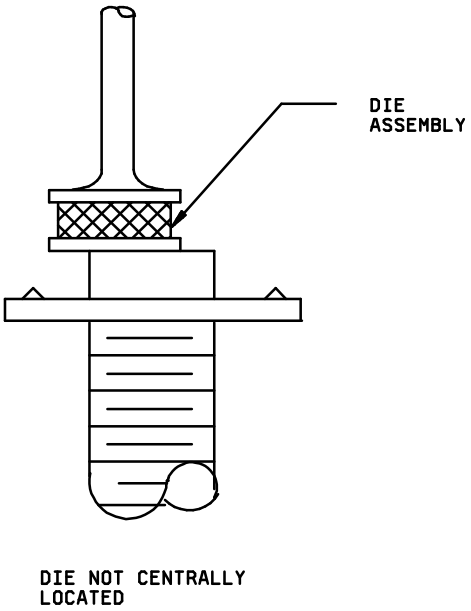


FIGURE 2074-35. Offset die.

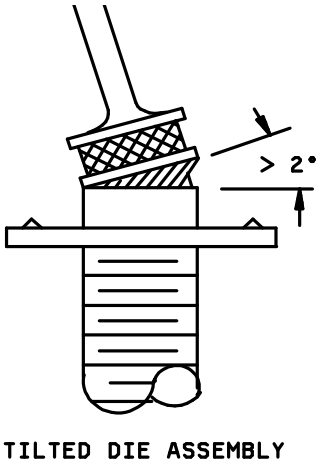


FIGURE 2074-36. Tilted die.

3.2.3.2 Extraneous matter.

a. Solder slivers and spikes. A device shall be rejected if solder slivers and spikes are not securely attached to the parent body of the solder. A securely attached sliver or spike is one having a cross sectional area greater at the area of attachment than anywhere else on the solder protrusion and having no necked-down areas.

b. Foreign matter. A device shall be rejected if there are unattached solder balls, semiconductor materials, chips, flaked plating, or opaque material that is larger than the smallest distance between exposed active areas.

c. Multiple die attachments. A device shall be rejected if the attached portion of an adjacent die exceeds 25 percent of the die area.

3.2.3.3 Assembly defects.

a. Tilted elements. A device shall be rejected if any element of the assembly is tilted in excess of 10E from the normal mounting plane.

b. Misaligned elements. A device shall be rejected if any element of the assembly is misaligned or displaced in excess of 33 percent of its width from the die or die stack centerline, bridges two active regions, or extends beyond the isolation region of the oxide.

3.2.3.4 Metal body diamond base regulators (see figure 2074-37).

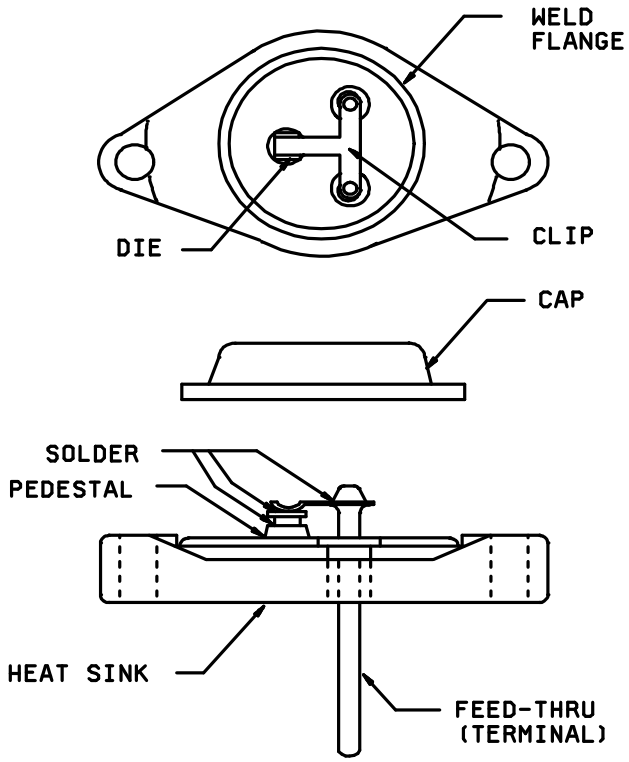


FIGURE 2074-37. Diamond base construction.

3.2.3.4.1 Die to pedestal and die to clip solder connections.

a. Solder voids. A device shall be rejected if solder flow is less than 50 percent of the perimeter of the minimum available contact area.

b. Solder overflow. A device shall be rejected if any solder flow bridges from the top to bottom surface of the die or reduces the normal separation of two active regions by 50 percent or more.

3.2.3.4.2 Clip to post and feed through to heat sink solder connections.

a. Solder voids. A device shall be rejected if the wetting action of the solder to each member of the connection is not continuous.

b. Solder overflow. A device shall be rejected if any solder flow extends on to any portion of the weld flange of the heat sink.

4. Summary.

a. Detailed requirements for materials, design, construction, and workmanship.

b. Magnification requirements, if other than specified.

METHOD 2076.3

RADIOGRAPHY

1. Purpose. The purpose of this examination is to nondestructively detect defects within the sealed case, especially those resulting from sealing of the lid to the case, and internal defects such as foreign objects, improper interconnecting wires, and voids in the die attach material or in the glass when glass seals are used. This test establishes methods, criteria, and standards for radiographic examination of discrete devices.

NOTE: For certain case types, the electron shielding effects of device construction materials (packages or internal) may effectively prevent radiographic identification of certain types of defects from some or all possible viewing angles. This factor should be considered in relation to the design of each when application of this test method is specified.

2. Apparatus. The apparatus and materials for this test shall include:

a. Radiographic equipment with a sufficient voltage range to penetrate the device. The focal distance shall be adequate to maintain a sharply defined image of a object with a major dimension of .001 inch (0.025 mm).

b. Radiographic film: (Eastman type R or equivalent).

c. Radiographic viewer capable of .001 inch (0.025 mm) resolution in any major dimension.

d. Holding fixtures capable of holding devices in the required positions without interfering with the accuracy or ease of image interpretation.

e. Radiographic quality standards capable of verifying the ability to detect all specified defects for particular package types being x-rayed.

f. A .062 inch (1.57 mm) minimum lead topped table shall be used to prevent back scatter of radiation.

3. Procedure. The x-ray exposure factors, voltage, milliampere setting and time settings shall be selected or adjusted as necessary to obtain satisfactory exposures and achieve maximum image details within the sensitivity requirements for the device or defect features the radiographic test is directed toward. Unless otherwise specified, the x-ray voltage shall be the lowest consistent with these requirements and shall not exceed 150 kV. Although higher voltages may be necessary to penetrate certain packages, these levels may be damaging to some device technologies.

3.1 Mounting and views. The devices shall be mounted in the holding fixture so that the devices are not damaged or contaminated and are in the proper plane as specified. The devices may be mounted in any type of fixture and masking with lead diaphragms or barium clay may be employed to isolate multiple specimens provided the fixtures or masking materials do not block the path of the x-rays to the film or any portion of the device.

3.1.1 Views.

a. Unless otherwise specified, flat packages and single ended cylindrical devices shall have one view taken with the x-rays penetrating in the Y direction as defined in figures 1 and 2 of the general requirements herein. When more than one view is required, the second and third views, as applicable, shall be taken with the x-rays penetrating in the X and Z directions respectively.

b. Unless otherwise specified, stud-mounted and cylindrical axial lead devices shall have one view taken with the x-rays penetrating in the X direction as defined in figures 1 and 2 of the general requirements herein. When more than one view is required, the second and third views, as applicable, shall be taken with the x-rays penetrating in the Z direction and at 45E between the X and Z directions.

c. All JANS devices shall have two views taken with x-rays penetrating in the X and Y directions, stud-mounted and axial lead device views shall be taken with x-rays penetrating in the X and Z directions.

3.2 Radiographic quality standard. The radiographic quality standard shall consist of a suitable standard penetrameter such as radiographic quality standard ASTM type B - Image quality indicator for semiconductor radiography or equivalent device. Each radiograph shall have two image quality standards exposed with each view located (and properly identified) in opposite corners of the film. The radiographic density of penetrameters chosen shall bracket the density of the devices beings inspected.

3.3 Film and marking. The radiograph film shall be in a film holder backed with a minimum of .062 inch (1.57 mm) lead or the holder shall be placed on the lead topped table (see 2.f). The film shall be identified using techniques that legibly print the following information, photographically on the radiograph:

a. Device manufacturer's name or code identification number.

b. Device type or Part or Identifying Number (PIN).

c. Production lot number, date code, or inspection lot number.

d. Radiographic film view number and date.

e. Device serial or cross reference numbers, when applicable (see 3.3.2).

f. X-ray laboratory identification, if other than device manufacturer.

g. X-ray axis view (X, Y, or Z).

3.3.1 Nonfilm techniques, when specified. The use of nonfilm techniques is permitted under the following conditions:

a. Permanent records are not required.

b. The equipment is capable of producing results of equal quality when compared with film techniques.

c. All requirements of this method are complied with except those pertaining to the actual film.

3.3.2 Serialized devices. When device serialization is required, each device shall be readily identified by a serial number. The devices shall be radiographed in consecutive, increasing serial order. When a device is missing, the blank space shall contain either the serial number or other x-ray opaque objects to readily identify and correlate the x-ray data. When more than one consecutive device is missing within serialized devices, the serial number of the last device before the skip and the first device after the skip may, at the manufacturers option, be used in place of the multiple opaque objects.

3.3.3 Special device marking. When specified (see 4.c), the devices that have been x-rayed and found acceptable shall be identified with a blue dot on the external case. The blue dot shall be approximately .062 inch (1.57 mm) in diameter. The color selected from FED-STD-595 shall be any shade between 15102-15123 or 25102-25109. The dot shall be placed so that it is readily visible but shall not obliterate other device marking.

3.4 Tests. The x-ray exposure factor shall be selected to achieve resolution of .001 inch (0.025 mm) major dimension, less than 10 percent distortion and an "H" and "D" film density between 1 and 2.5 in the area of interest of the device image. Radiographs shall be made for each view required (see 4.).

3.5 Processing. The radiographic film manufacturer's recommended procedure shall be used to develop the exposed film, and film shall be processed so that it is free of processing defects such as fingerprints, scratches, fogging, chemical spots, blemishes.

3.6 Operating personnel. Personnel who will perform radiographic inspection shall have training in radiographic procedures and techniques so that defects revealed by this method can be validly interpreted and compared with applicable standards. The following minimum vision requirements shall apply for visual acuity of personnel inspecting film as well as personnel authorized to conduct radiographic tests:

a. Distant vision shall equal at least 20/30 in both eyes, corrected or uncorrected.

b. Near vision shall be such that the operator can read Jaegger type No. 2 at a distance of 16 inches (406.4 mm), corrected or uncorrected.

c. Vision tests shall be performed by an oculist, optometrist, or other professionally recognized personnel at least once a year.

3.7 Interpretation of radiographs. Utilizing the equipment specified herein, radiographs shall be inspected to determine if each device conforms to this standard or if it is defective and shall be rejected. Interpretation of the radiograph shall be made under low light level conditions without glare on the radiographic viewing surface. The radiographs shall be examined on a suitable illuminator with variable intensity or on a viewer suitable for radiographic inspection on projection type viewing equipment. The radiograph shall be viewed at a magnification between 6X and 20X. Viewing masks may be used when necessary. Any radiograph not clearly illustrating the features in the radiographic quality standards is not acceptable and another radiograph of the devices shall be taken.

3.8 Reports and records.

3.8.1 Reports of inspection. For JANS devices, or when specified for other device classes, the manufacturer shall furnish inspection reports with each shipment of devices. The report shall describe the results of the radiographic inspection, and list the purchase order number or equivalent identification, the PIN, the date code, the quantity inspected, the quantity rejected, and the date of test. For each rejected device, the PIN, the serial number, when applicable, and the cause for rejection shall be listed.

3.8.2 Radiograph submission. When specified, one set of the applicable radiographs shall accompany each shipment of devices.

3.8.3 Radiograph and report retention. When specified, the manufacturer shall retain a set of the radiographs and a copy of the inspection report. These shall be retained for the period specified.

3.9 Examination and acceptance criteria.

3.9.1 Device construction. Acceptable devices shall be of the specified design and construction with regard to the characteristics discernible through radiographic examination. Devices that deviate significantly from the specified construction shall be rejected.

3.9.2 Individual device defects. The individual device examination shall include, but not be limited to, inspection for foreign particles, solder or weld "splash" build up of bonding material, proper shape and placement of lead wires or whiskers, and bond of lead or whisker to semiconductor element. Devices for which the radiograph reveals any of the following defects shall not be accepted.

3.9.2.1 Unacceptable construction. In the examination of devices, the following aspects shall be considered unacceptable construction and devices that exhibit any of the following defects shall be rejected:

a. Total contact area voids in excess of one-half of the total contact area.

b. A single void which traverses either the length or width of the semiconductor die and exceeds 10 percent of the total intended contact area.

(1) Voids: When radiographing devices, certain types of mounting do not give true representations of voids. When such devices are inspected, the mounting shall be noted on the inspection report (see figure 2076-1).

(2) Wires present, other than those connecting specific areas of the semiconductor die to the external leads.

(3) Angle between semiconductor die surface and edge less than 45°.

(4) Defective seal: Any device wherein the integral lid seal is not continuous or is reduced from its designed sealing width by more than 75 percent.

NOTE: Expulsion resulting from the final sealing operation is not considered extraneous material as long as it can be established that it is continuous, uniform, and attached to the parent material and does not exhibit a ball, splash, or tear-drop configuration.

(5) Inadequate clearance: Acceptable devices shall have adequate internal clearance to assure that the elements cannot contact one another or the case. No crossover of wires connected to different electrical elements shall be allowed. Depending upon the case type, devices shall be rejected for the following conditions:

(a) Flat pack and dual-in-line (see figure 2076-2).

1. Any lead wire that appears to touch or cross another lead wire or bond (Y plane only).

2. Any lead wire that deviates from a straight line from bond to external lead and appears to be within .002 inch (0.0504 mm) of another bond (Y plane only).

3. Lead wires that do not deviate from a straight line from bond to external lead and appear to touch another wire or bond (Y plane only).

4. Any lead wire that touches or is less than .002 inch (0.0504 mm) from the case or external lead to which it is not attached (X and Y plane).

5. Any bond that is less than .001 inch (0.0254 mm) (excluding bonds connected by a common conductor) from another bond (Y plane only).

6. Any wire making a straight line run (with no arc) from die bonding pad to package post.

(b) Round or "box" transistor type (see figure 2076-3).

1. Any lead wire that touches or is less than .002 inch (0.0504 mm) from the case or external lead to which it is not attached (X and Y plane).

2. Lead wires that sag below an imaginary plane across the top of the bond (X plane only).

3. Any lead wire that appears to touch or cross another lead wire or bond (Y plane only) if bonded to different electrical elements.

4. Any lead wire that deviates from a straight line from bond to external lead appears to touch or to be within .002 inch (0.0504 mm) of another wire or bond (Y plane only).

5. Any bond that is less than .001 inch (0.0254 mm) (excluding bonds connected by a common conductor) from another bond (Y plane only).

6. Any wire making a straight line run (with no arc) from die bonding pad to package post, unless specifically designed in this manner (e.g., clips, rigid connecting leads, or heavy power leads).

7. Any internal post that is bent more than 10° from the vertical (or intended design position) or is not uniform in length and construction or comes closer than one post diameter to another post.

8. Any post in a low profile case (such as a TO-46) which comes closer to the top of the case than 20 percent of the total inside dimension between the header and the top of the case. Any device in which the semiconductor element is vertical to the header, and comes closer than .002 inch (0.0504 mm) to the header or to any part of the case.

(c) Axial lead type (see figure 2076-4).

1. Whisker embedded within glass body wall.

2. Whisker tilted more than 5° in any direction from the device lead axis or deformed to the extent that it touches itself.

3. Either half of an S or C bend whisker that is compressed so that any dimension is reduced to less than 50 percent of its design value. On diodes with whiskers metallurgically bonded to the post and to the die, the whisker may be deformed to the extent that it touches itself if the minimum whisker clearance zone specified in figure 2076-4a is maintained for metal packages.

4. Whiskerless construction device with plug displacement distance more than one-fourth of the diameter of the plug with respect to the central axis of the device.

5. Semiconductor element mounting tilted more than 15E from normal to the main axis of the device.

6. Die hanging over edge of header or pedestal more than 20 percent of the die contact area by design.

7. Less than 75 percent of the semiconductor element base area is bonded to the mounting surface.

8. Voids in the welds which reduce the lead to plug connection by more than 25 percent of the total weld area.

9. Devices with package deformities such as body glass cracks, incomplete seals (e.g., voids, position of glass), die chip outs, and severe misalignment of S- and C-shaped whisker connections to die or post that exceed the limits of the applicable visual inspection requirements.

3.9.3 Encapsulated non-cavity assemblies of discrete devices. External to the individual devices, the encapsulating material shall be examined and rejected for the following defects.

3.9.3.1 Extraneous material. Extraneous matter of any shape with any dimension exceeding .020 inches (0.51 mm). Also, any two adjacent particles of such matter with total dimensions exceeding .030 inches (0.76 mm).

4. Summary. The following conditions shall be specified in the applicable detail specification:

a. Number of views, if other than indicated in 3.1.1 and 3.1.1.1.

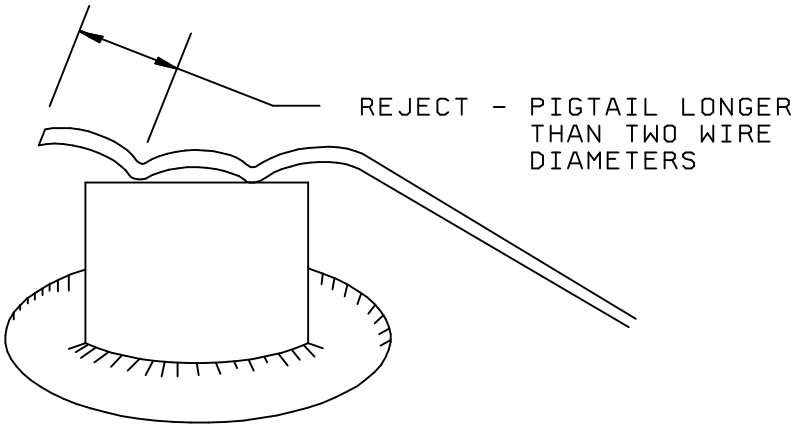
b. Radiograph submission, if applicable (see 3.8.2).

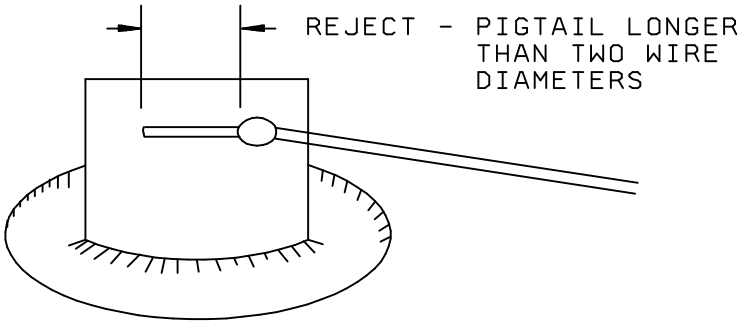
c. Marking, if other than indicated in 3.3 and marking of samples to indicate they have been radiographed, if required (see 3.3.3).

d. Sample defects and criteria for acceptance or rejection, if other than indicated in 3.9.

e. Radiograph and report retention, if applicable (see 3.8.3).

f. Test reports when required.





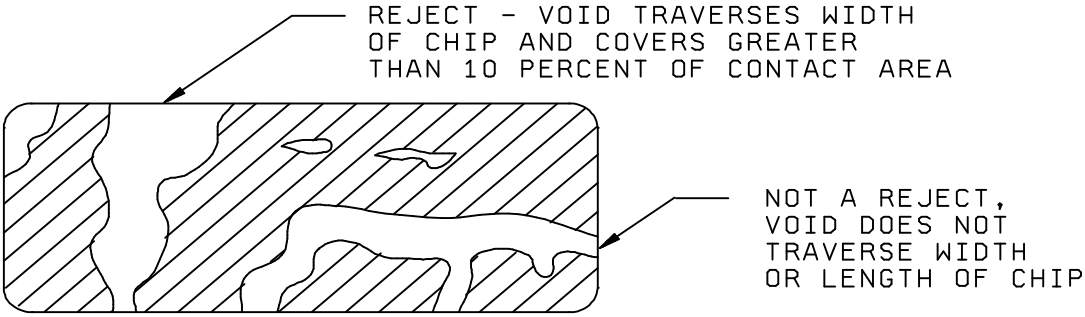


FIGURE 2076-1. Acceptable and unacceptable voids and excessive pigtails.

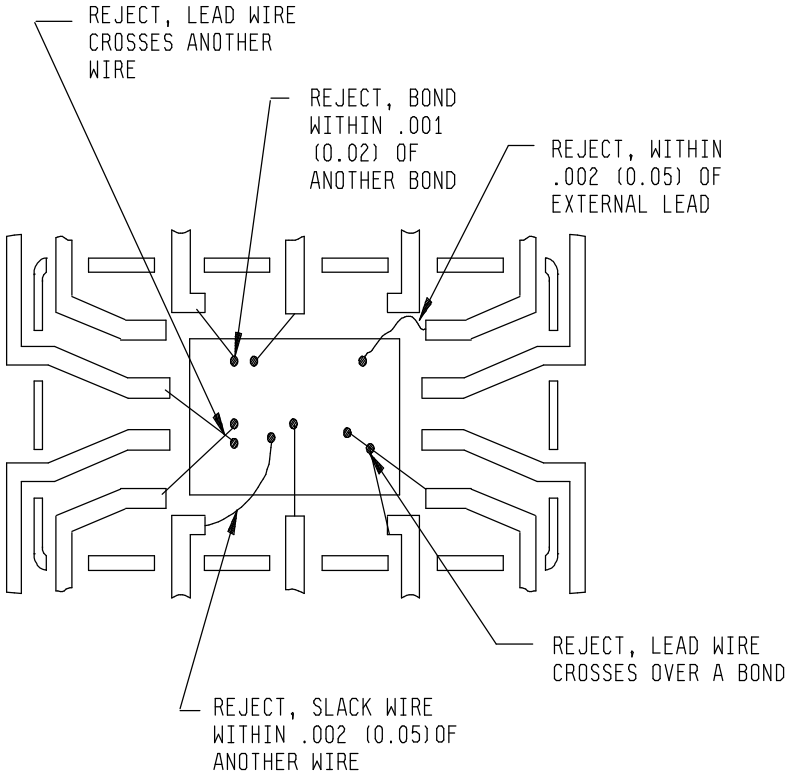


FIGURE 2076-2. Clearance in dual-in-line or flat pack type device.

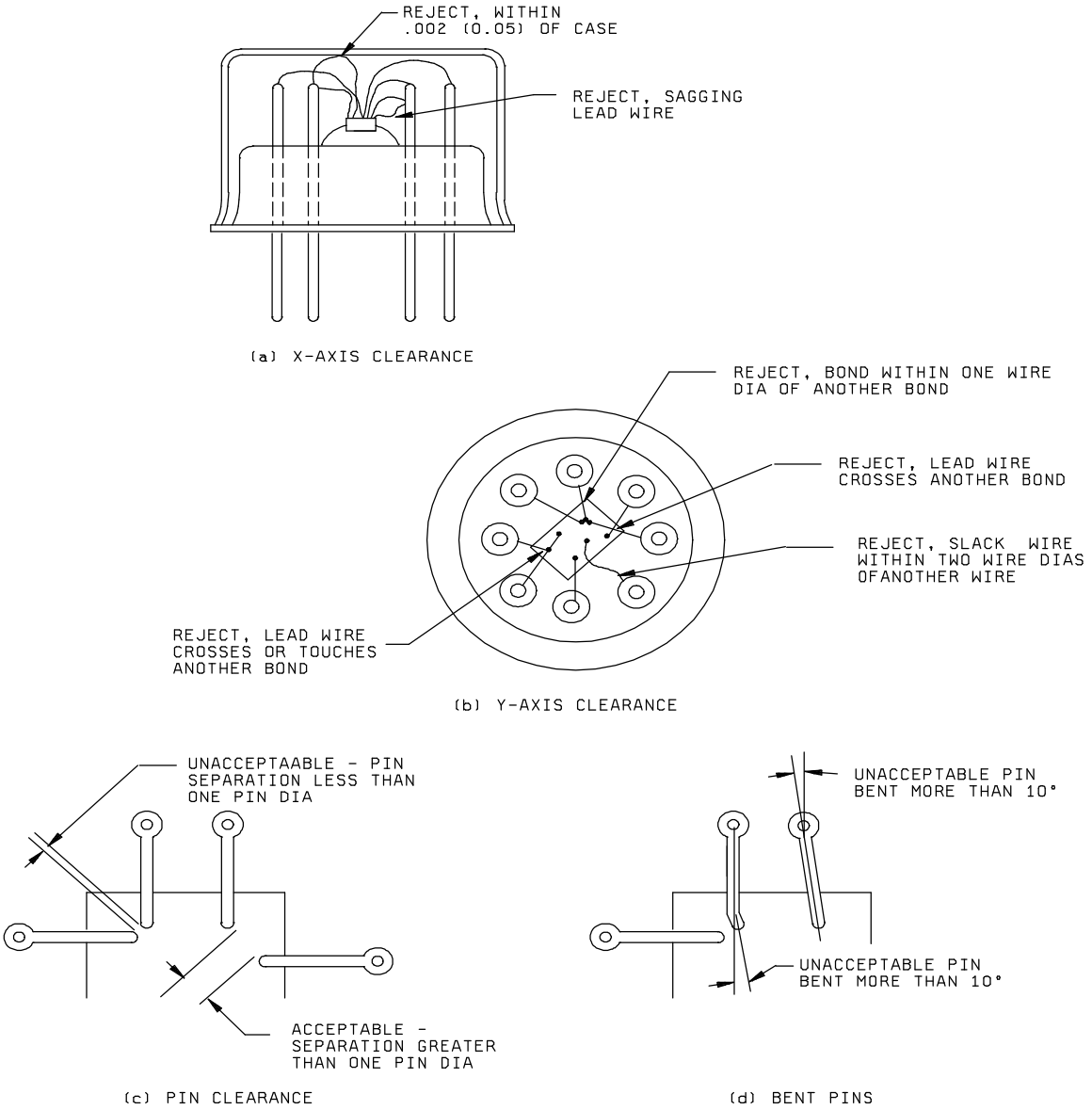


FIGURE 2076-3. Clearance in round or box transistor type device.

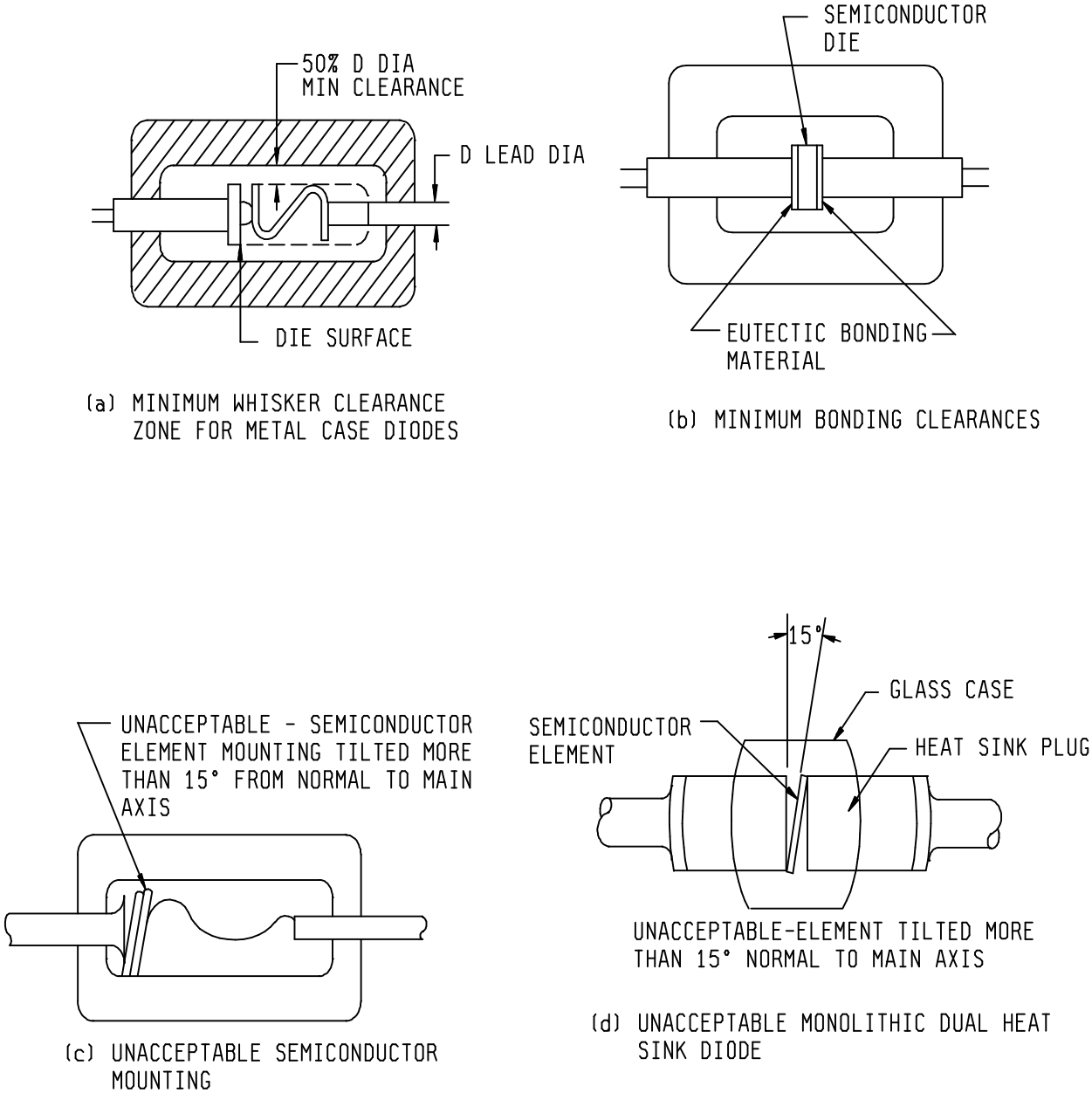


FIGURE 2076-4. Clearance in cylindrical axial lead type device.

METHOD 3105.1

MEASUREMENT METHOD FOR THERMAL RESISTANCE OF A BRIDGE RECTIFIER ASSEMBLY

1. Purpose. This method describes a means to cause current to flow alternately through the legs of a single-phase or three-phase bridge assembly under condition to make it feasible determines its effective thermal resistance. The bridge is operated under steady-state I_O conditions and the current in each leg is interrupted while readings are taken from which to calculate thermal resistance.

2. Definitions. The following symbols and terminology shall apply for the purposes of this test method:

a. V_F: The forward-biased junction voltage of the DUT used for junction temperature sensing. For bridge, this applies to individual legs (i.e., one ac to one dc terminal).

b. V_{F1}: The forward voltage at room temperature at I_{ref}.

c. V_{F2}: The forward voltage at I_{ref} and +100°C above that at V_{F1}.

d. V_{F2A}: The computed forward voltage at I_{ref} and at maximum rated T_J.

e. V_{F3}: The initial V_F value at I_{ref} before the application of heating power, with the device at rated case temperature.

f. V_{F4}: The final V_F value at I_{ref} after stabilization of temperatures due to the application of rated current at rated case temperature.

g.)V_F: The change in the TSP V_F, due to the application of heating power to the DUT in volts.

h. V_{FH}: The maximum forward voltage resulting from the application of I_O to the DUT.

i. I_O: The rated average current applied to the DUT.

j. I_{ref}: The measurement current used to forward-bias the temperature sensing diode junction for measurement of V_F.

k. TCVF: Voltage-temperature coefficient of V_F with respect to T_J at a fixed value of I_{ref} in V/°C.

l. T_J: The DUT junction temperature.

m.)T_J: The change in T_J caused by the application of I_O.

n. TSP: The temperature-sensitive parameter (V_F).

o. t_{F4}: Step trace time.

p. T_N: Reference case temperature for measuring V_N, when N = 1, 2, 3, or 4.

q. R_{thJX}: Thermal resistance from device junction to a defined reference point (e.g., lead or ambient) in units of °C/W.

r. R_{thJC}: Thermal resistance from device junction to a defined reference point on the outside surface of the case in units of °C/W.

3. Test circuit. The apparatus required for this test shall include the following, configured as shown on figures 3105-1 and 3105-2.

a. A source of 60 Hz, single or three phase sine wave (AC) capable of being adjusted to the desired value of I_O and able to supply the V_{FH} value required by the DUT. The current source should be able to maintain the desired current to within ±2 percent during the entire time needed for temperature stabilization and measurements.

b. A constant-current source to supply I_{REF} with sufficient compliance voltage range to turn on fully the junction of the diode leg being measured.

c. Anti-parallel fast recovery rectifier diodes with ratings exceeding I_O, to provide isolation of the high-current source from I_{REF} during commutation of I_O between legs.

d. A voltage measurement circuit capable of accurately making the V_F measurements within the available time interval (when the anti-parallel diodes are not conducting), with millivolt resolution.

4. Procedure. Refer to figures 3105-1 and 3105-2, test circuits for single- and three-phase bridges.

a. With S1 open, and DUT at +20°C to +30°C (temperature T_1), read V_{F1} of each leg at current I_{REF}. Elevate the device temperature to +100°C above temperature T_1 (temperature T_2). Allow the device to stabilize until the junction temperature is at T_2. Read V_{F2} of each leg at I_{REF} current. Compute the TCVF of each leg as follows:

$$TCVF = (V_{F1} - V_{F2}) / +100°C$$

Compute the expected V_{F2A} at T_J = maximum rated as follows:

$$V_{F2A} = V_{F1} - [(TCVF) \times (T_{Jmax} - T_1)]$$

Determine the average TCVF and the standard deviation of the TCVF from the readings on each leg. If the standard deviation is less than or equal to three percent of the average value of TCVF, TCVF may be used for all devices. If the standard deviation is greater than three percent of the average value of TCVF, then the individual values of TCVF shall be used in determining the performance of the bridge.

b. With the device held at T_3, at or below rated case temperature of I_O, close S1 and read V_{F3} for each leg.

c. After closing S1, adjust the power source, the load resistor, or both to obtain the maximum rated I_O (either I_{O1} or I_{O2}, depending on the rated T_C selected) and readjust the case temperature to the chosen rated value. Allow the device to achieve stable junction temperatures (see note 1).

d. Measure V_{F4} (see figure 3105-2) for each leg at the same reference current (±1 percent) as in steps a. and b. (The instrumentation used to measure V_{F4} must have sufficient resolution to read it within 2 mV or 2 percent).

NOTE: If V_{F3} for the leg is greater than V_{F2}, T_J is less than T_{Jmax}.

e. Measure V_{FH} for each leg.

f. Compute thermal resistance as follows:

(1) Compute $\Delta V_F = V_{F4} - V_{F3}$ for each leg.

(2) Compute $\Delta T_J = \frac{\Delta V_F}{TCVF}$ 1/

(3) Compute R_{thJC} of the full bridge: $R_{thJC} = \frac{\Delta T_{JC}}{I_o \times 2V_{FH}}$

Where: ΔT_J is the average of all legs. V_{FH} is the average of all legs and I_O is the rectified output current of the full bridge. 2/ 3/ 4/

5. Test condition to be specified.

I_O _____

T_C _____

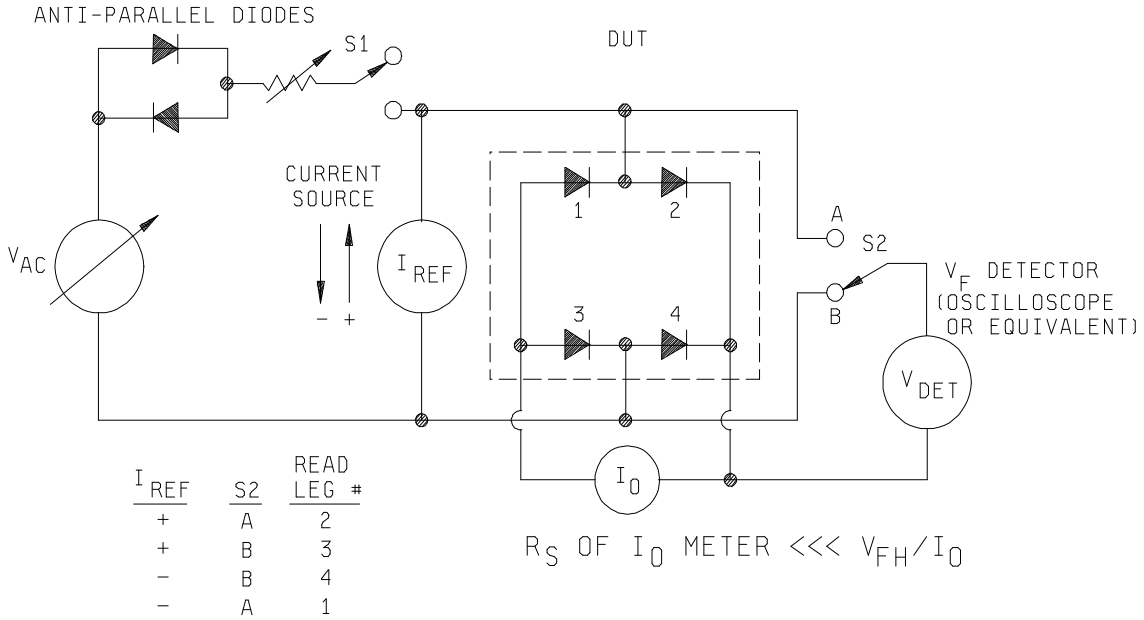
I_{REF} _____

Frequency _____
(if other than 60 Hz)

6. Characteristics to be determined:

Steady state thermal resistance. Unless otherwise specified, junction to care: _____°C/W.

1/ If, under power, the case is held to T_4, slightly above T_3, a corrected ΔT_J ($\Delta T_{J(corr)} = \Delta T_{JC} - (T_4 - T_3)$) should be used for step f(2).
2/ Step f(3) gives R_{th} for the bridge. The average per-leg R_{th} for a single-phase bridge is four times the value; six times for a three-phase bridge (see 3/).
3/ If desired, R_{th} of individual legs may be computed from the individual values of ΔT_{JC} and V_{FH}.
4/ The power dissipated $I_O \times 2V_{FH}$ is a reasonable approximation.

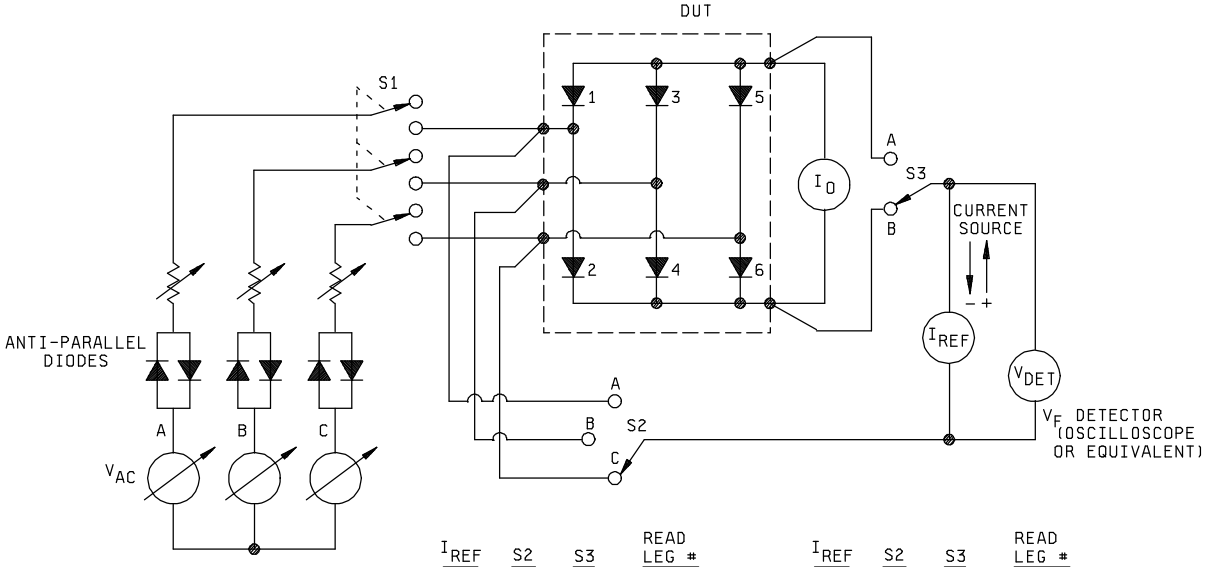


I_{REF}	S2	READ LEG #
+	A	2
+	B	3
−	B	4
−	A	1

NOTES:

1. All voltage measurements shall be made using leads Kelvin-connected directly to the bridge terminals.
2. V_{AC} is adjusted so that the V_{F4} step (t_{F4}) shown on figure 3105-3 is 100 μs ±50 μs and is clearly defined. A typical V_{AC} might be 10 volts peak. Bridges with parasitic inductive components must adjust V_{AC} so that after the inductive ringing settles, the V_{F4} step on figure 3105-3 (t_{F4}) is 100 μs ±50 μs.

FIGURE 3105-1. Single phase bridge.

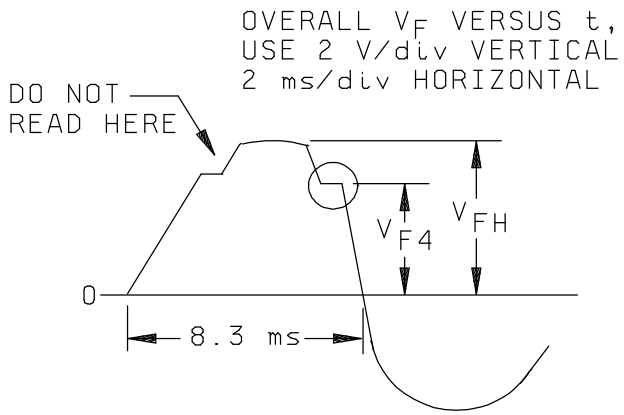


I_{REF}	S2	S3	READ LEG #	I_{REF}	S2	S3	READ LEG #
+	A	A	1	−	A	B	2
+	B	A	3	−	B	B	4
+	C	A	5	−	C	B	6

NOTES:

1. All voltage measurements shall be made using leads Kelvin-connected directly to the bridge terminals.
2. V_{AC} is adjusted so that the V_{F4} step (t_{F4}) shown on figure 3105-3 is 100 μs ±50 μs and is clearly defined. A typical V_{AC} might be 10 volts peak. Bridges with parasitic inductive components must adjust V_{AC} so that after the inductive ringing settles, the V_{F4} step on figure 3105-3 (t_{F4}) is 100 μs ±50 μs.

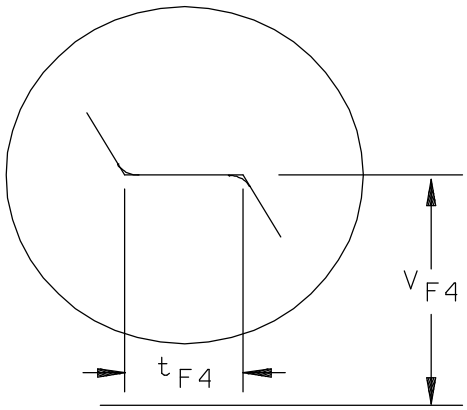
FIGURE 3105-2. Three phase bridge.



NOTE: V_{F4} "step trace" is provided when anti-parallel diodes in circuit briefly commutate off (the ac current passes through zero during each cooling cycle of individual bridge legs under ac test conditions.)

OSCILLOSCOPE DISPLAYS

EXPANDED AND CHOPPED
V_F VERSUS t. USE 5 OR
10 mV/div VERTICAL,
20 OR 50 us/div HORIZONTAL



NOTES:

1. Polarity shown applies when I_{REF} is positive. The trace in inverted when I_{REF} is negative.
2. V_{AC} is adjusted so that the V_{F4} step (t_{F4}) shown on figure 3105-3 is 100 μs ±50 μs and is clearly defined. A typical V_{AC} might be 10 volts peak. Bridges with parasitic inductive components must adjust V_{AC} so that after the inductive ringing settles, the V_{F4} step on figure 3105-3 (t_{F4}) is 100 μs ±50 μs.

FIGURE 3105-3. Oscilloscope displays.

METHOD 4026.3

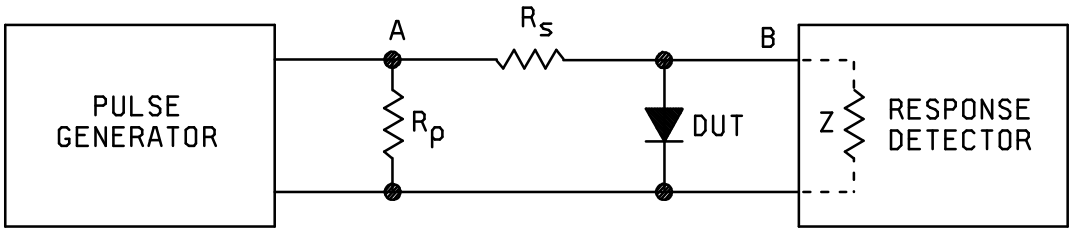
FORWARD RECOVERY VOLTAGE AND TIME

1. Purpose. This test is intended to measure the forward voltage and recovery time of the device. A device reveals an excessive transient forward voltage when it is switched rapidly into the forward conductance region. The amplitude and time duration of this voltage peak can be measured by observing the voltage waveform across the device when a flat-top pulse of the specified amplitude, rise time, pulse width and frequency are applied to the device.

2. Test circuit. See figure 4026-1.

a. The forward transient test circuit shown on figure 4026-1 is used in conjunction with a pulse generator and an output sensing device. Care should be taken to minimize lead length where lead inductance might cause ringing in the test circuit.

b. The value of resistor R_p shall be chosen to optimize the impedance match between pulse generator and test circuit, thereby minimizing the ringing in the test circuit.



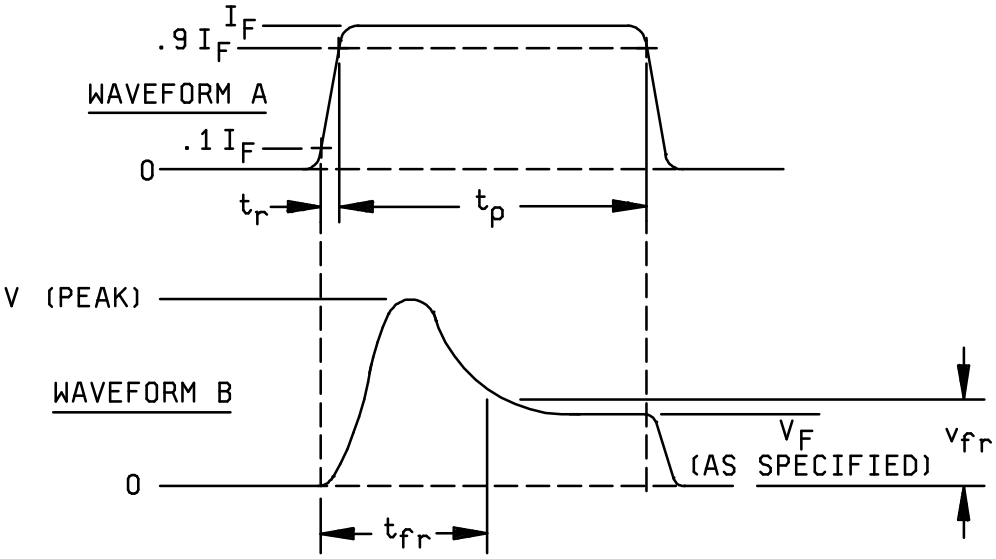


FIGURE 4026-1. Test circuit for forward recovery voltage and time.

3. Procedure. Test shall be performed using the following:

3.1 Conditions:

a. Pulse input A:

(1) I_F amplitude: As specified.

(2) Rise time = 10 ns or as specified.

(3) Pulse width $t_1 \geq$ 10X specified response time.

(4) Generator resistance $R_S \geq$ 20 RF ($R_F = V_F/I_F$ at specified IF).

(5) Pulse frequency shall be such that a reduction in frequency shall result in no change in forward recovery characteristics.

b. Response detector input impedance, $Z \geq 100\ R_F$.

4. Summary. The following conditions shall be specified in the detail specification:

a. I_F of input waveform A (see 3.1).

b. Rise time if other than 10 nanoseconds (see 3.1).

c. Forward recovery voltage $V_{(peak)}$chosen to terminate the forward recovery time measurement (see figure 4026-1).

d. The following measurements should be made:

Forward recovery time (t_{fr}) (measured from the time forward voltage becomes positive to the time that forward voltage recovers to a specified v_{fr}) (see figure 4026-1).

e. The peak forward voltage $V_{(peak)}$ (see figure 4026-1). This symbol is interchangeable with V_{FM}.

METHOD 4031.4

REVERSE RECOVERY CHARACTERISTICS

1. Purpose. The purpose of this test is to measure the reverse recovery time and other specified recovery characteristics related to signal, switching, and rectifier diodes by observing the reverse transient current versus time when switching from a specified forward current to a reverse biased state in a specified manner.

2. General guide for selecting appropriate condition. Four conditions are given to include recommended practice for the range of diodes considered. A general guide for selecting the appropriate condition letter is:

a. Signal diodes with reverse recovery time less than 6 ns.

b. Low to medium current rectifiers with maximum specified recovery times of 50 to 3,000 ns.

c. High current rectifiers with maximum specified recovery times of 350 ns or greater.

d. Ultra-fast rectifiers, particularly on new specifications.

Further, detailed guidance is given under each condition below.

3. Test condition A. This condition is particularly relevant to low-current, signal diodes faster than 6 ns and tested at 10 mA. However, it is practicable for measurements up to 20 ns and 100 mA.

3.1 Circuit notes for condition A.

a. Rise time of the reverse voltage pulse across a noninductive calibration resistor in place of the DUT shall be less than 20 percent of the recovery time of the DUT, for greatest accuracy.

b. Oscilloscope rise time shall be less than 20 percent of device recovery time, for greatest accuracy.

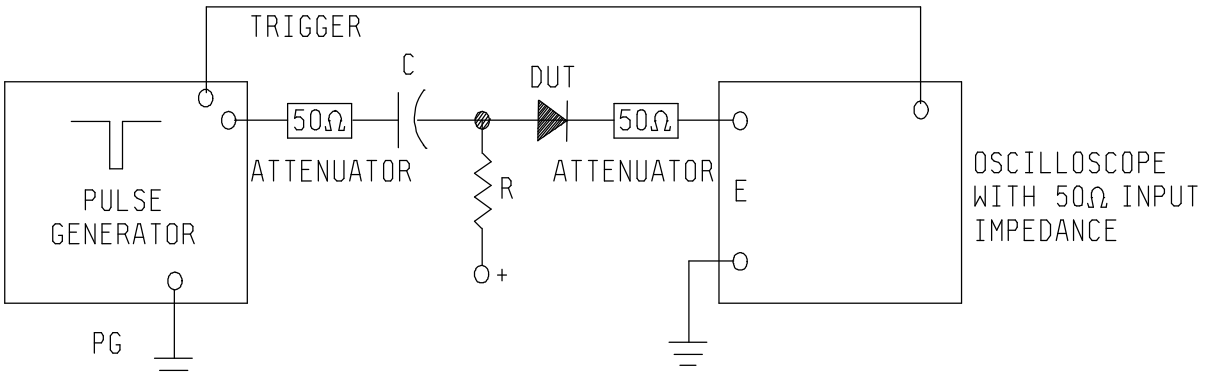
c. Proper coaxial networks and terminations shall be employed to ensure against error-producing pulse reflections.

d. $R > 10\ R_L$.

e. Unless otherwise specified, $R_L = Z_{PG} + Z_{SCOPE} = 100\ \Omega$.

f. C > 10 PW) R_L.

g. PW > 2 x maximum specified t_{rr} (see figure 4031-1.)



NOTE: The test circuit shall comply with the test conditions as stated under 2.1.
PW = Pulse width of reverse voltage pulse (see figure 4031-2).
R_L = Load resistance.
C = Coupling capacitance.

FIGURE 4031-1. Test circuit for condition A.

3.2 Procedure for condition A. The specified forward current shall be adjusted by resistor R and the + supply. Voltage E, developed across the 50 ohm oscilloscope input impedance shall be measured. Specified forward current shall be calculated by the expression $I_F = E/50$. The time duration of I_F shall be at least 10 times the device recovery time. The oscilloscope trace deflection above zero reference shall be adjusted by the oscilloscope vertical sensitivity to produce an amplitude of 2 cm minimum vertical deflection. Adjustment of the reverse transient current (I_{RM}) shall be made by varying the pulse generator output, observing the voltage E across the 50 ohm oscilloscope input impedance, and calculating I_{RM} by the expression I = E/50. When reverse bias voltage V_R is specified, and I_{RM} is not, the DUT shall be replaced with a shorting bar and I_{RM} shall be calculated by the expression $V_R/50$ (see figure 4031-2.)

3.3 Summary for condition A. The following conditions shall be specified in the detail specification:

a. Forward current, I_F.

b. Reverse current I_{RM} (preferred), or reverse voltage (optional alternative).

c. Load resistance, if other than 100 Ω (this is the sum of Z_{PG} and Z_{SCOPE}).

d. Ambient temperature in °C.

e. Generator impedance, if other than 50 Ω.

f. Recovery current measuring point, $i_{R(REC)}$, if different from 10 percent of I_{RM}.

The following measurement shall be made: t_{rr} (see figure 4031-2).

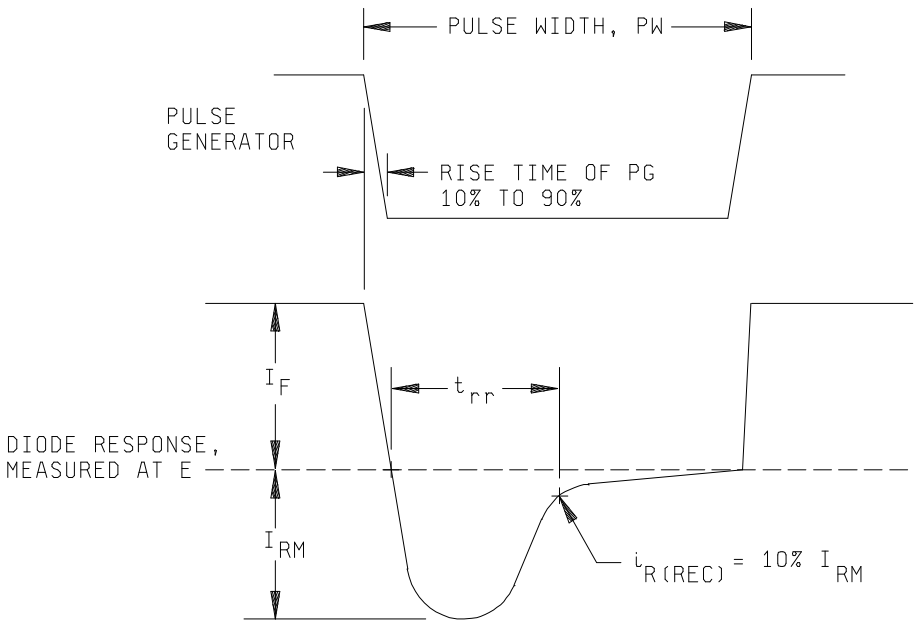


FIGURE 4031-2. Response pulse waveforms for condition A.

4. Test condition B. (See suggested conditions below (e.g., B1, B2).) This condition is particularly relevant to medium current (axial and similar) types of standard and fast rectifiers with maximum specified recovery times between 50 and 3,000 ns that measured at peak forward currents greater than 100 mA and less than or equal to 1.0 ampere. It is readily adapted to lower test currents. This test is also appropriate for devices with recovery times less than 50 ns that are measured at peak forward currents of 1A or less; below 25 ns, or at higher current, particular care must be used to achieve low loop inductance and low circuit rise times to achieve acceptable repeatability.

This condition differs from condition D in that the reverse current (I_{RM}) is limited by the test circuit, not by the DUT.

TABLE 4031-I. Test condition B.

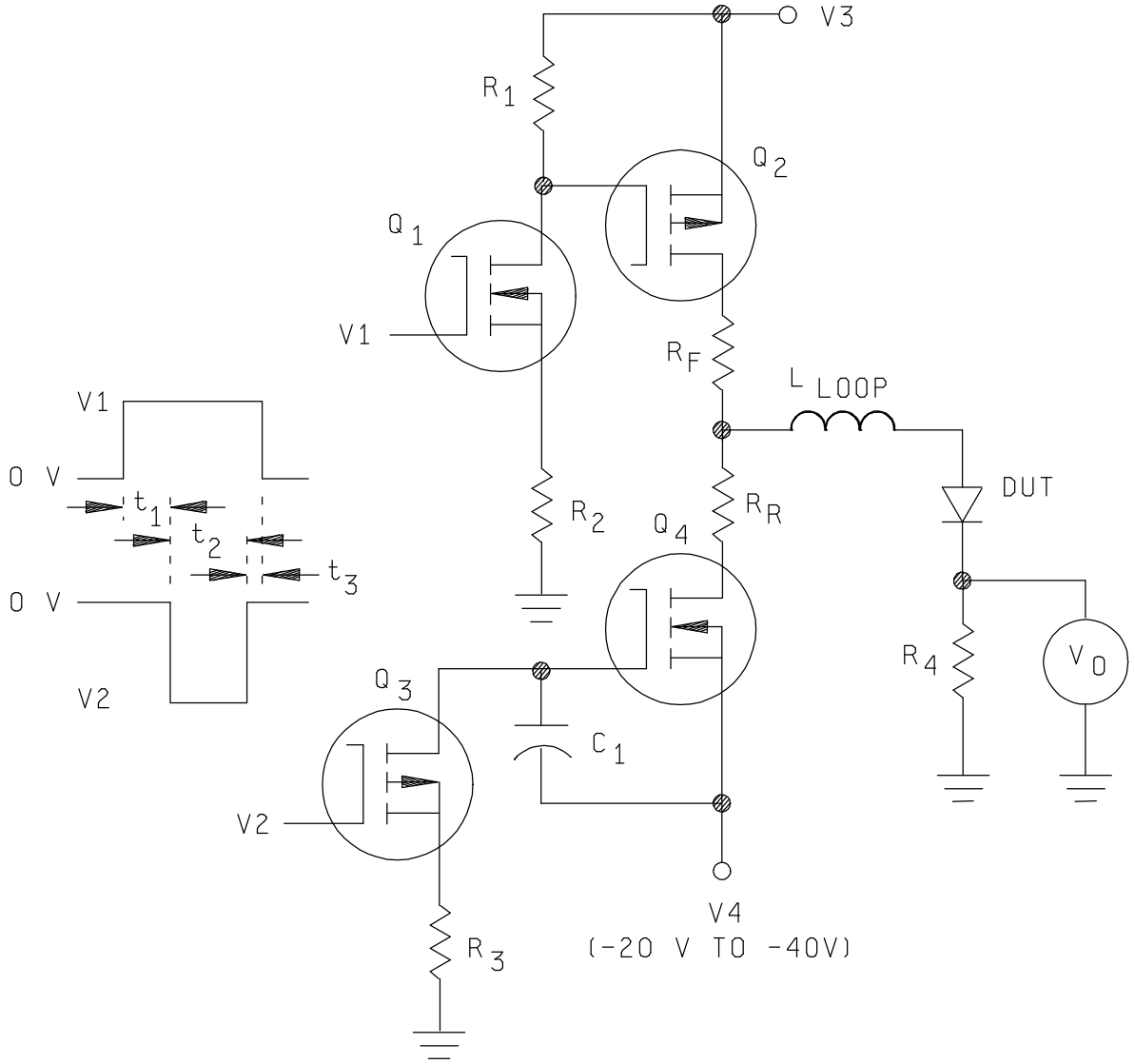
Designation (condition)		B1	B2	B3	B4	B5
Test current, (amperes) (see figure 40311-4)	I_F	0.5	0.5	1.0	1.0	0.01
	I_{RM}	1.0	0.5	1.0	1.0	0.01
	$i_{R(REC)}$	0.25	0.1	0.5	0.1	0.005
Circuit resistor 1/ (ohms)	R_F	33	33	50	50	1,200
	R_R	9	9	15	15	200
	R_4	1.00	1.00	1.00	1.00	10.0

1/ Preferred nominal resistance values are shown; modification of R_F and R_R may be needed to achieve the rise time of 4.1a and the I_{RM} specified.

4.1 Circuit notes for condition B. The timing and test circuit of figure 4031-3A is a guide to that needed. An equivalent circuit may be used. Figure 4031-3B shows a suggested configuration for R_4. Duty factor shall be 5 percent maximum.

a. The rise time of the reverse voltage pulse across a noninductive calibration resistor in place of DUT shall be less than 20 percent of the recovery time of the DUT.

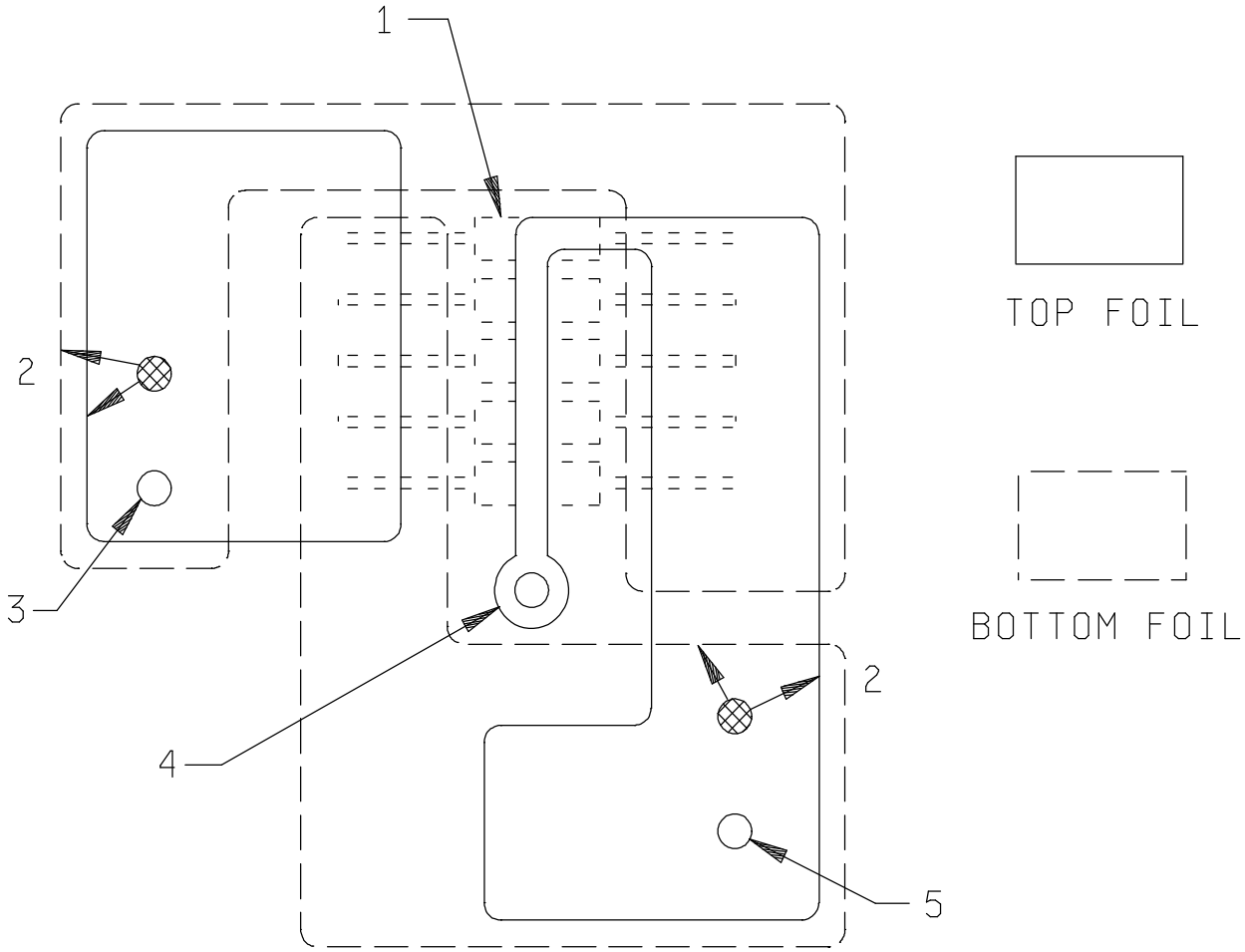
b. The oscilloscope rise time shall be less than 50 percent of the pulse generator rise time.



V_3 and R_F control forward current I_F.
V_4 and R_R control reverse current I_{RM}.
$t_{rr(max)}$ is the longest to be measured.
$t_{rr(min)}$ is the shortest expected.

$t_1 > 5\ t_{rr(max)}$.
$t_2 > t_{rr}$.
$t_3 > 0$.
$L_1/R_4 < t_{rr(min)}/10$.
(L_1 is the self inductance of R_4)

FIGURE 4031-3A. Test circuit for condition B.



NOTES:

1. Resistor assembly R_4 consists of 10 resistors (1 Ω, .25 W metal film), 5 on top and 5 on the bottom foils. The center of resistor bodies are not shown, and leads are shown dotted so that conducting foils may be more clearly shown. Bottom resistor current flow L to R (-->) is opposite to top current flow R to L (<--), providing magnetic field cancellation. Sense lead to the center conductor of the probe jack exits at right angle to resistor axes and is located between the top and bottom resistor layers.
2. Cross hatched circular areas show the connections between those top and bottom foil regions indicated by arrows.
3. To ground of circuit and probe.
4. To center conductor of miniature probe jack.
5. To cathode of DUT.

FIGURE 4031-3B. Suggested board layout for low L_3/R_4 for condition B.

4.2 Procedure for condition B. Specified forward current (I_F) shall be adjusted by varying positive voltage, V_3. Reverse current (I_{RM}) shall be controlled by varying the negative voltage, V_4 (see figure 4031-4). With the DUT in place the circuit must be capable of higher than specified I_{RM}; the circuit, and not the diode, must limit I_{RM}.

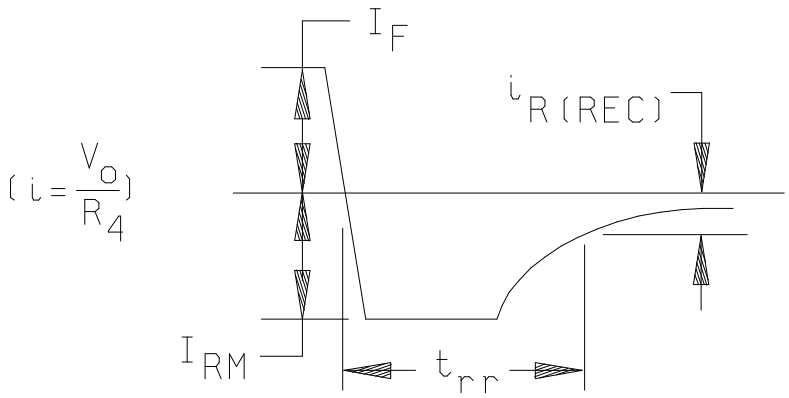


FIGURE 4031-4. Current through DUT (condition B).

4.3 Summary for condition B. The following conditions shall be specified in the detail specification:

a. Test condition (e.g., B1, B2) (see 3.) If not in table 4031-I, specify c, d, and e.

b. Ambient temperature, if other than +25°C.

c. Forward current, I_F.

d. Reverse current, I_{RM}.

e. Load resistances R_F and R_R.

f. Recovery measuring point, $i_{R(REC)}$.

-----> NOTE: Specify c through f only if not a condition designation in table 4031-1.

The following measurement shall be made: t_{rr} (see figure 4031-4).

5. Test condition C. This test is intended for high current rectifiers with reverse recovery times equal to or greater than 350 ns and tested with peak forward currents equal to or greater than 10 amperes.

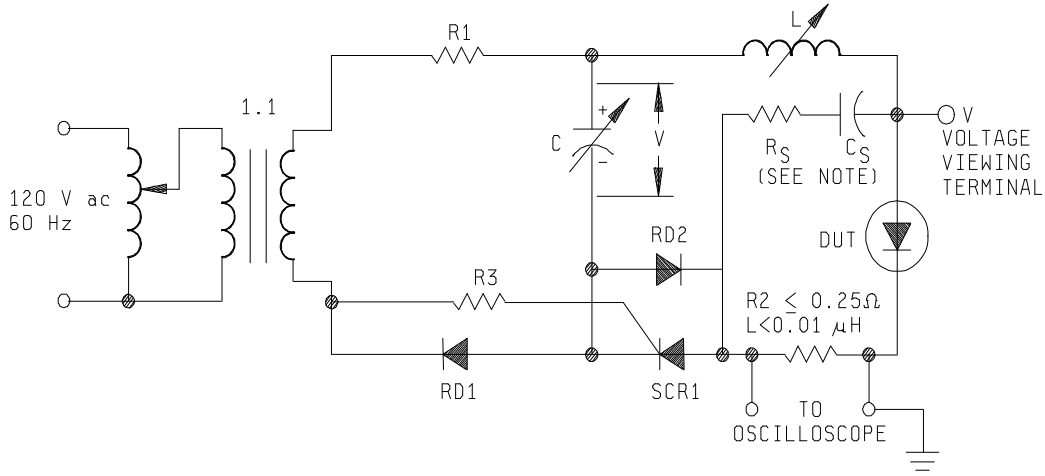


FIGURE 4031-5. Circuit for measuring reverse recovery characteristics (condition C).

NOTE: R_S and C_S are snubber components, when their use is specified

5.1 Circuit notes for condition C

a. The circuit is designed to simulate the commutation duty encountered in power rectifier diode circuits while also keeping average power dissipation low to minimize the need for thermal management.

b. The resistance of the C.L. and DUT loop (R_2 and parasitics) is small, e.g., $2\Pi\sqrt{L/C}$ much greater than R so the test current will essentially be sinusoidal, possessing a width of $\sqrt{C}$, a di/dt of V/L and a peak value of $\Pi\sqrt{L/C}$. The peak voltage across the capacitor shall be as small as practicable to achieve the desired test conditions. The effects of reverse voltage magnitude on the test device recovery characteristics are neglected.

c. The minimum forward current pulse time (t_p) shall be at least five times the recovery time (t_{rr}) of the DUT so that the di/dt will be linear and of the same value before and after current reversal.

d. The oscilloscope rise time shall be less than 1/5th of t_a or t_b (see figure 4031-6), whichever is less.

e. The inductance of the current viewing resistor shall be extremely low, e.g., 0.01 microhenry. Abrupt recovery rectifiers (figure 4031-6) can cause current oscillations which may be reduced by using a lower inductance current viewing resistor and by properly terminating the oscilloscope cable. A current transformer 1/ with suitable rise time may be substituted for the current viewing resistor. Rectifier diode RD2 provides a very low inductance path around SCR1 if the reverse recovery time of SCR1 is shorter than that of the DUT. An external SCR triggering source may be required to achieve stable triggering.

f. A slight oscillation may appear on the waveform following device recovery. This may be reduced by reducing the current viewing resistor's inductance, or properly terminating the viewing cable. The oscillation, however, does not affect the test results.

g. D_2 and its circuit branch should provide a very low inductance path around the SCR if the reverse recovery time of the SCR is shorter than that of the DUT.

h. R_3 must be sufficiently large such that the SCR triggers only after the capacitor, C, has had ample time to charge to its desired value. If stable triggering or ample charging is a problem, a momentary pushbutton switch may be inserted in line with R_3 to provide triggering. A pulse transformer technique is also acceptable in the triggering circuit.

5.2 Procedure for condition C. C, L, and V are adjusted to obtain the specified test current di/dt and magnitude, I_{FM}. The recovery time for rectifier diodes is defined as $t_{rr} = t_a + t_b$ (see figure 4031-6) t_a is measured from the instant of current reversal to the instant that current reaches its peak reverse value $I_{RM(REC)}$ and t_b is measured from $I_{RM(REC)}$ to the instant the straight line connecting $I_{RM(REC)}$ and 0.25 $I_{RM(REC)}$ intercepts the zero current axis. The recovery time for devices with abrupt recovery characteristics is defined in the same manner except t_b is measured from $I_{RM(REC)}$ to the instant the test current waveform intercepts the zero current axis, if applicable.

1/ Pearson Electronics, Inc. or equivalent types.

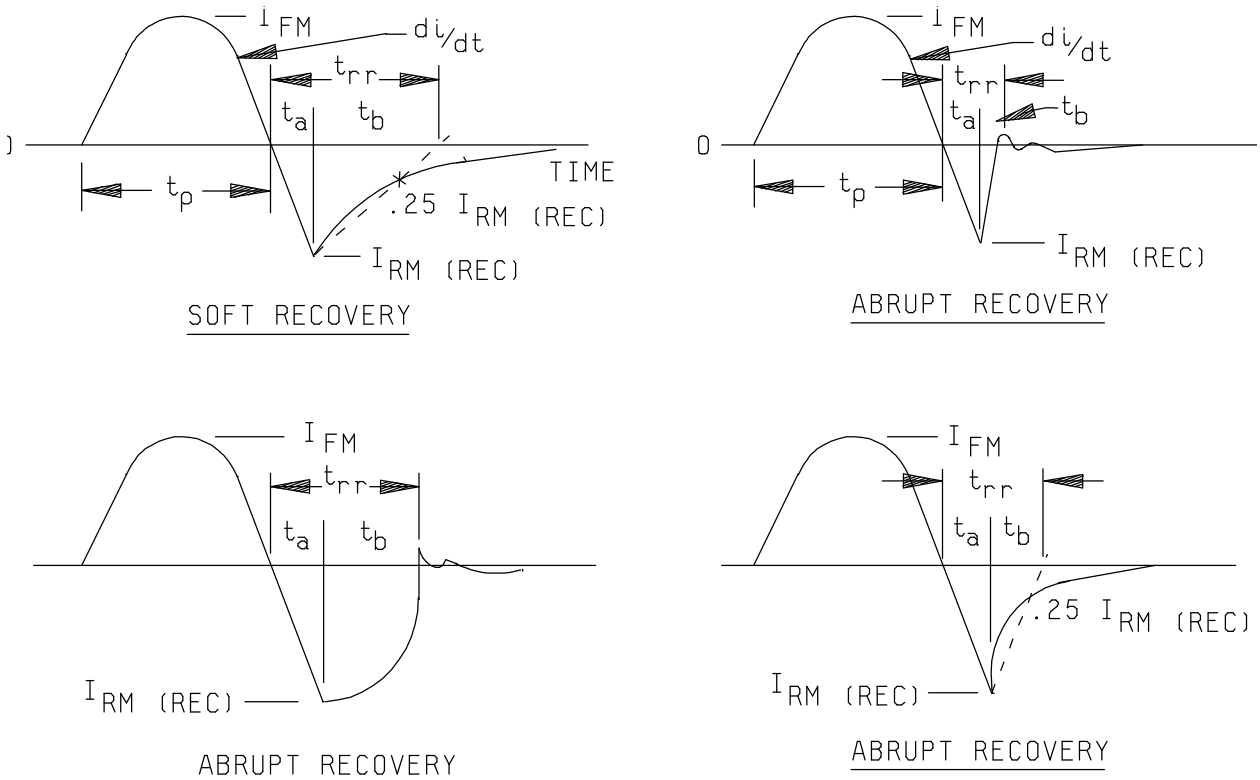


FIGURE 4031-6. Test current waveforms for various types of rectifier diodes under test in the circuit for measuring reverse recovery characteristics.

5.3 Summary for condition C.

a. The following conditions shall be specified in the detail specification:

(1) Case temperature in °C.

(2) Test repetition rate, in Hz.

(3) Peak forward current, I_{FM}, in amperes.

(4) Rate of decrease of forward current, di/dt, in A/μs.

(5) Minimum test current pulse width, tp, in microseconds. (Duty cycle shall be ≤ one percent).

b. The following characteristics shall be specified for measurement in the detail specification as required:

(1) Reverse recovery time (defined as $t_{rr} = t_a + t_b$), t_a, t_b.

(2) Reverse recovery current, $I_{RM(REC)}$, in amperes.

6. Test condition D. (See suggested conditions (e.g., D1, D2, D3) in table 4031-II.) This condition is intended for ultra-fast medium current rectifiers (axial and case mount, or equivalent styles) measured at $I_F \geq 1A$ and with reverse recovery time ≤ 100 ns. With good engineering practice, condition D can adequately measure t_{rr} down to about 10 ns; it can also utilize I_f up to at least 10 A.

TABLE 4031-II. Test condition D.

Device ratings		Designation (condition)	Values for testing	
I_O or I_F (AV) (A)	t_{rr} (ns)		I_F (A)	di/dt (μ/s)
1 to 4	> 65 to 100	D1	2	100
to 20	> 65 to 1.00	D2	6	100
over 20	> 65 to 1.00	D3	10	100
1 to 4	≤ 65	D4	2	200
to 20	≤ 65	D5	6	200
over 20 1/	≤ 65	D6	10	200

1/ For devices with substantially higher rated current it is desirable to use test conditions for I_F close to rated current, and higher values of di/dt.

6.1 Test circuit. Refer to figures 4031-7 and 4031-8 for timing and circuit details. Equivalent circuits may be used. The forward current generator consisting of Q_1, Q_2, R_1, and R_2 may be replaced with any functionally equivalent circuit. Likewise, the current-ramp generator consisting of Q_3, Q_4, R_3, and C_1. The duty factor shall be ≤ 5 percent.

a. This method presumes that good engineering practice will be employed in the construction of the test circuit, e.g., short leads, good ground plane, minimum inductance of the measuring loop and minimum self-inductance (L_1) of the current sampling resistor (R_4). Also, appropriate high speed generators and instruments must be used.

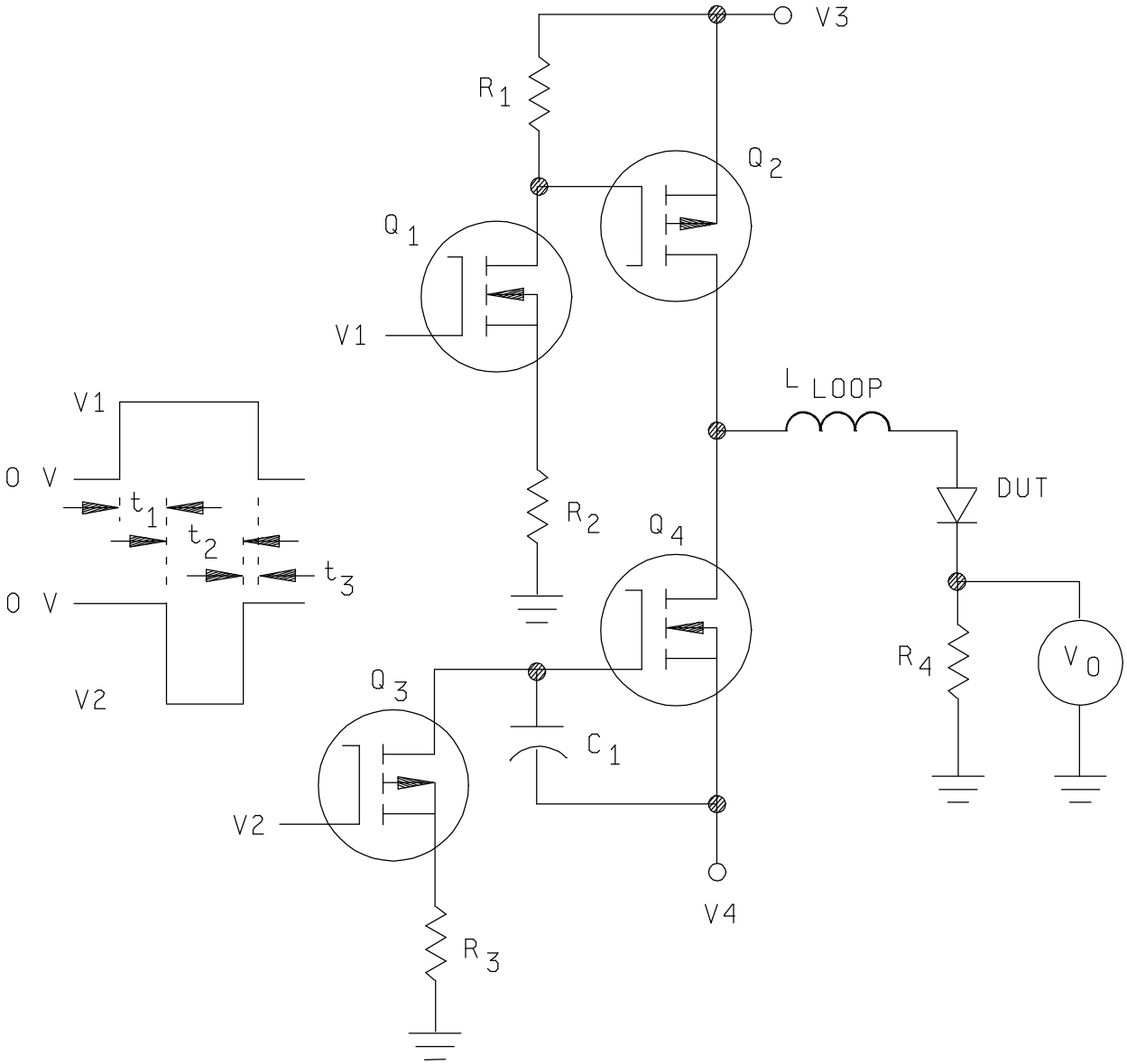
b. The measuring-loop inductance (L_{LOOP}, see figure 4031-7) represents the net effect of all inductive elements, whether lumped or distributed, e.g., bonding wires, test fixture, circuit board foil, inductance of energy storage capacitors. The value of L_{LOOP} should be 100 nH or less. The reason for controlling this circuit parameter is that it, combined with diode characteristics including C_T, determines the value of t_b.

c. The turn-off reverse-voltage overshoot shall not be allowed to exceed the device rated breakdown voltage. Ringing and overshoot may become a problem with $R_{LOOP} < 2\sqrt{(L/C)}$; where $L = L_{LOOP}$. That is another reason for minimizing L_{LOOP}.

d. Regarding breakdown voltage, $-V_4$ should be kept as low as practicable, especially when test low voltage devices. A value of approximately 30 volts is recommended.

e. The time constant of the self-inductance of the current-sample resistor R_4 (see figure 4031-8) must be kept low relative to t_a because the observed values of t_a and I_{RM} increase with increasing self-inductance. Since the value of R_4 is not specified, the recommended maximum inductance is expressed as a time constant (L_1/R_4) with a maximum value of t_a (minimum)/10, where t_a (minimum) is the lowest t_a value expected. This ratio was chosen as a practical compromise and would yield an observed t_a which is 10 percent high ($\hat{I}t_a = L_1/R_4$). The I_{RM} error is a function of the L_1/R_4 time constant and di/dt. For a di/dt of 100 A/μs the observed I_{RM} would also be 10 percent high. $\Delta I_{RM} = L_1/R_4$ di/dt.

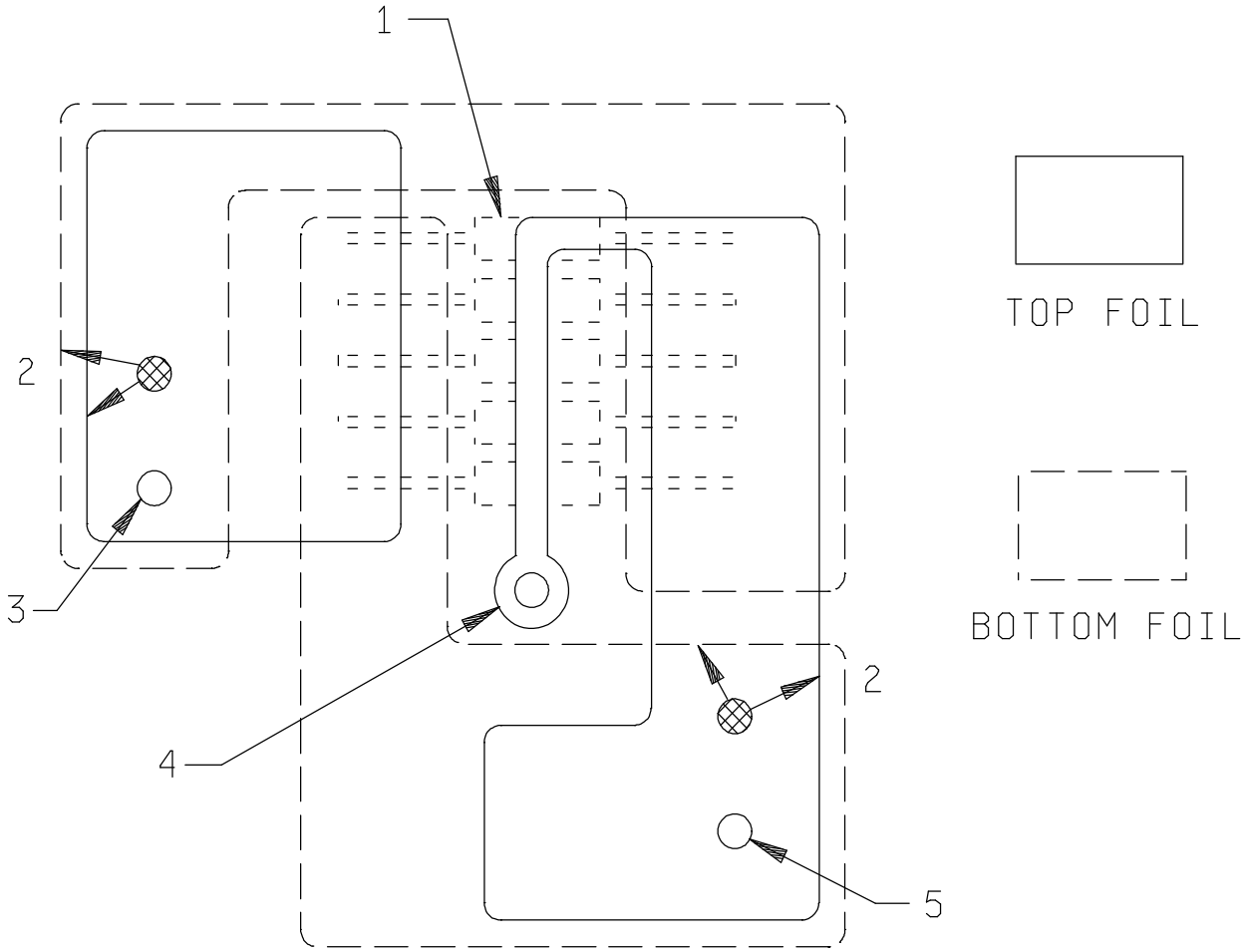
f. The di/dt of 100 A/μs was chosen so as to provide reasonably high signal levels and still not introduce the large I_{RM} errors caused by higher di/dt. Higher values of di/dt, without large errors, can be achieved with lower L_1/R_4.



V_1 amplitude controls forward current (I_F).
V_2 amplitude controls di/dt.
$t_{a(max)}$ is the longest t_a to be measured.
$t_{a(min)}$ is the shortest t_a to be measured.

$t_1 > 5\ t_{a(max)}$.
$t_2 > t_{rr}$.
$t_3 > 0$.
$L_1/R_4 < t_{a(min)}/10$.
L_1 is the self inductance of R_4.

FIGURE 4031-7. t_{rr} test circuit for condition D.



NOTES:

1. Resistor assembly R_r is made from 10 resistors (1 Ω, .25 W metal film), 5 on top and 5 on the bottom foils. The center of resistor bodies are not shown, and leads are shown dotted so that conducting foils may be more clearly shown. Bottom resistor current flow L or R (-->) is opposite to top resistor current flow R to L (<--), providing magnetic field cancellation. Sense lead to the center conductor of the probe jack exits at right angle to resistor axes and is located between the top and bottom resistor layers.
2. Crosses hatched circular areas show the connections between those top and bottom foil regions indicated by arrows.
3. To ground of circuit and probe.
4. To center conductor of miniature probe jack.
5. To cathode of DUT.

FIGURE 4031-8. Suggest board layout for low L_1/R_4 for condition D.

6.2 Procedure for condition D. Adjust V_1 for the specified forward current, I_F. Adjust $-V_2$ for the specified di/dt (see figures 4031-7 and 4031-9).

6.3 Summary for condition D.

a. The following conditions shall be specified:

(1) Designation (condition, see table 4031-II). If another is desired, 4 and 5 must be specified. If another is desired, d and e must be specified.

(2) $-V_4$, reverse ramp power supply voltage.

(3) T_C, case temperature, if other than +25°C.

(4) I_F, .25 (minimum) of the continuous rated current is the suggested alternative (see table 4031-II).

(5) di/dt, 100 A/µs is the suggested alternative (see table 4031-II).

b. The following characteristics shall be specified for measurement:

(1) Reverse recovery time, t_{rr} (see figure 4031-9).

(2) $I_{RM(REC)}$ (see figure 4031-9)

NOTE: An additional measurement, t_a may be made if desired to compute $t_b = t_{rr} - t_a$, and the recovery softness factor, RSF = t_b/t_a.

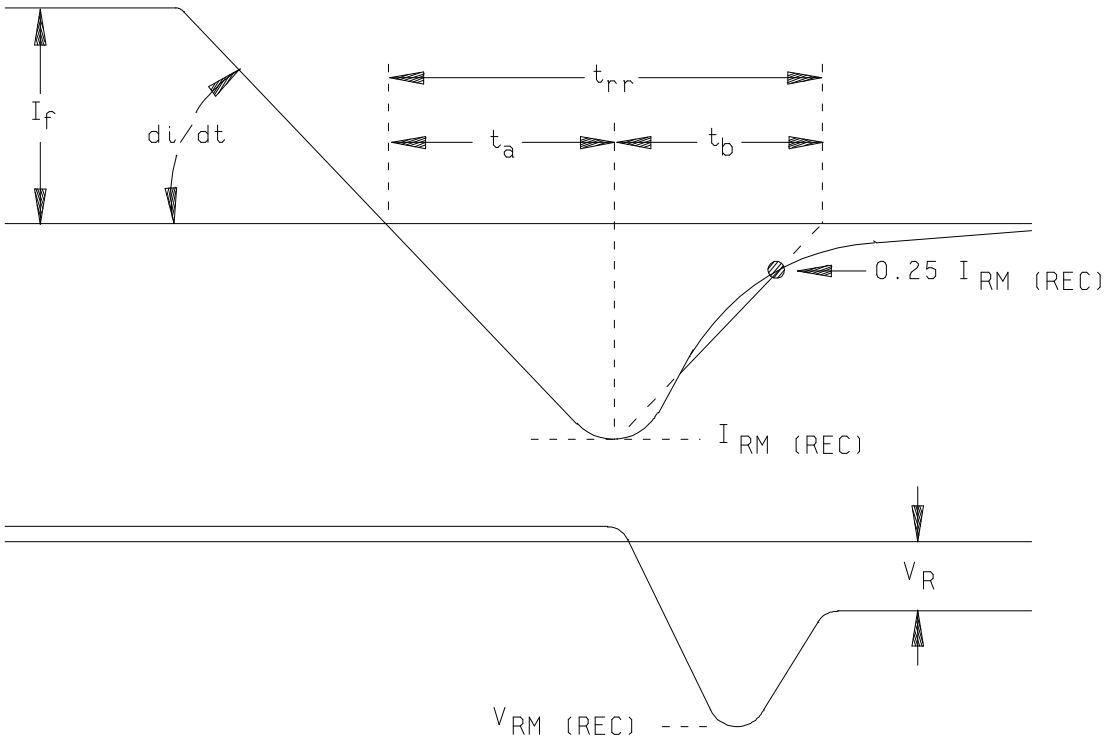


FIGURE 4031-9. Generalized reverse recovery waveforms for condition D.