REVISIONS

LTR	DESCRIPTION	DATE	APPROVED

Devices on this drawing may be used as a substitute for MIL-S-19500/493 which has been inactivated for new design.

Prepared in accordance with MIL-STD-100

Selected item drawing

REV																		
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PMIC N/A

PREPARED BY
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COLUMBUS, OH

Original date of drawing

5 December 2001

CHECKED BY
Alan Barone

TITLE

SEMICONDUCTOR DEVICE, PNPN, THYRISTOR, SILICON, (PROGRAMMABLE UNIJUNCTION TRANSISTOR), TYPES 2N6116, 2N6117, 2N6118, 2N6137, 2N6138

APPROVED BY
Thomas M. Hess

SIZE
A

CODE IDENT. NO.
037Z3

DWG NO.
01039

AMSC N/A

5961-E062

1. SCOPE

1.1 Scope. This drawing covers the detail requirements for PNPN, thyristor silicon, (programmable unijunction transistor). Three levels of product assurance are provided for each device type as specified in MIL-PRF-19500.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as follows:

01039	-	2N6116	NONTX, TX, TXV
|		|	|
Drawing number		Device type	Quality Level

1.2.1 Device types. The device type shall identify the polarity and voltage of the devices as follows:

Device type	Figure number
01039 - 2N6116, TX, TXV	1
01039 - 2N6117, TX, TXV	1
01039 - 2N6118, TX, TXV	1
01039 - 2N6137, TX, TXV	1
01039 - 2N6138, TX, TXV	1

1.2.2 Physical dimensions. See figure 1 (TO-18). The graphic symbol for the programmable unijunction transistor shall be as shown on figure 2.

1.3 Maximum ratings.

Device Types	P_T T_A = 25°C (1)	I_T	I_{TSM} Peak (2)	V_{GKS} (3)	V_{GKR}	V_{GAR}	V_{AKR}	V_{AKF}	T_{STG}	T_{OP}
	W	mA (rms)	A dc	V dc	V dc	V dc	V dc	V dc	°C	°C
2N6116	.300	300	5	40	5	40	40	40	-65 to +150	-55 to +125
2N6117	.300	300	5	40	5	40	40	40		
2N6118	.300	300	5	40	5	40	40	40		
2N6137	.300	300	5	40	5	40	40	40		
2N6138	.300	300	5	100	5	100	100	100		

(1) Derate linearly 2.5 mW/°C for T_A above +25° C.
(2) 10 µs, square wave, 1 percent duty cycle.
(3) Anode shorted to gate.

1.4 Primary electrical characteristics.

Device Types	I_P V_S = 10 V dc		I_V V_S = 10 V dc			V_F V_S = 10 V dc I_F = 50 mA dc	V_O	I_{GAO}	
	R_G = 10 kΩ	R_G = 1 MΩ	R_G = 200Ω	R_G = 10 kΩ	R_G = 1 MΩ			V_{GAO} = 40 V dc	V_{GAO} = 100 V dc
	Max µA dc	Max µA dc	Min mA dc	Min µA dc	Max µA dc	Min V dc	Min V (pk)	Max nA dc	Max nA dc
2N6116	5.0	2.0		70	50	1.5	6.0	5	
2N6117	2.0	0.3		50	50	1.5	6.0	5	
2N6118	1.0	0.15		50	25	1.5	6.0	5	
2N6137	5.0	2.0	1.5	70	50	1.0	9.0	10	
2N6138	5.0	2.0	1.5	70	50	1.0	9.0		10

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

STANDARD

DEPARTMENT OF DEFENSE

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from the Document Automation and Production Services (DAPS), Building 4D (DPM-DODSSP), 700 Robbins Avenue, Philadelphia, PA 19111-5094.

2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated detail specifications), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-PRF-19500, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-19500, and figure 1 herein.

3.2.1 Lead material and finish. Lead material shall be Kovar or Alloy 52; a copper core is permitted. Lead finish shall be gold or tin or solder. Where a choice of lead material or finish is desired, it shall be specified in the contract or purcahse order.

3.3 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, the following marking may be omitted from the body of the transistor.

a. Country of origin.

b. Manufacturer's identification.

3.4 Manufacturer eligibility. To be eligible to supply devices to this drawing, the manufacturer shall perform conformance inspection in accordance with procuring activity's requested first article testing requirements in accordance with 4.4 herein. Devices specified herein shall meet traceability and lot formation requirements of MIL-PRF-19500 except as modified by the procuring activity.

3.5 Submission of certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as a source of supply in 6.6. The certificate of compliance submitted to DSCC-VAC, prior to listing as a source of supply in 6.5, shall state that the manufacturer's product meets the applicable requirements of MIL-PRF-19500 and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance shall be provided with each lot of devices delivered in accordance with this drawing.

3.7 Recycled, recovered, or environmentally preferable materials. Recycled, recovered, or environmentally preferable materials should be used to the maximum extent possible provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.8 Quality levels. Three quality levels from the lowest level to the highest level are NON-TX, TX and TXV.

a. NON -TX devices are subjected to Groups A and B herein.

b. TX devices are subjected to the screening and burn-in requirements as specified in 4.3 herein, and Groups A and B.

c. TXV devices are subjected to the internal visual 100 percent inspection in accordance with Method 2072 of MIL-STD - 750 and table IV of MIL-PRF-19500, and then the screening and burn-in requirements as specified in 4.3 herein, and Groups A and B.

3.9 Workmanship. The semiconductor shall be uniform in quality and free from any defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Sample and inspection. Sampling and inspections shall be in accordance with MIL-PRF-19500, and as specified herein.

4.2 Conformance Inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.3 Screening. Screening shall be in accordance with MIL-PRF-19500 (table II), and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table II of MIL-PRF-19500)	Measurement TX and TXV levels
9	N/A
10	N/A
11	I_{GAO}, I_{P2} and I_{V2}
12	See 4.3.1
13	ΔI_{GAO} = 50% of initial value or 5 nA dc, whichever is greater. ΔI_{P2} = ± 100% of initial or 25 percent of maximum I_{P2}, whichever is greater. ΔI_{V2}= ± 25% of the initial reading.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows:

T_A = +125° C; I_A = 0; see figure 10; 2N6116, 2N6117, 2N6118, 2N6137 = V_{GK} = 40 V dc, 2N6138 = V_{GK} = 100 V dc.
Note: No heatsink or forced air cooling on the device shall be permitted.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein. (End-point electrical measurements shall be in accordance with the applicable steps of table III herein.)

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VIb of MIL-PRF-19500, and table II herein. Electrical measurements (end-points) and delta requirements shall be in accordance with the applicable steps of table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables.

4.5.1 Forward on-state voltage. The test circuit of figure 6 may be used to measure this parameter. The specified values (see table I) of V_S, R_G and anode current are applied. The anode to cathode voltage is measured as the on-state forward voltage.

4.5.2 Peak point anode current. This parameter shall be measured in the circuit of figure 5 or a suitable equivalent. The variable supply is adjusted to a point just prior to oscillation as detected by the absence of an output voltage pulse. Peak point anode current is the maxumim value is I_A just prior to oscillation.

4.5.3 Peak point offset voltage. This parameter shall be measured in the circuit of figure 7. The peak point offset voltage is equal to the peak point anode voltage minus the gate source voltage (V_S), immediately prior to triggering.

4.5.4 Valley point anode current. For the specified gate supply voltage (V_S) (see table I) and gate source resistance (R_G), the anode current corresponding to the valley point operating condition is measured. The test circuit of figure 6 or suitable equivalent, shall be used for this measurement. The specified gate supply voltage (V_S) and gate source resistance (R_G) shall be applied. The bias voltage shall be gradually increased until the device fires and then shall be varied to obtain a minimum value of V_{AK}. The I_A corresponding to this minimum value of V_{AK}. The I_A corresponding to this minimum value of V_{AK} is the I_V of the device under test.

4.5.5 Gate anode blocking current. This test shall be conducted in accordance with method 3036 of MIL-STD-750 except that the words and symbols, collector (C), base (B), and emitter (E) shall be replaced with gate (G), anode, and cathode, respectively.

4.5.6 Gate cathode blocking current. This test shall be conducted in accordance with method 3036 of MIL-STD-750, except that the words and symbols, collector (C), base (B) and emitter (E) shall be replaced with gate (G), anode, and cathode respectively.

4.5.7 Cathode peak pulse voltage. This test shall be conducted in the circuit of figure 8. The peak pulse voltage (V_O) is observed by an oscilloscope across the 20Ω resistor. The rise time of the pulse is defined as the time for the waveform to rise from 0.6 V to 6 V.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical examination	2071					
Subgroup 2						
Gate anode blocking current	3036	Bias condition D (see 4.5.5)	I_{GAO}			
2N6116, 2N6117, 2N6118		V_{GAO} = 40 V dc			5	nA dc
2N6137		V_{GAO} = 40 V dc			10	nA dc
2N6138		V_{AOS} = 100 V dc			10	nA dc
Gate cathode blocking current	3036	Bias condition C (see 4.5.6)	I_{GKS}			
2N6116, 2N6117, 2N6118		V_{GKS} = 40 V dc			50	nA dc
2N6137		V_{GKS} = 40 V dc			100	nA dc
2N6138		V_{GKS} = 100 V dc			100	nA dc
Peak point anode current		V_S = 10 V dc R_G = 1 MΩ See figure 5 (see 4.5.2)	I_{P1}			
2N6116, 2N6137, 2N6138					2.0	µA dc
2N6117					0.3	µA dc
2N6118					0.15	µA dc
Peak point anode current		V_S = 10 V dc R_G = 10 kΩ See figure 5 (see 4.5.2)	I_{P2}			
2N6116, 2N6137, 2N6138					5	µA dc
2N6117					2	µA dc
2N6118					1	µA dc
Peak point offset voltage		V_S = 10 V dc R_G = 1 MΩ See figure 7 (see 4.5.3)	V_{T1}			
2N6116				0.2	1.6	V dc
2N6117, 2N6118, 2N6137, 2N6138				0.2	0.6	V dc
Peak point offset voltage		V_S = 10 V dc R_G = 10 kΩ See figure 7 (see 4.5.3)	V_{T2}	0.2	0.6	V dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - continued						
Valley point anode current		V_S = 10 V dc R_G = 1 MΩ See figure 6 (see 4.5.4)	I_{V1}			
2N6116, 2N6117, 2N6137, 2N6138					50	µA dc
2N6118					25	µA dc
Valley point anode current		V_S = 10 V dc R_G = 10 kΩ See figure 6 (see 4.5.4)	I_{V2}			
2N6116, 2N6137, 2N6138				70		µA dc
2N6117, 2N6118				50		µA dc
Valley point anode current		V_S = 10 V dc R_G = 200 Ω See figure 6 (see 4.5.4)	I_{V3}	1.5		mA dc
2N6137, 2N6138 (only)						
Forward on-state voltage		V_S = 10 V dc R_G = 10 KΩ I_F = 50 mA dc See figure 6 (see 4.5.1)	V_F			
2N6116, 2N6117, 2N6118					1.5	V dc
2N6137, 2N6138					1.0	V dc
Subgroup 3						
Low temperature operation		T_A = -55°C				
Peak point anode current		V_S = 10 V dc R_G = 10 KΩ See figure 5 (see 4.5.2)	I_{P3}	0.001	10	µA dc
High temperature operation:		T_A = +125°C				
Gate anode blocking current	3036	Bias condition D (see 4.5.5)	I_{GAO2}		0.5	µA dc
2N6116, 2N6117, 2N6118, 2N6137		V_{GAO} = 40 V dc				
2N6138		V_{GAO} = 100 V dc				

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 3 - continued						
Valley point anode current		V_S = 10 V dc R_G = 10 kΩ See figure 6 (see 4.5.4)	I_{V2}			
2N6116, 2N6137, 2N6138					40	µA dc
2N6117, 2N6118					10	µA dc
Subgroup 4						
Peak pulse voltage		See figure 8 (see 4.5.7)	v_o			
2N6116, 2N6117, 2N6118				6.0		V dc
2N6137, 2N6138				9.0		V dc
Peak pulse voltage rise time		See figure 8 (see 4.5.7)	t_r		80	ns
Subgroups 5, 6, and 7						
Not applicable						

1/ For sampling plan, see MIL-PRF-19500.

TABLE II. Group B inspection.

Inspection 1/	MIL-STD-750	
	Method	Conditions
Subgroup 1 2/		
Solderability	2026	
Resistance to solvents	1022	
Subgroup 2		
Thermal shock (temperature cycling)	1051	
Hermetic seal Fine leak Gross leak	1071	
Electrical measurements		See table III steps 1, 3, and 5
Subgroup 3		
Steady-state operation	1027	T_A = +125°C; I_A = 0; See figure 10
2N6116, 2N6117, 2N6118, 2N6137		V_{GK} = 40 V dc
2N6138		V_{GK} = 100 V dc No heatsink or forced air cooling on the device shall be permitted.
Electrical measurements		See table III steps 2, 4, and 6
Subgroup 4		
Decap internal visual (design verification)	2075	
Bond strength	2037	Test condition A; All internal leads for each device shall be pulled separately.
Subgroup 5		
Not applicable		

See footnote at end of table.

TABLE II. Group B inspection – Continued.

Inspection 1/	MIL-STD-750	
	Method	Conditions
Subgroup 6		
High-temperature life (nonoperating)	1032	T_{STG} = +150°C
Electrical measurements		See table III steps 2, 4, and 6
Subgroup 7		
Not applicable		

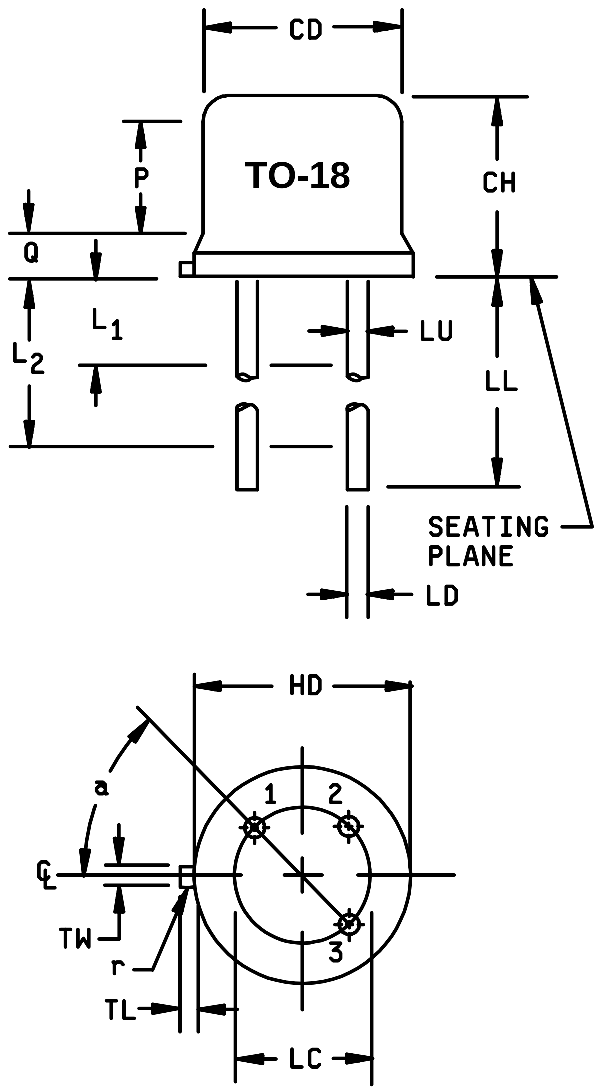
1/ For sample plan, see MIL-S-19500.

2/ Separate samples may be used for each test.

TABLE III. Groups A and B electrical measurements.

Step	Inspection	MIL-STD-750 Method	MIL-STD-750 Conditions	Symbol	Limits Min	Limits Max	Unit
1	Gate, anode blocking current	3036	Bias condition D (see 4.5.5)	I_{GAO}			
	2N6116, 2N6117, 2N6118		V_{GAO} = 40 V dc			5	nA dc
	2N6137		V_{GAO} = 40 V dc			10	nA dc
	2N6138		V_{GAO} = 100 V dc			10	nA dc
2	Gate, anode blocking current	3036	Bias condition D (see 4.5.5)	I_{GAO}			
	2N6116, 2N6117, 2N6118		V_{GAO} = 40 V dc			1	µA dc
	2N6137		V_{GAO} = 40 V dc			1	µA dc
	2N6138		V_{GAO} = 100 V dc			1	µA dc
3	Peak point anode current		V_S = 10 V dc R_G = 10 KΩ See figure 5 (see 4.5.2)	I_P			
	2N6116, 2N6137, 2N6138					5.0	µA dc
	2N6117					2.0	µA dc
	2N6118					1.0	µA dc
4	Peak point anode current		V_S = 10 V dc R_G = 10 KΩ See figure 5 (see 4.5.2)	I_P	.001		
	2N6116, 2N6137, 2N6138					6.0	µA dc
	2N6117					3.0	µA dc
	2N6118					2.0	µA dc
5	Valley point anode current		V_S = 10 V dc R_G = 10 KΩ See figure 6 (see 4.5.4)	I_V			
	2N6116, 2N6137, 2N6138				70		µA dc
	2N6117, 2N6118				50		µA dc
6	Valley point anode current		V_S = 10 V dc R_G = 10 KΩ See figure 6 (see 4.5.4)	I_V			
	2N6116, 2N6137, 2N6138				55		µA dc
	2N6117, 2N6118				35		µA dc

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7,8
LL	.500	.750	12.70	19.05	7,8
LU	.016	.019	0.41	0.48	7,8
L1		.050		1.27	7,8
L2	.250		6.35		7,8
P	.100		2.54		
Q		.030		0.76	5
TL	.028	.048	0.71	1.22	3,4
TW	.036	.046	0.91	1.17	3
r		.010		0.25	10
α	45° TP		45° TP		6
1, 2, 9, 11, 12					



NOTES:
1. Dimension are in inches.
2. Metric equivalents are given for general information only.
3. Beyond r (radius) maximum, TH shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods or by the gauge and gauging procedure shown in figure 2.
7. Dimension LU applies between L_1 and L_2. Dimension LD applies between L_2 and LL minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ANSI Y14.5M, diameters are equivalent to ϕx symbology.
12. Lead 1 = emitter, lead 2 = base, lead 3 = collector.

FIGURE 1. Physical dimensions TO-206AA (formerly TO-18)

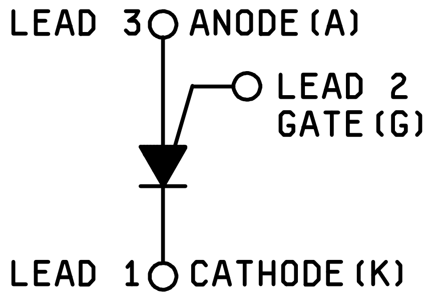


FIGURE 2. Symbol for programmable unijunction transistor.

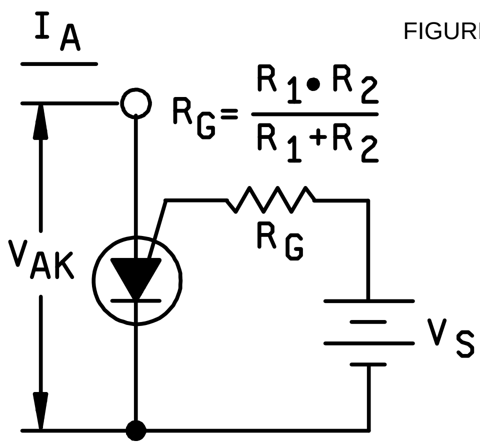


FIGURE 3. Equivalent test circuit used for electrical characteristics testing.

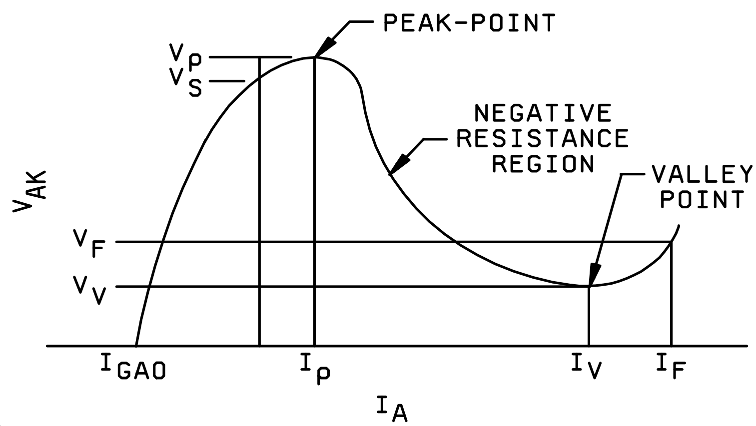
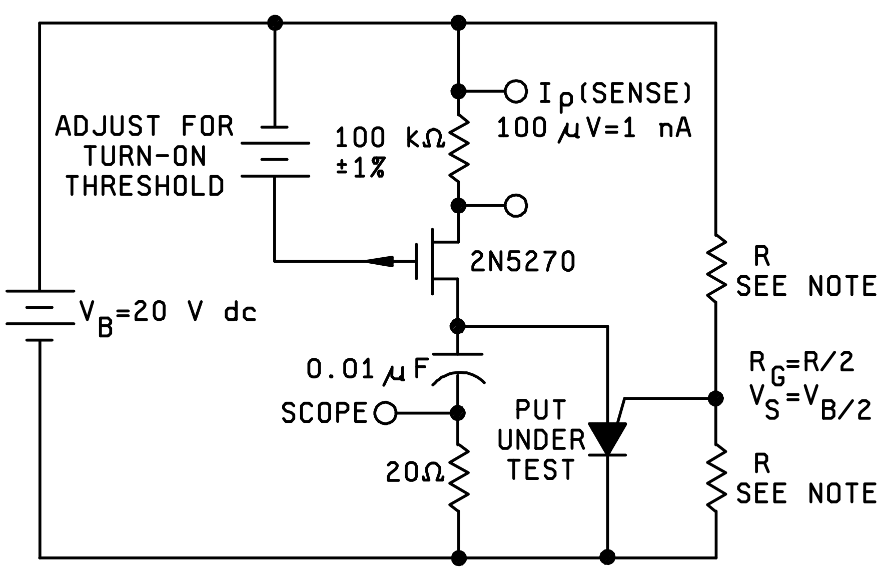
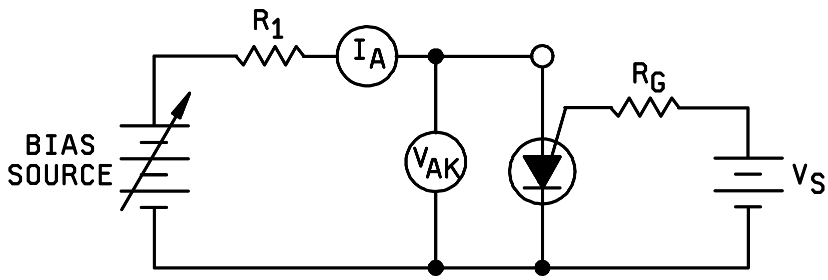


FIGURE 4. Static characteristics.



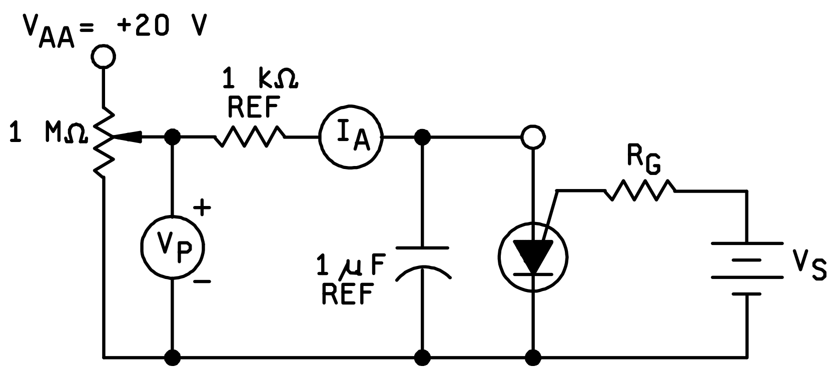
NOTE: Use 1 percent metal film resistors

FIGURE 5. Peak current (I_P) test circuit.



NOTES:
1. R1 chosen to limit current to a safe value.
2. Bias source is a well regulated 1 mV peak to peak ripple supply.

FIGURE 6. Valley point anode current and forward on-state voltage circuit.



NOTES:
1. 1 MΩ pot must be noisless to prevent false triggering.
2. Voltage source with less than 1 mV peak to peak ripple.

FIGURE 7. Offset voltage circuit.

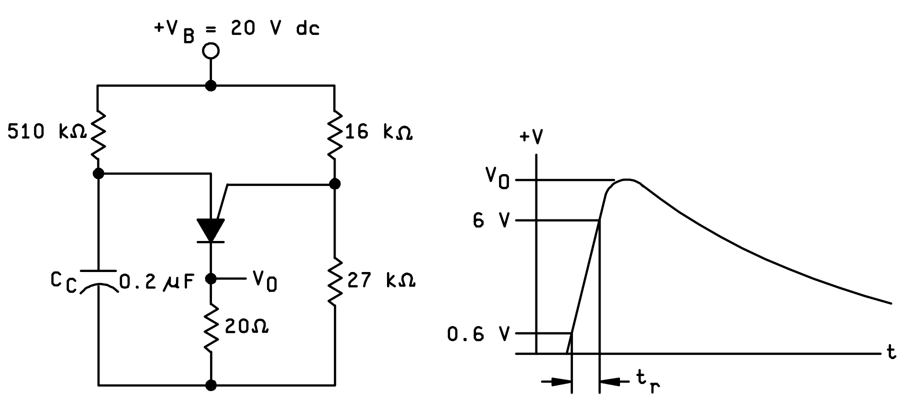
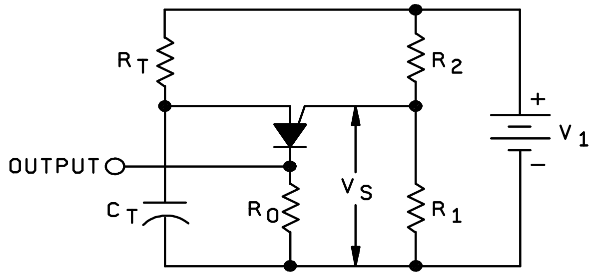
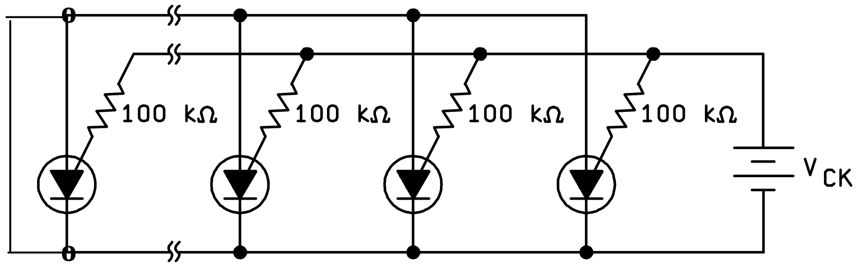


FIGURE 8. V_O and t_r test circuit.



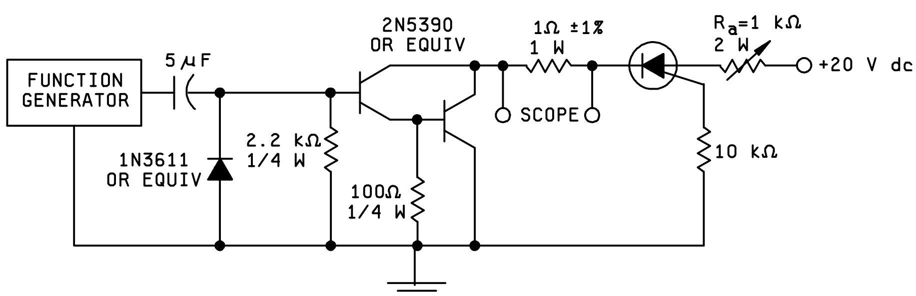
$V_S = R_1 (V_1 / R_1 + R_2)$

FIGURE 9. Typical oscillator circuit.



NOTE: Any number of devices under test may be added in parallel up to the maximum capability of the power supply to maintain voltage under the theoretical worst case condition if all devices under test shorted.

FIGURE 10. Burn-in and operating life test circuit.



NOTE: Adjust function generator to pulse width = 10 µs (square wave) and repetition rate = 1 kHz. Adjust R_a for 5 V peak (equivalent to 5 A peak). Total test time = 1 minute minimum.

FIGURE 11. Peak anode current test circuit.

5 PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Points' packaging activity within the Military Department or Defense Agency, or within the Military Departments' System Command. Packaging data retrieval is available from the managing Military Departments' or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6 NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Devices conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. This drawing is intended exclusively to prevent the proliferation of duplicate specifications, drawings, and stock number listings.

6.2 Ordering data. The contract or purchase order should specify the following:

a. Complete PIN (see 1.2).

b. Requirements for delivery of one copy of the conformance inspection data or certificate of compliance that parts have passed conformance inspection with each shipment of parts by the manufacturer.

c. Requirements for packaging and packing.

6.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

R_G Equivalent gate resistance (see figure 3).
I_F On-state current, RMS, from anode through cathode (see figure 4).
I_{GAO} Gate anode blocking current (dc), anode shorted to gate.
I_{GKS} Gate to cathode blocking current (dc), anode shorted to gate.
I_P Peak point anode current. This is the minimum value of anode current for which the slope of the static anode characteristic curve (see figures 4 and 5) is zero for a specified value of V_S and R_G.
I_T Maximum dc forward anode current.
I_{TSM} Nonrepetitive peak forward current.
I_V Valley point anode current. This is the maximum value of anode current for which the slope of the static anode characteristic curve (see figures 4 and 6) is zero for a specified value of V_S and R_G.
V_{GK} Gate to cathode voltage, (dc) voltage from gate to cathode.
V_{GA} Voltage (dc) from gate to anode.
V_{GKR} Gate to cathode reverse voltage.
V_{GAR} Gate to anode reverse voltage.
V_{AKR} Anode to cathode reverse voltage.
V_{AKF} Anode to cathode forward voltage.
V_T Offset voltage, at the peak point current (I_p). The difference between the anode peak point voltage (V_p) and the gate source voltage (V_S) (see figure 7).
V_F On-state voltage. The resultant dc voltage measured between the anode and cathode for specified values of on-state anode current (I_F) (see figure 6).
V_O Cathode peak pulse voltage. The cathode peak pulse voltage is defined as shown on figure 7. This parameter is a relative indicator of the peak anode current available for use in firing circuits.

V_P Peak point anode voltage. The voltage from anode to cathode when the peak point anode current flows for a specified value of V_S and R_G.

V_S Gate source voltage (see figure 9).

6.4 Replaceability. Devices covered by this drawing may be used as a substitute for MIL-S-19500/493.

DSCC drawing PIN (1)	Military part number
01039-2N6116	JAN2N6116
01039-2N6116TX	JANTX2N6116
01039-2N6116TXV	JANTXV2N6116
01039-2N6117	JAN2N6117
01039-2N6117TX	JANTX2N6117
01039-2N6117TXV	JANTXV2N6117
01039-2N6118	JAN2N6118
01039-2N6118TX	JANTX2N6118
01039-2N6118TXV	JANTXV2N6118
01039-2N6137	JAN2N6137
01039-2N6137TX	JANTX2N6137
01039-2N6137TXV	JANTXV2N6137
01039-2N6138	JAN2N6138
01039-2N6138TX	JANTX2N6138
01039-2N6138TXV	JANTXV2N6138

(1) Parts must be purchased to this DSCC Drawing PIN to assure that all performance requirements are met and tests performed.

6.5 Comments. Comments on this drawing should be directed to contact Defense Supply Center, Columbus, ATTN: DSCC-VAC, Post Office Box 3990, Columbus, OH 43216-5000.

6.6 Suggested sources of supply. Suggested sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have concurred with this drawing and have submitted a certificate of compliance (see 3.6 herein) to DSCC-VAC.

DSCC drawing PIN (1)	Vendor similar designation or type number	Vendor CAGE	Vendor name and address
01039-2N6116	2N6116	43611	Microsemi-NES 6 Lake Street Lawrence, MA 01841-3011
01039-2N6116TX	2N6116TX		
01039-2N6116TXV	2N6116TXV		
01039-2N6117	2N6117		
01039-2N6117TX	2N6117TX		
01039-2N6117TXV	2N6117TXV		
01039-2N6118	2N6118		
01039-2N6118TX	2N6118TX		
01039-2N6118TXV	2N6118TXV		
01039-2N6137	2N6137		
01039-2N6137TX	2N6137TX		
01039-2N6137TXV	2N6137TXV		
01039-2N6138	2N6138		
01039-2N6138TX	2N6138TX		
01039-2N6138TXV	2N6138TXV		

(1) Parts must be purchased to this DSCC PIN to assure that all performance requirements and tests are met.