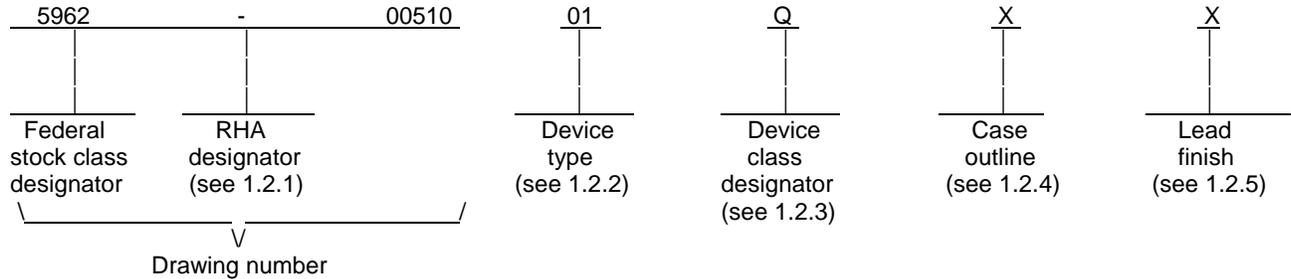


REVISIONS																				
LTR	DESCRIPTION														DATE (YR-MO-DA)	APPROVED				
A	Correct junction temperature in paragraph 1.3. - LTG														02-07-23	Thomas M. Hess				
REV																				
SHEET	55	56	57																	
REV																				
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
REV STATUS OF SHEETS				REV			A		A											
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14
PMIC N/A				PREPARED BY Larry T. Gauder						DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 http://www.dscc.dla.mil MICROCIRCUIT, DIGITAL, FIXED-POINT DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON										
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY Thanh V. Nguyen																
				APPROVED BY Thomas M. Hess																
				DRAWING APPROVAL DATE 02-02-08																
				REVISION LEVEL A						SIZE A	CAGE CODE 67268			5962-00510						
										SHEET 1 OF 57										

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (CV _{DD}).....	-0.3 V dc to +1.8 V dc
Supply voltage range (DV _{DD}).....	-0.3 V dc to +4.0 V dc
Input voltage range (V _{IN})	-0.3 V dc to +4.0 V dc
Output voltage range (V _{OUT}).....	-0.3 V dc to +4.0 V dc
Storage temperature range	-65°C to +150°C
Maximum junction temperature (T _J)	+129°C at 200 MHz
Thermal resistance, junction-to-case (θ _{JC})	3.00°C/W
Solder ball reflow condition (Peak temperature)	+220°C ±10°C

1.4 Recommended operating conditions.

Supply voltage range (CV _{DD}).....	+1.43 V dc to +1.57 V dc
Supply voltage range (DV _{DD}).....	+3.14 V dc to +3.46 V dc
Supply ground (V _{SS})	+0.0 V dc
High level input voltage (V _{IH}).....	2.0 V 3/
Low level input voltage (V _{IL})	0.8 V 4/
High level output current (I _{OH})	-8 mA
Low level output current (I _{OL})	8 mA
Case operating temperature range (T _C).....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ All voltage values are with respect to V_{SS}.
- 3/ V_{IH} is not production tested for CLKIN, CLKMODE[2:0], XCLKIN, XCS.
- 4/ V_{IL} is not production tested for CLKIN, TRST.

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2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Boundry scan instruction codes. The boundry scan instruction codes shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

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3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A)

3.11 IEEE 1149.1 compliance. These devices shall be compliant to IEEE1149.1.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low level output voltage <u>1/</u>	V _{OL}	DV _{DD} = 3.14 V I _{OL} = 12 mA	1, 2, 3	All		0.6	V
High level output voltage <u>1/</u>	V _{OH}	DV _{DD} = 3.14 V I _{OH} = -12 mA	1, 2, 3	All	2.4		V
Input current	I _{IN} <u>3/</u>	V _{IN} = V _{SS} to DV _{DD}	1, 2, 3	All		±10	μA
OFF- state output leakage current <u>2/</u>	I _{OZH} I _{OZL}	V _{OUT} = DV _{DD} or 0 V	1, 2, 3	All		±10	μA
Supply current, CPU + CPU memory access	I _{DD1V}	CV _{DD} = 1.43 V, CPU clock = 200 MHz	1, 2, 3	All		340.0 <u>4/</u>	mA
Supply current, peripherals	I _{DD2V}	CV _{DD} = 1.43 V, CPU clock = 200 MHz	1, 2, 3	All		235.0 <u>4/</u>	mA
Supply current, I/O pins	I _{DD3V}	DV _{DD} = 3.14 V, CPU clock = 200 MHz	1, 2, 3	All		45.0 <u>4/</u>	mA
Input capacitance	C _{IN}	f = 1 MHz at 0 V See 4.4.1b	4	All		15	pF
Output capacitance	C _{OUT}	f = 1 MHz at 0 V See 4.4.1b	4	All		15	pF
Functional tests		CV _{DD} = 1.43 V to 1.57 V DV _{DD} = 3.14 V to 3.46 V See 4.4.1c	7, 8	All			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLKIN TIMINGS [PLL USED] 6/ 7/ 8/							
Cycle time, CLKIN	1 <u>5/</u>	See figure 5	9, 10, 11	All	5.*M		ns
Pulse duration, CLKIN high	2		9, 10, 11	All	0.45C		ns
Pulse duration, CLKIN low	3		9, 10, 11	All	0.45C		ns
Transition time, CLKIN	4		9, 10, 11	All		0.5	ns
CLKIN TIMINGS [PLL BYPASSED](X1)] 6/ 8/							
Cycle time, CLKIN	1	See figure 5	9, 10, 11	All	5		ns
Pulse duration, CLKIN high	2		9, 10, 11	All	0.45C		ns
Pulse duration, CLKIN low	3		9, 10, 11	All	0.45C		ns
Transition time, CLKIN	4		9, 10, 11	All		0.6	ns
XCLKIN TIMINGS 9/							
Cycle time, XCLKIN	1 <u>5/</u>	See figure 5	9, 10, 11	All	4P		ns
Pulse duration, XCLKIN high	2		9, 10, 11	All	1.8P		ns
Pulse duration, XCLKIN low	3		9, 10, 11	All	1.8P		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
CLKOUT2 TIMINGS <u>9/ 10/</u>							
Cycle time, CLKOUT2	1	See figure 5	9, 10, 11	All	2P - 0.7	2P + 0.7	ns
Pulse duration, CLKOUT2 high	2		9, 10, 11	All	P - 0.7	P + 0.7	ns
Pulse duration, CLKOUT2 low	3		9, 10, 11	All	P - 0.7	P + 0.7	ns
XFCLK TIMINGS <u>9/ 11/</u>							
Cycle time, XFCLK	1	See figure 5	9, 10, 11	All	D*P -0.7	D*P +0.7	ns
Pulse duration, XFCLK high	2		9, 10, 11	All	D/2* P -0.7	D/2*P +0.7	ns
Pulse duration, XFCLK low	3		9, 10, 11	All	D/2*P -0.7	D/2*P +0.7	ns
ASYNCHRONOUS MEMORY READ and WRITE TIMING <u>9/ 12/ 13/ 14/ 15/</u>							
Output setup time, select signals valid to ARE low	1 <u>5/</u>	See figure 5	9, 10, 11	All	RS*P-2		ns
Output hold time, $\overline{\text{ARE}}$ high to select signals invalid	2		9, 10, 11	All	RH*P-2		ns
Setup time, EDx valid before $\overline{\text{ARE}}$ high	3 <u>5/</u>		9, 10, 11	All	1		ns
Hold time, EDx valid after ARE high	4 <u>5/</u>		9, 10, 11	All	4.9		ns
Setup time, ARDY high before ARE low	6 <u>5/</u>		9, 10, 11	All	-[(RST -3) * P-6]		ns
Hold time, ARDY high after ARE low	7 <u>5/</u>		9, 10, 11	All	(RST -3) * P+2		ns
Delay time, ARDY high to $\overline{\text{ARE}}$ high	8		9, 10, 11	All	3P	4P+5	ns
Setup time, ARDY low before ARE low	9 <u>5/</u>		9, 10, 11	All	-[(RST -3) * P-6]		ns
Hold time, ARDY low after ARE low	10 <u>5/</u>		9, 10, 11	All	(RST -3) * P+2		ns
Pulse width, ARDY high	11		9, 10, 11	All	2P		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	

ASYNCHRONOUS MEMORY READ and WRITE TIMING 9/ 12/ 13/ 14/ 15/ – Continued

Output setup time, $\overline{\text{select}}$ signals valid to AWE low	12 <u>5/</u>	See figure 5	9, 10, 11	All	WS * P-3		ns
Output hold time, $\overline{\text{AWE}}$ high to select signals invalid	13		9, 10, 11	All	WH * P-2		ns
Setup time, $\overline{\text{ARDY}}$ high before $\overline{\text{AWE}}$ low	15 <u>5/</u>		9, 10, 11	All	-[(WST-3) * P-6]		ns
Hold time, $\overline{\text{ARDY}}$ high after $\overline{\text{AWE}}$ low	16 <u>5/</u>		9, 10, 11	All	(WST-3) * P+2		ns
Delay time, $\overline{\text{ARDY}}$ high to $\overline{\text{AWE}}$ high	17		9, 10, 11	All	3P	4P +5	ns
Setup time, $\overline{\text{ARDY}}$ low before $\overline{\text{AWE}}$ low	18 <u>5/</u>		9, 10, 11	All	-[(WST-3) * P-6]		ns
Hold time, $\overline{\text{ARDY}}$ low after $\overline{\text{AWE}}$ low	19 <u>5/</u>		9, 10, 11	All	(WST-3) * P+2		ns

SBSRAM READ and WRITE TIMING 9/ 16/

Output setup time, $\overline{\text{CEx}}$ valid before CLKOUT2 high	1 <u>5/</u>	See figure 5	9, 10, 11	All	P -0.8		ns
Output hold time, $\overline{\text{CEx}}$ valid after CLKOUT2 high	2		9, 10, 11	All	P -4.0		ns
Output setup time, $\overline{\text{BEx}}$ valid before CLKOUT2 high	3 <u>5/</u>		9, 10, 11	All	P -0.8		ns
Output hold time, $\overline{\text{BEx}}$ invalid after CLKOUT2 high	4		9, 10, 11	All	P -4.0		ns
Output setup time, $\overline{\text{EAx}}$ valid before CLKOUT2 high	5 <u>5/</u>		9, 10, 11	All	P -0.8		ns
Output hold time, $\overline{\text{EAx}}$ invalid after CLKOUT2 high	6		9, 10, 11	All	P -4.0		ns
Setup time, read EDx valid before CLKOUT2 high	7 <u>5/</u>		9, 10, 11	All	2.0		
Hold time, read EDx valid after CLKOUT2 high	8 <u>5/</u>		9, 10, 11	All	2.0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions -55°C ≤ T _c ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	

SBSRAM READ and WRITE TIMING 9/ 16/ – Continued

Output setup time, $\overline{SDCAS}/\overline{SSADS}$ valid before CLKOUT2 high	9 <u>5/</u>	See figure 5	9, 10, 11	All	P-0.8		ns
Output hold time, $\overline{SDCAS}/\overline{SSADS}$ valid after CLKOUT2 high	10		9, 10, 11	All	P-4.0		ns
Output setup time, $\overline{SDRAS}/\overline{SSOE}$ valid before CLKOUT2 high	11 <u>5/</u>		9, 10, 11	All	P-0.8		ns
Output hold time, $\overline{SDRAS}/\overline{SSOE}$ valid after CLKOUT2 high	12		9, 10, 11	All	P-4		ns
Output setup time, EDx valid before CLKOUT2 high <u>17/</u>	13 <u>5/</u>		9, 10, 11	All	P-1.2		ns
Output hold time, EDx invalid after CLKOUT2 high	14		9, 10, 11	All	P-4.0		ns
Output setup time, $\overline{SDWE}/\overline{SSWE}$ valid before CLKOUT2 high	15 <u>5/</u>		9, 10, 11	All	P-0.8		ns
Output hold time, $\overline{SDWE}/\overline{SSWE}$ valid after CLKOUT2 high	16		9, 10, 11	All	P-4.0		ns

SDRAM COMMAND TIMING 9/ 16/

Output setup time, \overline{CEx} valid before CLKOUT2 high	1 <u>5/</u>	See figure 5	9, 10, 11	All	P-0.9		ns
Output hold time, \overline{CEx} valid after CLKOUT2 high	2		9, 10, 11	All	P-4.0		ns
Output setup time, \overline{BEx} valid before CLKOUT2 high	3 <u>5/</u>		9, 10, 11	All	P-0.9		ns
Output hold time, \overline{BEx} invalid after CLKOUT2 high	4		9, 10, 11	All	P-4.0		ns
Output setup time, EAx valid before CLKOUT2 high	5 <u>5/</u>		9, 10, 11	All	P-0.9		ns
Output hold time, EAx invalid after CLKOUT2 high							

See footnote at end of table.

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TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
SDRAM COMMAND TIMING <u>9/ 16/</u> – Continued							
Output hold time, EAx invalid after CLKOUT2 high	6	See figure 5	9, 10, 11	All	P-4.0		ns
Setup time, read EDx valid before CLKOUT2 high	7 <u>5/</u>		9, 10, 11	All	1.2		ns
Hold time, read EDx valid after CLKOUT2 high	8 <u>5/</u>		9, 10, 11	All	2.9		ns
Output setup time, SDCAS/ SSADS valid before CLKOUT2 high	9 <u>5/</u>		9, 10, 11	All	P-0.9		ns
Output hold time, SDCAS/ SSADS valid after CLKOUT2 high	10		9, 10, 11	All	P-4.0		ns
Output setup time, EDx <u>17/</u> valid before CLKOUT2 high	11 <u>5/</u>		9, 10, 11	All	P-1.5		ns
Output hold time, read EDx invalid after CLKOUT2 high	12		9, 10, 11	All	P-4.0		ns
Output setup time, SDWE/ SSWE valid before CLKOUT2 high	13 <u>5/</u>		9, 10, 11	All	P-0.9		ns
Output hold time, SDWE/ SSWE valid after CLKOUT2 high	14		9, 10, 11	All	P-4.0		ns
Output setup time, SDA10 valid before CLKOUT2 high	15 <u>5/</u>		9, 10, 11	All	P-0.9		ns
Output hold time, SDA10 invalid after CLKOUT2 high	16		9, 10, 11	All	P-4.0		ns
Output setup time, SDRAS/ SSOE valid before CLKOUT2 high	17 <u>5/</u>		9, 10, 11	All	P-0.9		ns
Output hold time, SDRAS/ SSOE valid after CLKOUT2 high	18		9, 10, 11	All	P-4.0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
<u>HOLD/HOLDA TIMING 9/ 18/ 19/</u>							
Delay time, $\overline{\text{HOLD}}$ low to EMIF Bus high impedance	1	See figure 5	9, 10, 11	All	3P		ns
Delay time, EMIF Bus high impedance to $\overline{\text{HOLDA}}$ low	2		9, 10, 11	All	0.0	2P	ns
Output hold time, $\overline{\text{HOLD}}$ low after $\overline{\text{HOLDA}}$ low	3		9, 10, 11	All	P		ns
Delay time, $\overline{\text{HOLD}}$ high to EMIF Bus low impedance	4		9, 10, 11	All	3P	7P	ns
Delay time, EMIF Bus low impedance to $\overline{\text{HOLDA}}$ high	5		9, 10, 11	All	0.0	2P	ns
<u>RESET TIMING 9/</u>							
Width of the $\overline{\text{RESET}}$ pulse (PLL stable) <u>20/</u>	1	See figure 5	9, 10, 11	All	10P		ns
Width of the $\overline{\text{RESET}}$ pulse (PLL needs to sync up) <u>21/</u>					250.0		μs
Delay time, $\overline{\text{RESET}}$ low to CLKOUT2 invalid <u>23/</u>	2		9, 10, 11	All	P		ns
Delay time, $\overline{\text{RESET}}$ high to CLKOUT2 valid <u>23/</u>	3		9, 10, 11	All		4P	ns
Delay time, $\overline{\text{RESET}}$ low to high group invalid <u>23/</u>	4		9, 10, 11	All	P		ns
Delay time, $\overline{\text{RESET}}$ high to high group valid <u>23/</u>	5		9, 10, 11	All		4P	ns
Delay time, $\overline{\text{RESET}}$ low to low group invalid <u>23/</u>	6		9, 10, 11	All	P		ns
Delay time, $\overline{\text{RESET}}$ high to low group valid <u>23/</u>	7		9, 10, 11	All		4P	ns
Delay time, $\overline{\text{RESET}}$ low to Z group high impedance <u>23/</u>	8		9, 10, 11	All	P		ns
Delay time, $\overline{\text{RESET}}$ high to Z group valid <u>23/</u>	9	9, 10, 11	All		4P	ns	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
RESET TIMING 9/ – Continued							
Setup time, XD configuration bits valid before RESET high 22/	10	See figure 5	9, 10, 11	All	5P		ns
Hold time, XD configuration bits valid after RESET high 22/	11		9, 10, 11	All	5P		ns
INTERRUPT TIMING 9/							
Response time, EXT_INTx high to IACK high	1	See figure 5	9, 10, 11	All	9P		ns
Width of the interrupt pulse low	2		9, 10, 11	All	2P		ns
Width of the interrupt pulse high	3		9, 10, 11	All	2P		ns
Delay time, CLKOUT2 low to IACK valid	4		9, 10, 11	All	-1.5	10.0	ns
Delay time, CLKOUT2 low to INUMx valid	5		9, 10, 11	All	-2.0	10.0	ns
Delay time, CLKOUT2 low to INUMx invalid	6		9, 10, 11	All	-2.0	10.0	ns
EXPANSION BUS SYNCHRONOUS FIFO TIMING							
Delay time, XFCLK high to XCE _x valid 26/	1	See figure 5	9, 10, 11	All	-1.5	4.5	ns
Delay time, XFCLK high to XBE[3:0]/XA[5:2] valid 24/	2		9, 10, 11	All	-1.5	4.5	ns
Delay time, XFCLK high to XOE valid	3		9, 10, 11	All	-1.5	4.5	ns
Delay time, XFCLK high to XRE valid	4		9, 10, 11	All	-1.5	4.5	ns
Setup time, read XD _x valid before XFCLK high	5 5/		9, 10, 11	All	3.0		ns
Hold time, read XD _x valid after XFCLK high	6 5/		9, 10, 11	All	2.5		ns
Delay time, XFCLK high to XWE/XWAIT valid 25/	7		9, 10, 11	All	-1.5	4.5	ns
Delay time, XFCLK high to XD _x valid	8 5/		9, 10, 11	All		4.5	ns
Delay time, XFCLK high to XD _x invalid	9		9, 10, 11	All	-1.5		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
EXPANSION BUS ASYNCHRONOUS PERIPHERAL TIMING <u>9/ 12/ 13/ 14/ 15/</u>							
Output setup time, <u>select</u> signals valid to XRE low	1 <u>5/</u>	See figure 5	9, 10, 11	All	RS * P-2		ns
Output hold time, <u>XRE</u> low to select signals invalid	2		9, 10, 11	All	RH * P-2		ns
Setup time, <u>XDx</u> valid before XRE high	3 <u>5/</u>		9, 10, 11	All	4.5		ns
Hold time, XDx valid after XRE high	4 <u>5/</u>		9, 10, 11	All	2.5		ns
Setup time, <u>XRDY</u> high before XRE low	6 <u>5/</u>		9, 10, 11	All	-[(RST-3) * P-6]		ns
Hold time, <u>XRDY</u> high after XRE low	7 <u>5/</u>		9, 10, 11	All	(RST-) * P+2		ns
Delay time, XRDY high to XRE high	8		9, 10, 11	All	3P	4P+ 5	ns
Setup time, <u>XRDY</u> low before XRE low	9 <u>5/</u>		9, 10, 11	All	-[(RST-3) * P-6]		ns
Hold time, XRDY low after XRE low	10 <u>5/</u>		9, 10, 11	All	(RST-3) * P+2		ns
Pulse width, XRDY high	11		9, 10, 11	All	2P		ns
Output setup time, <u>select</u> signals valid to XWE low	12 <u>5/</u>		9, 10, 11	All	WS * P-3		ns
Output hold time, <u>XWE</u> low to select signals invalid	13		9, 10, 11	All	WH * P-2		ns
Setup time, <u>XRDY</u> high before XWE low	15 <u>5/</u>		9, 10, 11	All	-[(WST-3) * P-6]		ns
Hold time, XRDY high after XWE low	16 <u>5/</u>		9, 10, 11	All	(WST-3) * P+2		ns
Delay time, XRDY high to XWE high	17		9, 10, 11	All	3P	4P +5	ns
Setup time, <u>XRDY</u> low before XWE low	18 <u>5/</u>		9, 10, 11	All	-[(WST-3) * P-6]		ns
Hold time, XRDY low after XWE low	19 <u>5/</u>		9, 10, 11	All	(WST-3) * P+2		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions -55°C ≤ T _c ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
EXPANSION BUS SYNCHRONOUS HOST PORT TIMING <u>9/</u>							
Setup time, \overline{XCS} valid before XCLKIN high	1 <u>5/</u>	See figure 5	9, 10, 11	All	3.5		ns
Hold time, \overline{XCS} valid after XCLKIN high	2 <u>5/</u>		9, 10, 11	All	2.8		ns
Setup time, \overline{XAS} valid before XCLKIN high	3 <u>5/</u>		9, 10, 11	All	3.5		ns
Hold time, \overline{XAS} valid after XCLKIN high	4 <u>5/</u>		9, 10, 11	All	2.8		ns
Setup time, XCNTL valid before XCLKIN high	5 <u>5/</u>		9, 10, 11	All	3.5		ns
Hold time, XCNTL valid after XCLKIN high	6 <u>5/</u>		9, 10, 11	All	2.8		ns
Setup time, XW/R valid before XCLKIN high <u>27/</u>	7 <u>5/</u>		9, 10, 11	All	3.5		ns
Hold time, XW/R valid after XCLKIN high <u>27/</u>	8 <u>5/</u>		9, 10, 11	All	2.8		ns
Setup time, XBLAST valid before XCLKIN high <u>28/</u>	9 <u>5/</u>		9, 10, 11	All	3.5		ns
Hold time, XBLAST valid after XCLKIN high <u>28/</u>	10 <u>5/</u>		9, 10, 11	All	2.8		ns
Delay time, XCLKIN high to XDx low impedance	11		9, 10, 11	All	0.0		ns
Delay time, XCLKIN high to XDx valid	12 <u>5/</u>		9, 10, 11	All		17.0	ns
Delay time, XCLKIN high to XDx invalid	13		9, 10, 11	All	5.0		ns
Delay time, XCLKIN high to XDx high impedance	14		9, 10, 11	All		4P	ns
Delay time, XCLKIN high to XRDY invalid <u>30/</u>	15		9, 10, 11	All	5.0	17.0	ns
Setup time, $\overline{XBE[3:0]}/XA[5:2]$ valid before XCLKIN high <u>29/</u>	16 <u>5/</u>		9, 10, 11	All	3.5		ns
Hold time, $\overline{XBE[3:0]}/XA[5:2]$ valid after XCLKIN high <u>29/</u>	17 <u>5/</u>		9, 10, 11	All	2.8		ns
Setup time, XDx valid before XCLKIN high	18 <u>5/</u>		9, 10, 11	All	3.5		ns
Hold time, XDx valid after XCLKIN high	19 <u>5/</u>		9, 10, 11	All	2.8		ns
Delay time, XCLKIN high to XRDY low impedance	20		9, 10, 11	All	5.0	17.0	ns
Delay time, XCLKIN high to XRDY high impedance <u>30/</u>	21		9, 10, 11	All	2P+5	3P +17.0	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions -55°C ≤ T _c ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
EXPANSION BUS SYNCHRONOUS HOST PORT TIMING - Continued <u>9/</u>							
Delay time, XCLKIN high to XAS valid	1	See figure 5	9, 10, 11	All	5.0	17.0	ns
Delay time, XCLKIN high to XW/R valid <u>27/</u>	2		9, 10, 11	All	5.0	17.0	ns
Delay time, XCLKIN high to XBLAST valid <u>31/</u>	3		9, 10, 11	All	5.0	17.0	ns
Delay time, XCLKIN high to XBE[3:0]/XA[5:2] valid <u>29/</u>	4		9, 10, 11	All	5.0	17.0	ns
Delay time, XCLKIN high to XDx low impedance	5		9, 10, 11	All	0.0		ns
Delay time, XCLKIN high to XDx valid	6 <u>5/</u>		9, 10, 11	All		17.0	ns
Delay time, XCLKIN high to XDx invalid	7		9, 10, 11	All	5.0		ns
Delay time, XCLKIN high to XDx high impedance	8		9, 10, 11	All		4P	ns
Setup time, XDx valid before XCLKIN high	9 <u>5/</u>		9, 10, 11	All	3.5		ns
Hold time, XDx valid after XCLKIN high	10 <u>5/</u>		9, 10, 11	All	2.8		ns
Setup time XRDY valid before XCLKIN high <u>30/</u>	11 <u>5/</u>		9, 10, 11	All	3.5		ns
Hold time, XRDY valid after XCLKIN high <u>30/</u>	12 <u>5/</u>		9, 10, 11	All	2.8		ns
Delay time, XCLKIN high to XWE/XWAIT valid <u>32/</u>	13		9, 10, 11	All	5.0	17.0	ns
Setup time, XBOFF valid before XCLKIN high	14 <u>5/</u>		9, 10, 11	All	3.5		ns
Hold time, XBOFF valid after XCLKIN high	15 <u>5/</u>		9, 10, 11	All	2.8		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
EXPANSION BUS ASYNCHRONOUS HOST PORT TIMING <u>9/</u>							
Pulse duration, \overline{XCS} low	1 <u>5/</u>	See figure 5	9, 10, 11	All	4P		ns
Pulse duration, \overline{XCS} high	2 <u>5/</u>		9, 10, 11	All	4P		ns
Setup time, expansion bus select signals valid before \overline{XCS} low <u>33/</u>	3 <u>5/</u>		9, 10, 11	All	1.0		ns
Hold time, expansion bus select signals valid after \overline{XCS} low <u>33/</u>	4 <u>5/</u>		9, 10, 11	All	3.4		ns
Delay time, \overline{XCS} low to XDx low impedance	5		9, 10, 11	All	0.0		ns
Delay time, \overline{XCS} high to XDx invalid	6		9, 10, 11	All	0.0	12.0	ns
Delay time, \overline{XCS} high to XDx high impedance	7		9, 10, 11	All		4P	ns
Delay time, XRDY low to XDx valid	8		9, 10, 11	All	-4.0	1.0	ns
Delay time, \overline{XCS} high to XRDY high	9		9, 10, 11	All	0.0	12.0 <u>5/</u>	ns
Hold time, \overline{XCS} low after XRDY low	10		9, 10, 11	All	P+1.5		ns
Setup time, $\overline{XBE[3:0]}/XA[5:2]$ valid before \overline{XCS} high <u>29/</u>	11 <u>5/</u>		9, 10, 11	All	1.0		ns
Hold time, $\overline{XBE[3:0]}/XA[5:2]$ valid after \overline{XCS} high <u>29/</u>	12 <u>5/</u>		9, 10, 11	All	3.0		ns
Setup time, XDx valid before \overline{XCS} high	13 <u>5/</u>		9, 10, 11	All	1.0		ns
Hold time, XDx valid after \overline{XCS} high	14 <u>5/</u>		9, 10, 11	All	3.0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	

EXPANSION BUS ARBITRATION - INTERNAL ARBITER ENABLED 9/ 34/

Delay time, XHOLD high to XBus high impedance <u>35/</u>	1	See figure 5	9, 10, 11	All	3P		ns
Delay time, XBus high impedance to XHOLDA high	2		9, 10, 11	All	0.0	2P	ns
Output hold time, XHOLD high after XHOLDA high	3		9, 10, 11	All	P		ns
Delay time, XHOLD low to XHOLDA low	4		9, 10, 11	All	3P		ns
Delay time, XHOLDA low to XBus low impedance	5		9, 10, 11	All	0.0	2P	ns

EXPANSION BUS ARBITRATION - INTERNAL ARBITER DISABLED 9/ 34/

Delay time, XHOLDA high to XBus low impedance	1	See figure 5	9, 10, 11	All	2P	2P+10	ns
Delay time, XBus high impedance to XHOLD low	2		9, 10, 11	All	0.0	2P	ns

McBSP TIMINGS 9/ 36/

Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input <u>37/</u>	1	See figure 5	9, 10, 11	All	4.0	16.0	ns	
Cycle time, CLKR/X <u>38/</u>	2		CLKR/X int	9, 10, 11	All	2P		ns
	2		CLKR/X ext			2P		
Pulse duration, CLKR/X high or CLKR/X low <u>39/</u>	3		CLKR/X int	9, 10, 11	All	C-2	C+2	ns
	3		CLKR/X ext			P-1 <u>40/</u>		
Delay time, CLKR high to internal FSR valid <u>37/</u>	4		CLKR int	9, 10, 11	All	-3.0	3.0	ns
Setup time, external FSR high before CLKR low	5 <u>5/</u>		CLKR int	9, 10, 11	All	9.0		ns
			CLKR ext			2.0		
Hold time, external FSR high after CLKR low	6 <u>5/</u>		CLKR int	9, 10, 11	All	6.0		ns
			XLKR ext			4.0		
Setup time, DR valid before CLKR low	7 <u>5/</u>		CLKR int	9, 10, 11	All	8.0		ns
			CLKR ext			0.5		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions -55°C ≤ T _c ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
McBSP TIMINGS – Continued <u>9/ 36/</u>								
Hold time, DR valid after CLKR low	8 <u>5/</u>	See figure 5	CLKR int	9, 10, 11	All	3.0	ns	
			CLKR ext			5.0		
Delay time, CLKX high to internal FSX valid <u>37/</u>	9		CLKX int	9, 10, 11	All	-3.0	3.0	ns
			CLKX ext			-3.0	9.0	
Setup time, external FSX high before CLKX low	10 <u>5/</u>		CLKX int	9, 10, 11	All	9.0	ns	
			CLKX ext			2.0		
Hold time, external FSX high after CLKX low	11 <u>5/</u>		CLKX int	9, 10, 11	All	6.0	ns	
			CLKX ext			4.0		
Disable time, DX high impedance following last data bit from CLKX high <u>37/</u>	12		CLKX int	9, 10, 11	All	-1.0	5.0	ns
			CLKC ext			2.0	9.0	
Delay time, CLKX high to DX valid <u>37/</u>	13		CLKX int	9, 10, 11	All	-1.0	4.0	ns
			CLKX ext			2.0	11.0	
Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode <u>37/</u>	14		FSX int	9, 10, 11	All	-1.0	5.0	ns
			FSX ext			0.0	10.0	

FSR TIMING When GSYNC = 1

Setup time, FSR high before CLKS high	1	See figure 5	9, 10, 11	All	4.0	ns
Hold time, FSR high after CLKS high	2		9, 10, 11	All	4.0	ns

McBSP TIMING as SPI MASTER or SLAVE: CLKSTP = 10b, CLKXP = 0 9/ 41/

Hold time, FSX low after CLKX low <u>43/</u>	1	See figure 5	Master <u>42/</u>	9, 10, 11	All	T-2	T+3	ns
Delay time, FSX low to CLKX low <u>44/</u>	2		Master <u>42/</u>	9, 10, 11	All	L-2	L+3	ns
Delay time, CLKX high to DX valid	3		Master <u>42/</u>			-4.0	4.0	ns
			Slave			3P+4	5P+17	
Setup time, DR valid before CLKX low	4		Master	9, 10, 11	All	12.0		ns
			Slave			2-3P		
Hold time, DR valid after CLKX low	5	Master			4.0		ns	
		Slave			5+6P			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions -55°C ≤ T _c ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
McBSP TIMING as SPI MASTER or SLAVE: CLKSTP = 10b, CLKXP = 0 – Continued <u>9/ 41/</u>								
Disable time, DX high impedance following last data bit from CLKX low	6	See figure 5	Master <u>42/</u>	9, 10, 11	All	L-2	L+3	ns
Disable time, DX high impedance following last data bit from FSX high	7		Slave	9, 10, 11	All	P+3	3P+17	ns
Delay time, FSX low to DX valid	8		Slave	9, 10, 11	All	2P+2	4P+17	ns
McBSP TIMING as SPI MASTER or SLAVE: CLKSTP = 11b, CLKXP = 0 <u>9/ 41/</u>								
Hold time, FSX low after CLKX low <u>43/</u>	1	See figure 5	Master <u>42/</u>	9, 10, 11	All	L-2	L+3	ns
Delay time, FSX low to CLKX high <u>44/</u>	2		Master <u>42/</u>	9, 10, 11	All	T-2	T+3	ns
Delay time, CLKX low to DX valid	3		Master <u>42/</u>	9, 10, 11	All	-4.0	4.0	ns
			Slave			3P+4	5P+17	
Setup time, DR valid before CLKX high	4		Master	9, 10, 11	All	12.0		ns
			Slave			2-3P		
Hold time, DR valid after CLKX high	5		Master	9, 10, 11	All	4.0		ns
		Slave	5+6P					
Disable time, DX high impedance following last data bit from CLKX low	6	Master <u>42/</u>	9, 10, 11	All	-2.0	4.0	ns	
		Slave			3P+3	5P+17		
Delay time, FSX low to DX valid	7	Master <u>42/</u>	9, 10, 11	All	H-2	H+4	ns	
		Slave			2P+2	4P+17		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions -55°C ≤ T _c ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
McBSP TIMING as SPI MASTER or SLAVE: CLKSTP = 10b, CLKXP = 1 9/ 41/								
Hold time, FSX low after CLKX high 43/	1	See figure 5	Master 42/	9, 10, 11	All	T-2	T+3	ns
Delay time, FSX low to CLKX low 44/	2		Master 42/	9, 10, 11	All	H-2	H+3	ns
Delay time, CLKX low to DX valid	3		Master 42/	9, 10, 11	All	-4.0	4.0	ns
			Slave			3P+4	5P+17	
Setup time, DR valid before CLKX high	4		Master	9, 10, 11	All	12.0		ns
			Slave			2-3P		
Hold time, DR valid after CLKX high	5		Master	9, 10, 11	All	4.0		ns
			Slave			5+6P		
Disable time, high impedance following last data bit from CLKX high	6	Master 42/	9, 10, 11	All	H-2	H+3	ns	
Disable time, high impedance following last data bit from FSX high	7	Slave	9, 10, 11	All	P+3	3P+17	ns	
Delay time, FSX low to DX valid	8	Master 42/	9, 10, 11	All			ns	
		Slave			2P+2	4P+17		

McBSP TIMING as SPI MASTER or SLAVE: CLKSTP = 11b, CLKXP = 1 9/ 41/								
Hold time, FSX low after CLKX high 43/	1	See figure 5	Master 42/	9, 10, 11	All	H-2	H+3	ns
Delay time, FSX low to CLKX low 44/	2		Master 42/	9, 10, 11	All	T-2	T+2	ns
Delay time, CLKX high to DX valid	3		Master 42/	9, 10, 11	All	-4.0	4.0	ns
			Slave			3P+4	5P+17	
Setup time, DR valid before CLKX low	4		Master	9, 10, 11	All	12.0		ns
			Slave			2-3P		
Hold time, DR valid after CLKX low	5		Master	9, 10, 11	All	4.0		ns
			Slave			5+6P		
Disable time, DX high impedance following last data bit from CLKX high	6	Master 42/	9, 10, 11	All	-2.0	4.0	ns	
		Slave			3P+3	5P+17		
Delay time, FSX low to DX valid	7	Master 42/	9, 10, 11	All	L-2	L+5	ns	
		Slave			2P+2	4P+17		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions -55°C ≤ T _c ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DMAC TIMING <u>g/</u>							
Pulse duration, DMAC high	1	See figure 5	9, 10, 11	All	2P-3		ns
TIMER TIMING <u>g/</u>							
Pulse duration, TINP high	1	See figure 5	9, 10, 11	All	2P		ns
Pulse duration, TINP low	2		9, 10, 11	All	2P		ns
Pulse duration, TOUT high	3		9, 10, 11	All	2P-3		ns
Pulse duration, TOUT low	4		9, 10, 11	All	2P-3		ns
POWER-DOWN TIMING <u>g/</u>							
Pulse duration, PD high	1	See figure 5	9, 10, 11	All	2P		ns
JTAG TEST-PORT TIMING							
Cycle time, TCK	1	See figure 5	9, 10, 11	All	35.0		ns
Delay time, TCK low to TDO valid	2		9, 10, 11	All	-4.5	13.5	ns
Setup time, TDI/TMS/ $\overline{\text{TRST}}$ valid before TCK high	3		9, 10, 11	All	11.0		ns
Hold time, TDI/TMS/ $\overline{\text{TRST}}$ valid after TCK high	4		9, 10, 11	All	9.0		ns

See footnotes on next page.

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TABLE I. Electrical performance characteristics. – Continued

- 1/ V_{OH}/V_{OL} is not production tested for CLKOUT1, EMU0, and EMU1
- 2/ I_{OZL}/I_{OZH} is not production tested for TDO.
- 3/ TMS and TDI are not included due to internal pullups. \overline{TRST} is not included due to internal pulldown.
- 4/ This limit is not production tested. Measured with average activity (50%high/50%low power). The value provided is a typical value.
- 5/ Tested parameters.
- 6/ The reference points for the rise and fall transitions are measured at V_{IL} Max and V_{IH} Min.
- 7/ M = the PLL multiplier factor (x4, x6, x7, x8, x9 x10, or x11).
- 8/ C = CLKIN cycle time in ns. For example, when CLKIN frequency is 50 MHz, use C = 20 ns. The maximum CLKIN cycle time in PLL bypass mode (x1) is 200 MHz.
- 9/ P = 1/CPU clock frequency in ns.
- 10/ The reference points for the rise and fall transitions are measured at V_{OL} Max and V_{OH} Min.
- 11/ D = 8, 6, 4, or 2; FIFO clock divide ratio, user-programmable.
- 12/ To ensure data setup time, simply program the strobe width wide enough. ARDY (XRDY) is internally synchronized. If ARDY (XRDY) does meet setup or hold time, it may be recognized in the current cycle or the next cycle. Thus, ARDY (XRDY) can be asynchronous input.
- 13/ RS = Read Setup, RST = Read Strobe, RH = Read Hold, WS = Write Setup, WST = Write Strobe, WH = Write Hold. These parameters are programmed via the EMIF CE (XBUS XCE) space control registers.
- 14/ The sum of RS and RST (or WS and WST) must be minimum of 4 in order to use ARDY (XRDY) input to extend strobe width.
- 15/ Select signals include: \overline{CEx} , $\overline{BE[3:0]}$, $EA[21:2]$, \overline{AOE} , $(\overline{XCEx}, \overline{XBE[3:0]}, XA[5:2], \overline{XOE})$ and for writes, include ED[31:0] (XD[31:0]), with the exception that \overline{CEx} (\overline{XCEx}) can stay active for an additional 7P ns following the end of the cycle.
- 16/ $\overline{SDCAS}/\overline{SSADS}$, $\overline{SDRAS}/\overline{SSOE}$, and $\overline{SDWE}/\overline{SSWE}$ operate as \overline{SSADS} , \overline{SSOE} and \overline{SSWE} , respectively during SBSRAM accesses.
- 17/ For the first write in a series of one or more consecutive adjacent writes, the write data is generated one CLKOUT2 cycle early to accommodate the ED enable time.
- 18/ EMIF Bus consists of $\overline{CE[3:0]}$, $\overline{BE[3:0]}$, ED[31:0], EA[21:2], \overline{ARE} , \overline{AOE} , \overline{AWE} , $\overline{SDCAS}/\overline{SSADS}$, $\overline{SDRAS}/\overline{SSOE}$, $\overline{SDWE}/\overline{SSWE}$, and SDA10.
- 19/ All pending EMIF transactions are allowed to complete before \overline{HOLDA} is asserted. The worst case for this is an asynchronous read or write with external ARDY used or a minimum of eight consecutive SDRAM reads or writes when RBTR8 = 1. If no bus transactions are occurring, then the minimum delay time can be achieved. Also, bus hold can be indefinitely delayed by setting NOHOLD = 1.
- 20/ This parameter applies to CLKMODEx1 when CLKIN is stable, and applies to CLKMODEx4, x6, x7, x8, x9, x10, and x11 when CLKIN and PLL are stable.

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TABLE I. Electrical performance characteristics. – Continued

- 21/ This parameter applies to CLKMODE x4, x6, x7, x8, x9, x10 and x11 only (it does not apply to CLKMODE x1). The $\overline{\text{RESET}}$ signal is not connected internally to the clock PLL circuit. The PLL, however, may need up to 250 μs to stabilize following device power up or after PLL configuration has been changed. During that time, RESET must be asserted to ensure proper device operation.
- 22/ XD[31:0] are the boot configuration pins during device reset.
- 23/ High group consists of: XFCLK, $\overline{\text{HOLDA}}$
 Low group consists of: IACK, INUM[3:0], DMAC[3:0], PD, TOUT0, and TOUT1
 Z group consists of: EA[21:2], ED[31:0], CE[3:0], BE[3:0], ARE, AWE, $\overline{\text{AOE}}$, SDCAS/SSADS, SDRAS/SSOE, SDWE/SSWE, SDA10, CLKX0, CLKX1, CLKX2, FSX0, FSX1, FSX2, DX0, DX1, DX2, CLKR0, CLKR1, CLKR2, FSR0, FSR1, FSR2, XCE[3:0], XBE[3:0]/XA[5:2], XOE, XRE, XWE/XWAIT, XAS, XW/R, XRDY, XBLAST, XHOLD, and XHOLDA
- 24/ $\overline{\text{XBE}}[3:0]/\text{XA}[5:2]$ operate as address signals XA[5:2] during synchronous FIFO accesses.
- 25/ $\overline{\text{XWE}}/\overline{\text{XWAIT}}$ operates as the write-enable signal $\overline{\text{XWE}}$ during synchronous FIFO accesses.
- 26/ FIFO read (glueless) mode only available in XCE3.
- 27/ XW/R input/output polarity selected at boot.
- 28/ XBLAST input polarity selected at boot.
- 29/ $\overline{\text{XBE}}[3:0]/\text{XA}[5:2]$ operate as byte-enables $\overline{\text{XBE}}[3:0]$ during host-port accesses.
- 30/ XRDY operates as active-low ready input/output during host-port accesses.
- 31/ XBLAST output polarity is always active low.
- 32/ $\overline{\text{XWE}}/\overline{\text{XWAIT}}$ operates as XWAIT output signal during host-port accesses.
- 33/ Expansion bus select signals include XCNTL and XR/W.
- 34/ XBus consists of $\overline{\text{XBE}}[3:0]/\text{XA}[5:2]$, $\overline{\text{XAS}}$, XW/R, and XBLAST.
- 35/ All pending XBus transactions are allowed to complete before XHOLDA is asserted.
- 36/ CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
- 37/ Minimum delay times also represent minimum output hold times

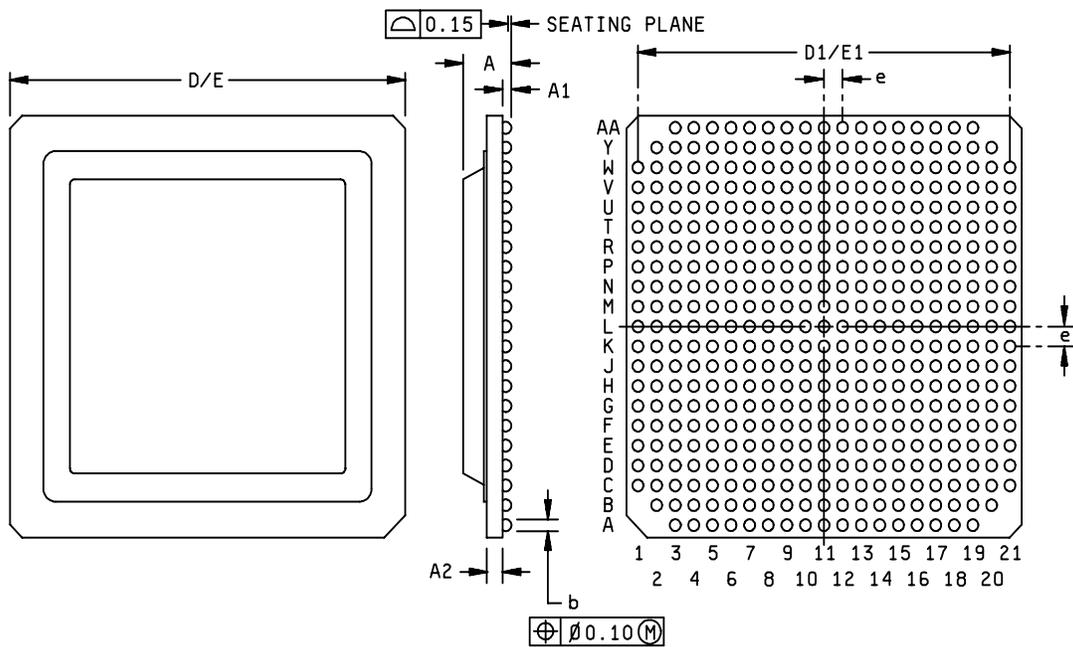
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TABLE I. Electrical performance characteristics. – Continued

- 38/ The maximum bit rate for this device is 100 Mbps or CPU/2 (the slower of the two). The maximum bit rate for McBSP-to-McBSP communications is 100 MHz; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 10 ns (100 MHz), whichever value is larger. For example, when running parts at 300 MHz (P = 3.3 ns), use 10 ns as the minimum CLKR/X cycle (by setting the appropriate CLKGDV ratio of external clock source). When running parts at 100 MHz (P = 10 ns), use 2P = 20 ns (50 MHz) as the minimum CLKR/X clock cycle. The maximum bit rate for McBSP-to-McBSP communications applies when the serial port is a master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.
- 39/ C = H or L
 S = sample rate generator input clock = P if CLKSM = 1 (P = 1/CPU clock frequency)
 = sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
 H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
 = (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
 L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
 = (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
 CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the 100-MHz limit.
- 40/ The minimum CLKR/X pulse duration is either (P-1) or 4 ns, whichever is larger. For example, when running parts at 300 MHz (P = 3.3 ns), use 4 ns as the minimum CLKR/X pulse duration. When running parts at 100 MHz (P = 10 ns), use (P-1) = 9 ns as the minimum CLKR/X pulse duration.
- 41/ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
- 42/ T = CLKX period = (1 + CLKGDV) * S.
 S = sample rate generator input clock = P if CLKSM = 1 (P = 1/CPU clock frequency)
 = sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
 L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even.
 = (CLKGDV + 1)/2 * S if CLKGDV is odd or zero.
 H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even.
 = (CLKGDV + 1)/2 * S if CLKGDV is odd or zero.
 CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the 100 MHz limit.
- 43/ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
 CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP.
 CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP.
- 44/ FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

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CASE X



Case outline Symbol	X Millimeters	
	Min	Max
A		3.30
A1	0.50	0.70
A2	1.00	1.22
b	0.60	0.90
D/E	26.80	27.20
D1/E1	25.40 BSC	
e	1.27 BSC	

NOTE: All dimensions are in Millimeters.

FIGURE 1. Case outline.

<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000</p>	<p align="center">SIZE A</p>		<p align="center">5962-00510</p>
		<p align="center">REVISION LEVEL</p>	<p align="center">SHEET 26</p>

Case outline	X				
Symbol number	Pin Symbol	Type	Symbol number	Pin Symbol	Type
D10	CLKIN	I	R15	<u>BE3</u>	O
C12	CLKMODE0	I	U18	<u>CE0</u>	O
G10	CLKMODE1	I	T15	<u>CE1</u>	O
G12	CLKMODE2	I	W18	<u>CE2</u>	O
Y17	CLKOUT1	O	V18	<u>CE3</u>	O
L1	CLKR0	I/O	V14	ED0	I/O
H2	CLKR1	I/O	R13	ED1	I/O
M2	CLKR2	I/O	Y15	ED2	I/O
K6	CLKS0	I	T13	ED3	I/O
G2	CLKS1	I	Y14	ED4	I/O
L4	CLKS2	I	Y13	ED5	I/O
K3	CLKX0	I/O	V13	ED6	I/O
H4	CLKX1	I/O	R12	ED7	I/O
N4	CLKX2	I/O	AA13	ED8	I/O
V4	DMAC0	O	T12	ED9	I/O
T6	DMAC1	O	Y12	ED10	I/O
U2	DMAC2	O	Y11	ED11	I/O
R6	DMAC3	O	W12	ED12	I/O
M1	DR0	I	W10	ED13	I/O
J2	DR1	I	AA10	ED14	I/O
P3	DR2	I	T11	ED15	I/O
L6	DX0	O	V10	ED16	I/O
H3	DX1	O	W9	ED17	I/O
N2	DX2	O	Y10	ED18	I/O
T18	EA2	O	T10	ED19	I/O
P20	EA3	O	V9	ED20	I/O
N16	EA4	O	AA9	ED21	I/O
N21	EA5	O	Y9	ED22	I/O
M21	EA6	O	V8	ED23	I/O
R18	EA7	O	AA8	ED24	I/O
M16	EA8	O	T9	ED25	I/O
M20	EA9	O	V7	ED26	I/O
N18	EA10	O	Y8	ED27	I/O
L21	EA11	O	Y7	ED28	I/O
M18	EA12	O	T8	ED29	I/O
K21	EA13	O	Y6	ED30	I/O
L16	EA14	O	V6	ED31	I/O
M19	EA15	O	T19	<u>HOLD</u>	I
K20	EA16	O	T16	HOLDA	O
J21	EA17	O	Y5	EMU0	I/O
K19	EA18	O	T7	EMU1	I/O
J20	EA19	O	T14	<u>SDA10</u>	O
K16	EA20	O	V17	<u>SDCAS/SSADS</u>	O
K18	EA21	O	W17	<u>SDRAS/SSOE</u>	O
P16	<u>AOE</u>	O	W15	<u>SDWE/SSWE</u>	O
R16	ARDY	I	L2	FSR0	I/O
T20	<u>ARE</u>	O	J6	FSR1	I/O
R20	<u>AWE</u>	O	M6	FSR2	I/O
V16	<u>BE0</u>	O	L3	FSX0	I/O
U20	<u>BE1</u>	O	J1	FSX1	I/O
V19	<u>BE2</u>	O	N1	FSX2	I/O

I = Input, O = Output, S = Supply voltage, GND = Ground.

FIGURE 2. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
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Case outline	X				
Symbol number	Pin Symbol	Type	Symbol number	Pin Symbol	Type
T3	EXT_INT4	I	J18	XD2	I/O
T2	EXT_INT5	I	G20	XD3	I/O
P6	EXT_INT6	I	H19	XD4	I/O
R4	EXT_INT7	I	G16	XD5	I/O
R2	IACK	O	E20	XD6	I/O
N6	INUM0	O	F19	XD7	I/O
P2	INUM1	O	F16	XD8	I/O
P1	INUM2	O	D19	XD9	I/O
P4	INUM3	O	G15	XD10	I/O
G11	PLL \overline{F}	A	D18	XD11	I/O
K2	NMI	I	E18	XD12	I/O
V3	PD	O	C18	XD13	I/O
A10	RSV2	I	D17	XD14	I/O
D9	RSV4	O	G14	XD15	I/O
J4	RESET	I	C17	XD16	I/O
F3	RSV1	I	F15	XD17	I/O
Y16	CLKOUT2	O	D14	XD18	I/O
V5	TCK	I	B17	XD19	I/O
W4	TDI	I	B16	XD20	I/O
R8	TDO	O	D13	XD21	I/O
K1	RSV0	I	C15	XD22	I/O
E2	TINP0	I	B15	XD23	I/O
H6	TINP1	I	F13	XD24	I/O
W5	TMS	I	B14	XD25	I/O
F2	TOUT0	O	A14	XD26	I/O
G4	TOUT1	O	D12	XD27	I/O
R7	TRST	I	C13	XD28	I/O
F11	RSV3	O	F12	XD29	I/O
B11	PLL \overline{V}	A	B13	XD30	I/O
A11	PLL \overline{G}	A	D11	XD31	I/O
G9	XAS	I/O	C4	XHOLD	I/O
C7	XBE0/XA2	I/O	D6	XHOLDA	I/O
B5	XBE1/XA3	I/O	B7	XOE	O
F7	XBE2/XA4	I/O	F4	XRDY	I/O
F6	XBE3/XA5	I/O	B8	XRE	O
C5	XBLAST	I/O	D7	XWE/XWAIT	O
C10	XBOFF	I	F9	XW/R	I/O
E4	XCE0	O	R11	NC	no
D4	XCE1	O	R9	NC	no
G6	XCE2	O	W7	NC	no
D3	XCE3	O	A3	CV \overline{DD} -1.5V	PS1
C9	XCLKIN	I	A5	CV \overline{DD} -1.5V	PS1
B9	XFCLK	O	A7	CV \overline{DD} -1.5V	PS1
A9	XCNTL	I	A12	CV \overline{DD} -1.5V	PS1
D8	XCS	I	A13	CV \overline{DD} -1.5V	PS1
H21	XD0	I/O	A16	CV \overline{DD} -1.5V	PS1
H20	XD1	I/O	A18	CV \overline{DD} -1.5V	PS1

I = Input, O = Output, GND = Ground, NC = No connection

PPLV and PLLG signals are not part of external voltage supply or ground. See the CLOCK/PLL documentation for information on how to connect those pins. A = Analog Signal (PLL Filter).

FIGURE 2. Terminal connections. - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
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Case outline	X				
Symbol number	Pin Symbol	Type	Symbol number	Pin Symbol	Type
B2	CV _{DD} -1.5V	PS1	P17	CV _{DD} -1.5V	PS1
B4	CV _{DD} -1.5V	PS1	P18	CV _{DD} -1.5V	PS1
B6	CV _{DD} -1.5V	PS1	P19	CV _{DD} -1.5V	PS1
B10	CV _{DD} -1.5V	PS1	R10	CV _{DD} -1.5V	PS1
B12	CV _{DD} -1.5V	PS1	R14	CV _{DD} -1.5V	PS1
B19	CV _{DD} -1.5V	PS1	R21	CV _{DD} -1.5V	PS1
C1	CV _{DD} -1.5V	PS1	T1	CV _{DD} -1.5V	PS1
C3	CV _{DD} -1.5V	PS1	T5	CV _{DD} -1.5V	PS1
C20	CV _{DD} -1.5V	PS1	T17	CV _{DD} -1.5V	PS1
D2	CV _{DD} -1.5V	PS1	U4	CV _{DD} -1.5V	PS1
D15	CV _{DD} -1.5V	PS1	U6	CV _{DD} -1.5V	PS1
D16	CV _{DD} -1.5V	PS1	U8	CV _{DD} -1.5V	PS1
D21	CV _{DD} -1.5V	PS1	U10	CV _{DD} -1.5V	PS1
E1	CV _{DD} -1.5V	PS1	U12	CV _{DD} -1.5V	PS1
E6	CV _{DD} -1.5V	PS1	U14	CV _{DD} -1.5V	PS1
E8	CV _{DD} -1.5V	PS1	U16	CV _{DD} -1.5V	PS1
E10	CV _{DD} -1.5V	PS1	U21	CV _{DD} -1.5V	PS1
E12	CV _{DD} -1.5V	PS1	V1	CV _{DD} -1.5V	PS1
E14	CV _{DD} -1.5V	PS1	V11	CV _{DD} -1.5V	PS1
E16	CV _{DD} -1.5V	PS1	V12	CV _{DD} -1.5V	PS1
F5	CV _{DD} -1.5V	PS1	V15	CV _{DD} -1.5V	PS1
F8	CV _{DD} -1.5V	PS1	V20	CV _{DD} -1.5V	PS1
F10	CV _{DD} -1.5V	PS1	W2	CV _{DD} -1.5V	PS1
F14	CV _{DD} -1.5V	PS1	W13	CV _{DD} -1.5V	PS1
F17	CV _{DD} -1.5V	PS1	W19	CV _{DD} -1.5V	PS1
F20	CV _{DD} -1.5V	PS1	W21	CV _{DD} -1.5V	PS1
F21	CV _{DD} -1.5V	PS1	Y3	CV _{DD} -1.5V	PS1
G1	CV _{DD} -1.5V	PS1	Y18	CV _{DD} -1.5V	PS1
G7	CV _{DD} -1.5V	PS1	Y20	CV _{DD} -1.5V	PS1
G8	CV _{DD} -1.5V	PS1	AA4	CV _{DD} -1.5V	PS1
G13	CV _{DD} -1.5V	PS1	AA6	CV _{DD} -1.5V	PS1
G18	CV _{DD} -1.5V	PS1	AA11	CV _{DD} -1.5V	PS1
H5	CV _{DD} -1.5V	PS1	AA12	CV _{DD} -1.5V	PS1
H16	CV _{DD} -1.5V	PS1	AA15	CV _{DD} -1.5V	PS1
H17	CV _{DD} -1.5V	PS1	AA17	CV _{DD} -1.5V	PS1
H18	CV _{DD} -1.5V	PS1	AA19	CV _{DD} -1.5V	PS1
K4	CV _{DD} -1.5V	PS1	C8	DV _{DD} -3.3V	PS2
K5	CV _{DD} -1.5V	PS1	C14	DV _{DD} -3.3V	PS2
K17	CV _{DD} -1.5V	PS1	E3	DV _{DD} -3.3V	PS2
L18	CV _{DD} -1.5V	PS1	E19	DV _{DD} -3.3V	PS2
L19	CV _{DD} -1.5V	PS1	H9	DV _{DD} -3.3V	PS2
L20	CV _{DD} -1.5V	PS1	H11	DV _{DD} -3.3V	PS2
M3	CV _{DD} -1.5V	PS1	H13	DV _{DD} -3.3V	PS2
M4	CV _{DD} -1.5V	PS1	J3	DV _{DD} -3.3V	PS2
M5	CV _{DD} -1.5V	PS1	J8	DV _{DD} -3.3V	PS2
M17	CV _{DD} -1.5V	PS1	J10	DV _{DD} -3.3V	PS2
N20	CV _{DD} -1.5V	PS1	J12	DV _{DD} -3.3V	PS2
P5	CV _{DD} -1.5V	PS1	J14	DV _{DD} -3.3V	PS2

I = Input, O = Output, GND = Ground

FIGURE 2. Terminal connections - Continued

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Case outline	X				
Symbol number	Pin Symbol	Type	Symbol number	Pin Symbol	Type
J19	DV _{DD} -3.3V	PS2	E13	GND	GND
K7	DV _{DD} -3.3V	PS2	E15	GND	GND
K9	DV _{DD} -3.3V	PS2	E17	GND	GND
K11	DV _{DD} -3.3V	PS2	E21	GND	GND
K13	DV _{DD} -3.3V	PS2	F1	GND	GND
K15	DV _{DD} -3.3V	PS2	F18	GND	GND
L8	DV _{DD} -3.3V	PS2	G3	GND	GND
L10	DV _{DD} -3.3V	PS2	G5	GND	GND
L12	DV _{DD} -3.3V	PS2	G17	GND	GND
L14	DV _{DD} -3.3V	PS2	G19	GND	GND
M7	DV _{DD} -3.3V	PS2	G21	GND	GND
M9	DV _{DD} -3.3V	PS2	H1	GND	GND
M11	DV _{DD} -3.3V	PS2	H7	GND	GND
M13	DV _{DD} -3.3V	PS2	H8	GND	GND
M15	DV _{DD} -3.3V	PS2	H10	GND	GND
N3	DV _{DD} -3.3V	PS2	H12	GND	GND
N8	DV _{DD} -3.3V	PS2	H14	GND	GND
N10	DV _{DD} -3.3V	PS2	H15	GND	GND
N12	DV _{DD} -3.3V	PS2	J5	GND	GND
N14	DV _{DD} -3.3V	PS2	J7	GND	GND
N19	DV _{DD} -3.3V	PS2	J9	GND	GND
P9	DV _{DD} -3.3V	PS2	J11	GND	GND
P11	DV _{DD} -3.3V	PS2	J13	GND	GND
P13	DV _{DD} -3.3V	PS2	J15	GND	GND
U3	DV _{DD} -3.3V	PS2	J16	GND	GND
U19	DV _{DD} -3.3V	PS2	J17	GND	GND
W8	DV _{DD} -3.3V	PS2	K8	GND	GND
W14	DV _{DD} -3.3V	PS2	K10	GND	GND
A4	GND	GND	K12	GND	GND
A6	GND	GND	K14	GND	GND
A8	GND	GND	L5	GND	GND
A15	GND	GND	L7	GND	GND
A17	GND	GND	L9	GND	GND
A19	GND	GND	L11	GND	GND
B3	GND	GND	L13	GND	GND
B18	GND	GND	L15	GND	GND
B20	GND	GND	L17	GND	GND
C2	GND	GND	M8	GND	GND
C6	GND	GND	M10	GND	GND
C11	GND	GND	M12	GND	GND
C16	GND	GND	M14	GND	GND
C19	GND	GND	N5	GND	GND
C21	GND	GND	N7	GND	GND
D1	GND	GND	N9	GND	GND
D5	GND	GND	N11	GND	GND
D20	GND	GND	N13	GND	GND
E5	GND	GND	N15	GND	GND
E7	GND	GND	N17	GND	GND
E9	GND	GND	P7	GND	GND
E11	GND	GND	P8	GND	GND

I = Input, O = Output, GND = Ground

FIGURE 2. Terminal connections - Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
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Case outline	X	
Symbol number	Pin Symbol	Type
P10	GND	GND
P12	GND	GND
P14	GND	GND
P15	GND	GND
P21	GND	GND
R1	GND	GND
R3	GND	GND
R5	GND	GND
R17	GND	GND
R19	GND	GND
T4	GND	GND
T21	GND	GND
U1	GND	GND
U5	GND	GND
U7	GND	GND
U9	GND	GND
U11	GND	GND
U13	GND	GND
U15	GND	GND
U17	GND	GND
V2	GND	GND
V21	GND	GND
W1	GND	GND
W3	GND	GND
W6	GND	GND
W11	GND	GND
W16	GND	GND
W20	GND	GND
Y2	GND	GND
Y4	GND	GND
Y19	GND	GND
AA3	GND	GND
AA5	GND	GND
AA7	GND	GND
AA14	GND	GND
AA16	GND	GND
AA18	GND	GND

I = Input, O = Output, GND = Ground.

FIGURE 2. Terminal connections - Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
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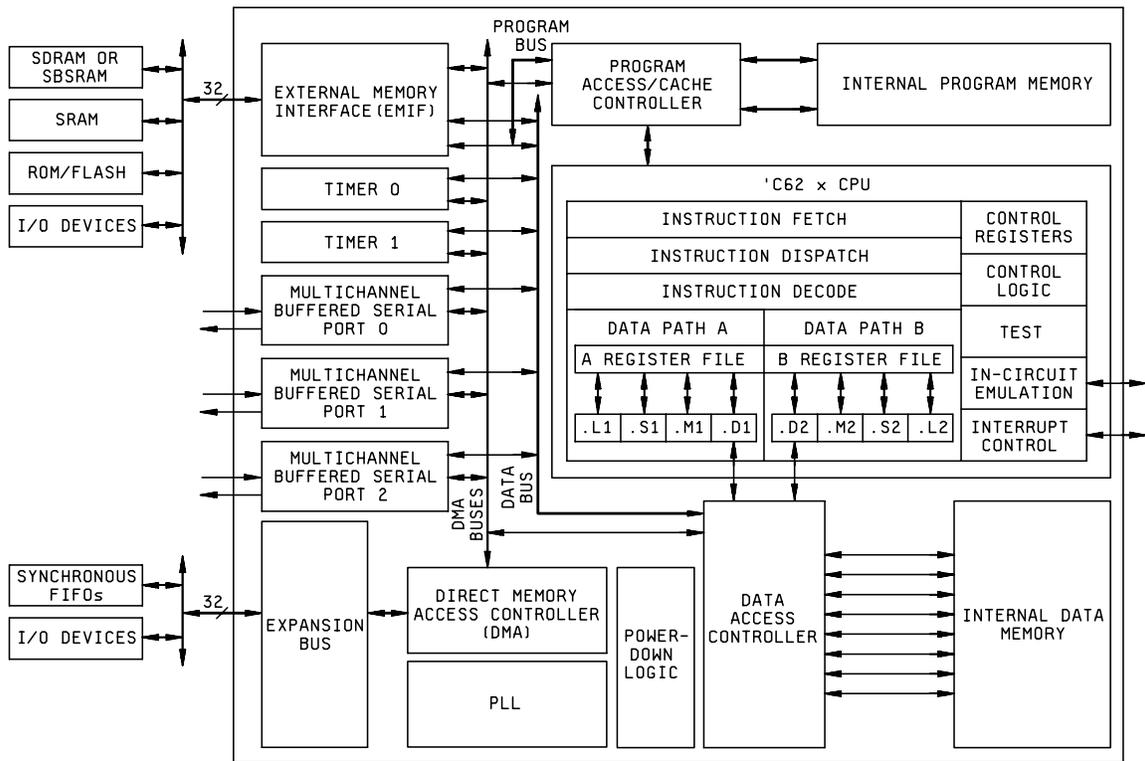
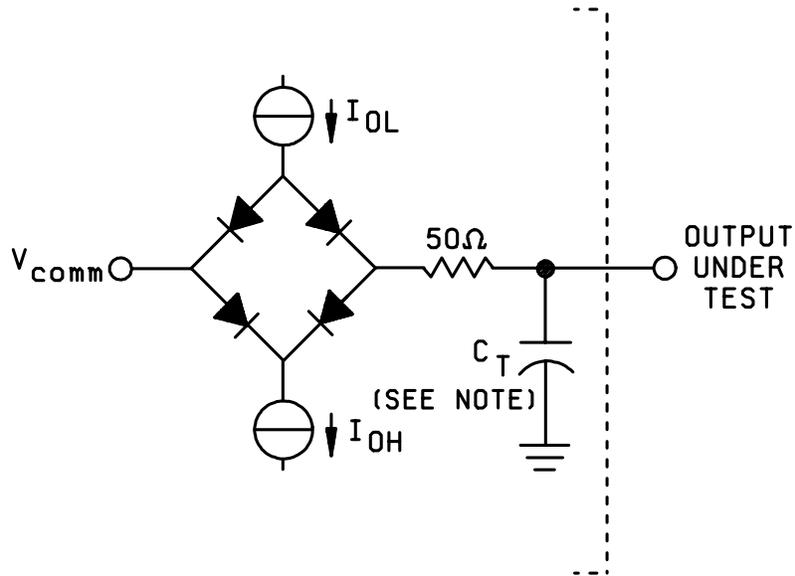


FIGURE 3. Block diagram.

Instruction name	Instruction code
IDCODE	0100
INT_SCAN	0111
EXTEST	0000
SAMPLE	0001
BYPASS	1111

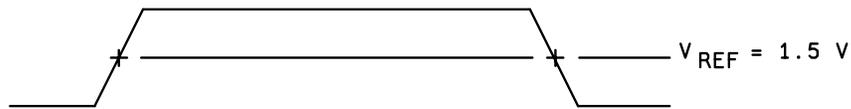
FIGURE 4. Boundry scan instruction codes.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
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TEST LOAD CIRCUIT FOR AC TIMING MEASUREMENTS

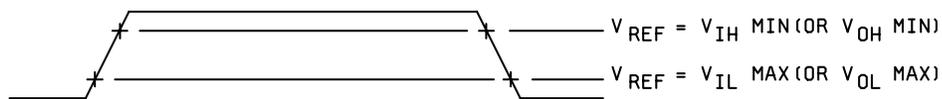
$I_{OL} = 2 \text{ mA}$
 $I_{OH} = 2 \text{ mA}$
 $V_{COMM} = 2.1 \text{ V}$
 $C_T = 15\text{-}30 \text{ pF}$ typical load-circuit capacitance



INPUT AND OUTPUT VOLTAGE REFERENCE LEVELS FOR AC TIMING MEASUREMENTS

NOTE:

All input and output timing parameters are referenced to 1.5 V for both "0" and "1" logic levels.



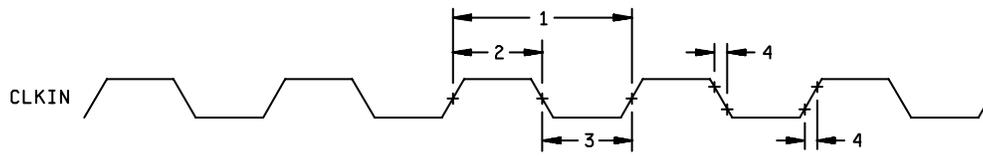
RISE AND FALL TRANSITION TIME VOLTAGE REFERENCE LEVELS

NOTE:

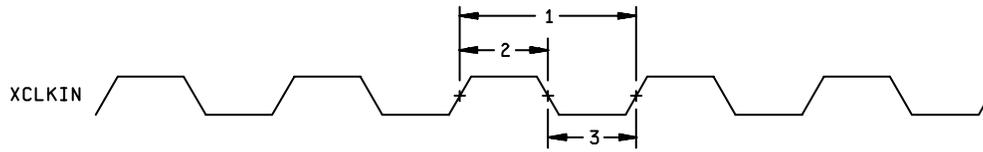
All rise and fall transition timing parameters are referenced to $V_{IL} \text{ max}$ and $V_{IH} \text{ min}$ for input clocks and $V_{OL} \text{ max}$ and $V_{OH} \text{ min}$ for output clocks.

FIGURE 5. Timing waveforms.

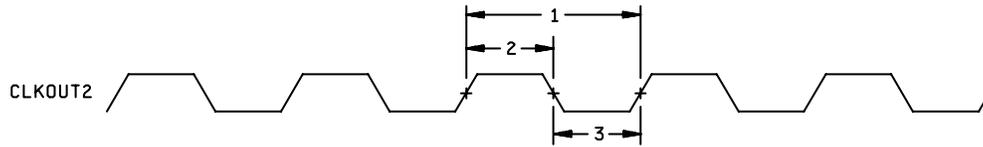
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
		REVISION LEVEL	SHEET 33



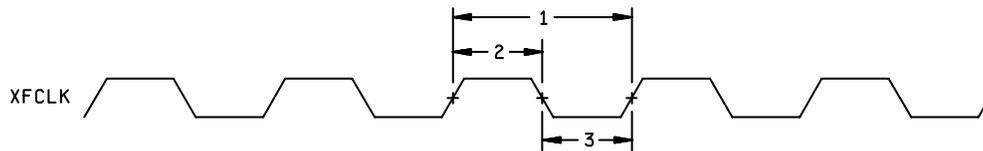
CLKIN TIMINGS



XCLKIN TIMINGS



CLKOUT2 TIMINGS



XFCLK TIMINGS

FIGURE 5. Timing waveforms. - Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
		REVISION LEVEL	SHEET 34

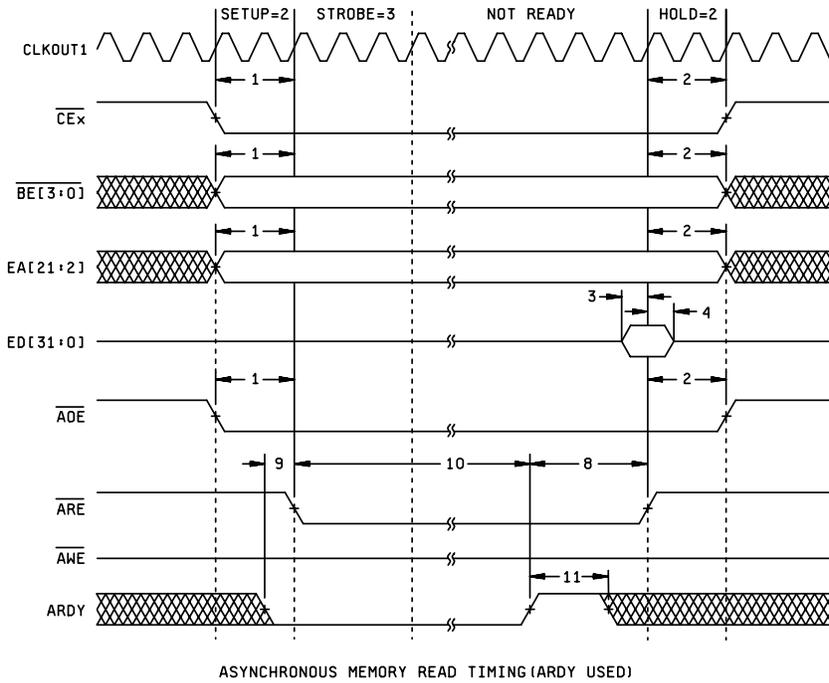
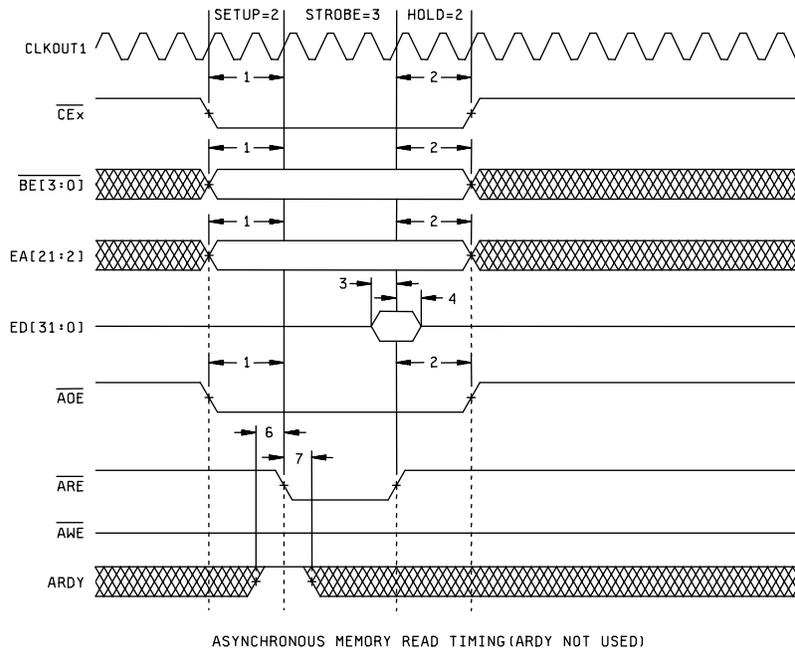
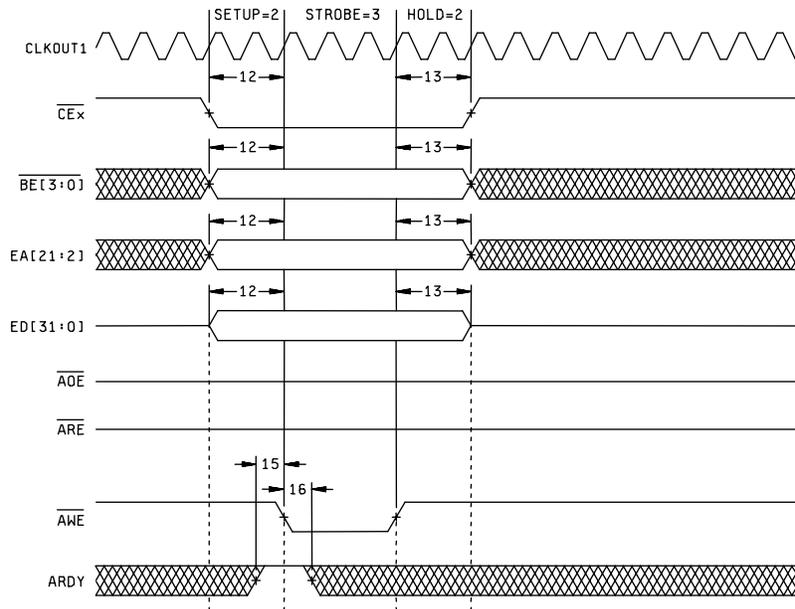
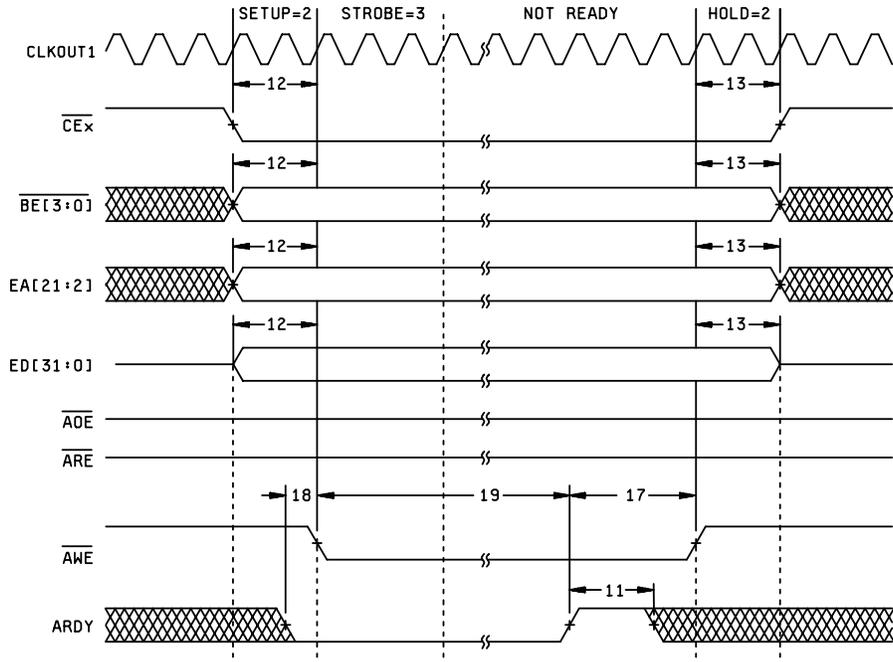


FIGURE. 5. Timing waveforms. - Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
		REVISION LEVEL	SHEET 35



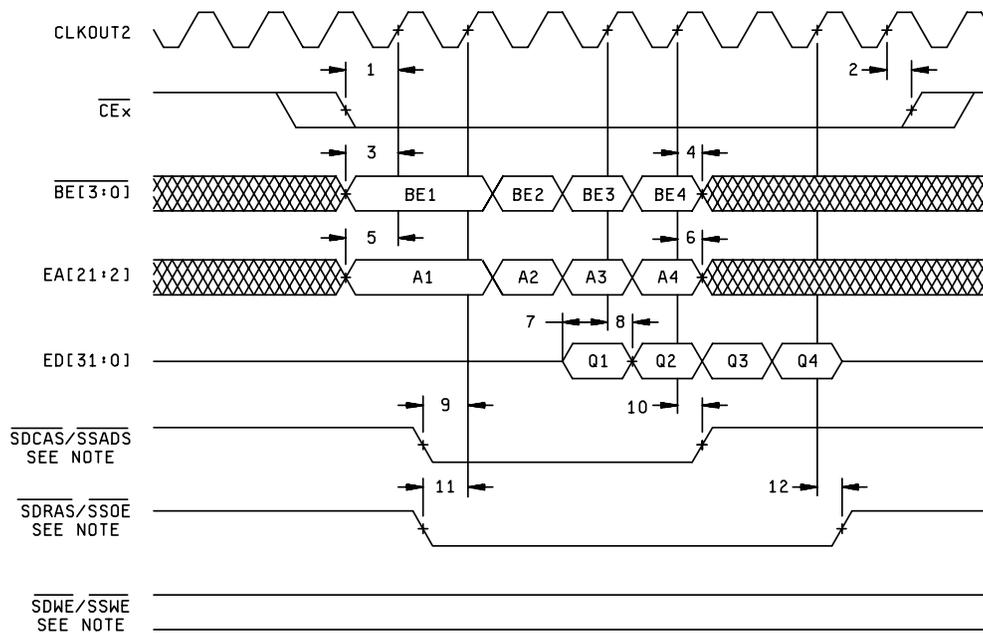
ASYNCHRONOUS MEMORY WRITE TIMING (ARDY NOT USED)



ASYNCHRONOUS MEMORY WRITE TIMING (ARDY USED)

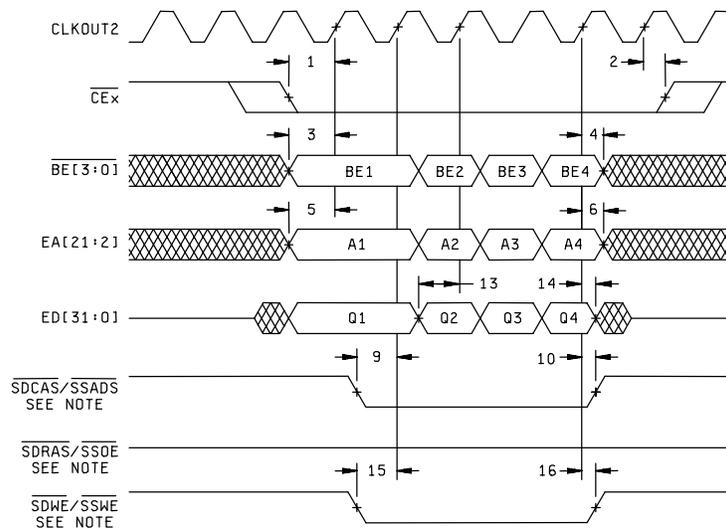
FIGURE 5. Timing waveforms. - Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
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SBSRAM READ TIMING

SDCAS/SSADS, SDRAS/SSOE, and SDWE/SSWE operate as SSADS, SSOE and SSWE, respectively during SBSRAM accesses.

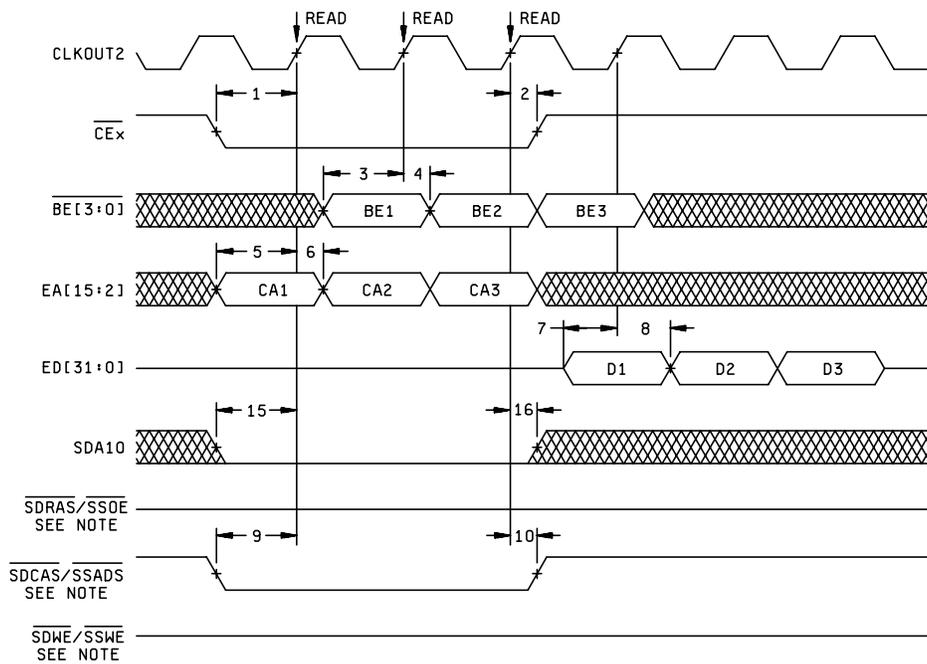


SBSRAM WRITE TIMING

SDCAS/SSADS, SDRAS/SSOE, and SDWE/SSWE operate as SSADS, SSOE and SSWE, respectively during SBSRAM accesses.

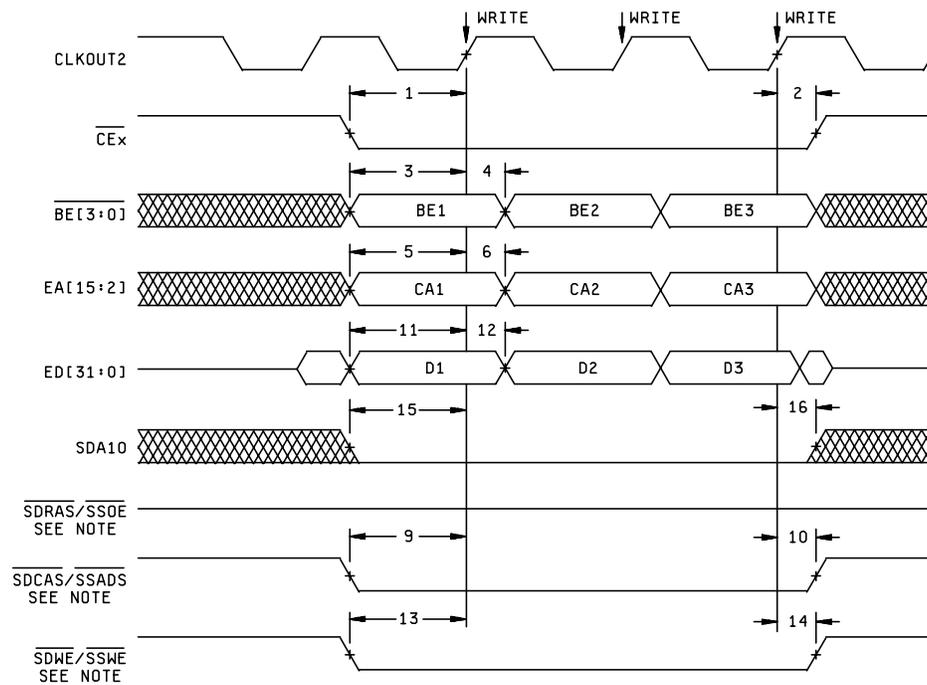
FIGURE 5. Timing waveforms. - Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
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THREE SDRAM READ COMMANDS

$\overline{\text{SDCAS}}/\overline{\text{SSADS}}$, $\overline{\text{SDRAS}}/\overline{\text{SSOE}}$, and $\overline{\text{SDWE}}/\overline{\text{SSWE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDRAS}}$ and $\overline{\text{SDWE}}$, respectively during SDRAM accesses.

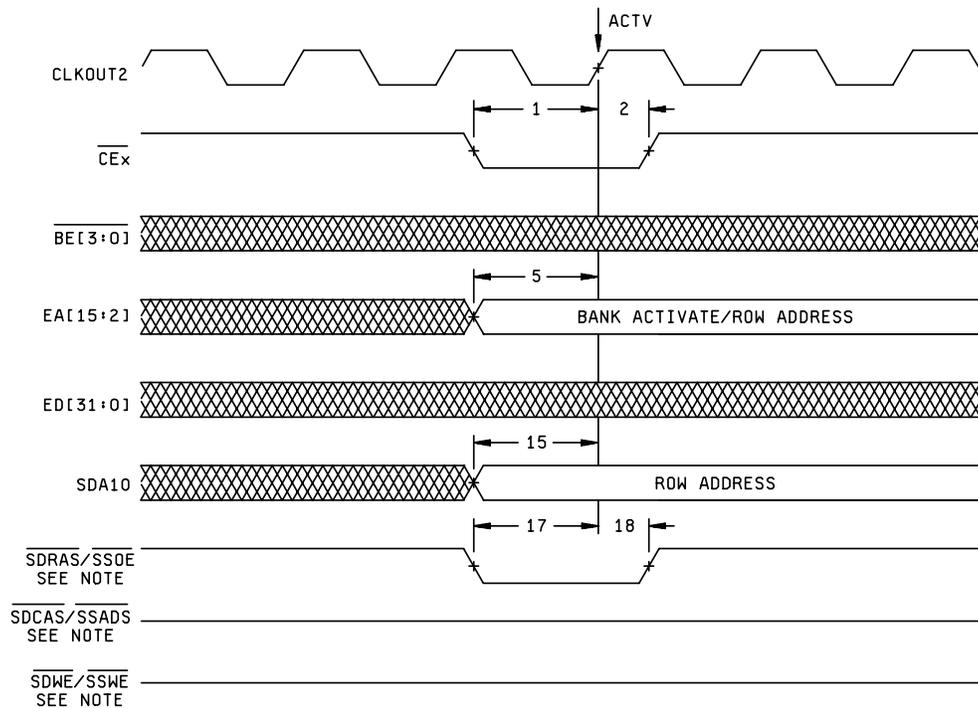


THREE SDRAM WRT COMMANDS

$\overline{\text{SDCAS}}/\overline{\text{SSADS}}$, $\overline{\text{SDRAS}}/\overline{\text{SSOE}}$, and $\overline{\text{SDWE}}/\overline{\text{SSWE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDRAS}}$ and $\overline{\text{SDWE}}$, respectively during SDRAM accesses.

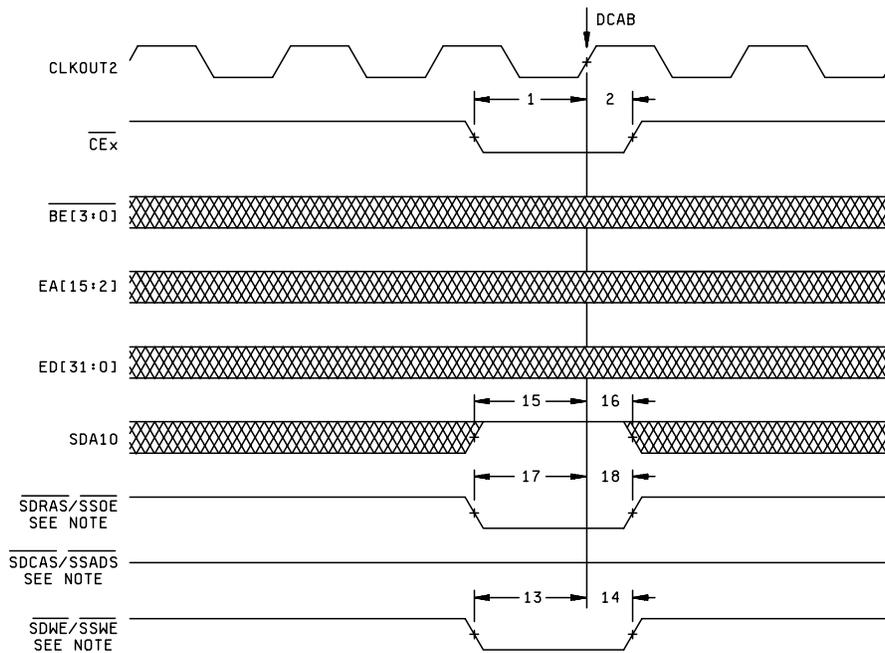
FIGURE 5. Timing waveforms. - Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
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SDRAM ACTV COMMAND

$\overline{SDCAS}/\overline{SSADS}$, $\overline{SDRAS}/\overline{SSOE}$, and $\overline{SDWE}/\overline{SSWE}$ operate as \overline{SDCAS} , \overline{SDRAS} and \overline{SDWE} , respectively during SDRAM accesses.

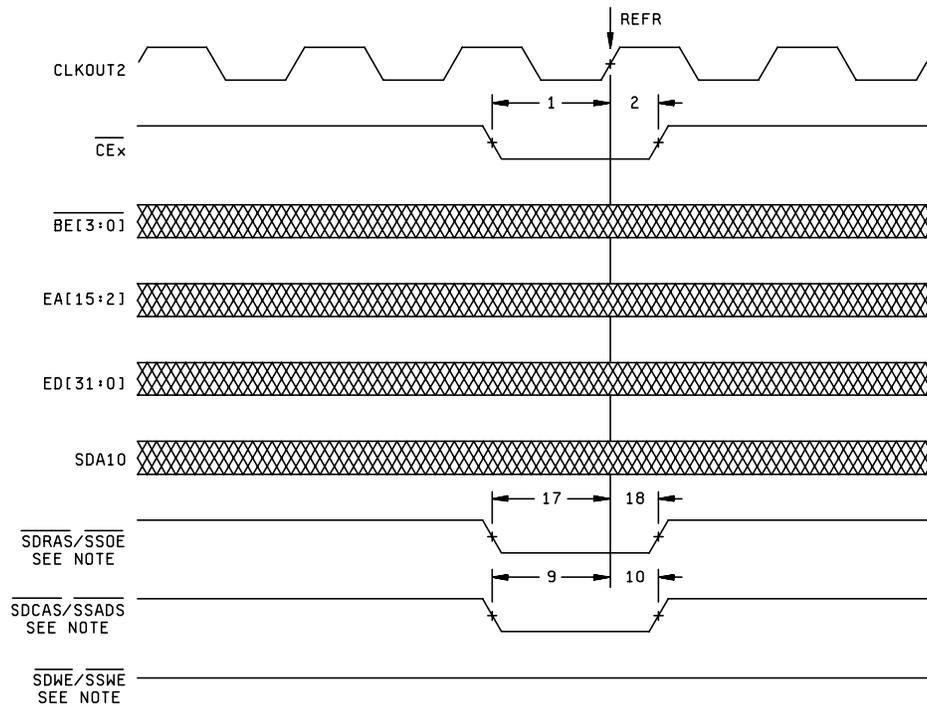


SDRAM DCAB COMMAND

$\overline{SDCAS}/\overline{SSADS}$, $\overline{SDRAS}/\overline{SSOE}$, and $\overline{SDWE}/\overline{SSWE}$ operate as \overline{SDCAS} , \overline{SDRAS} and \overline{SDWE} , respectively during SDRAM accesses.

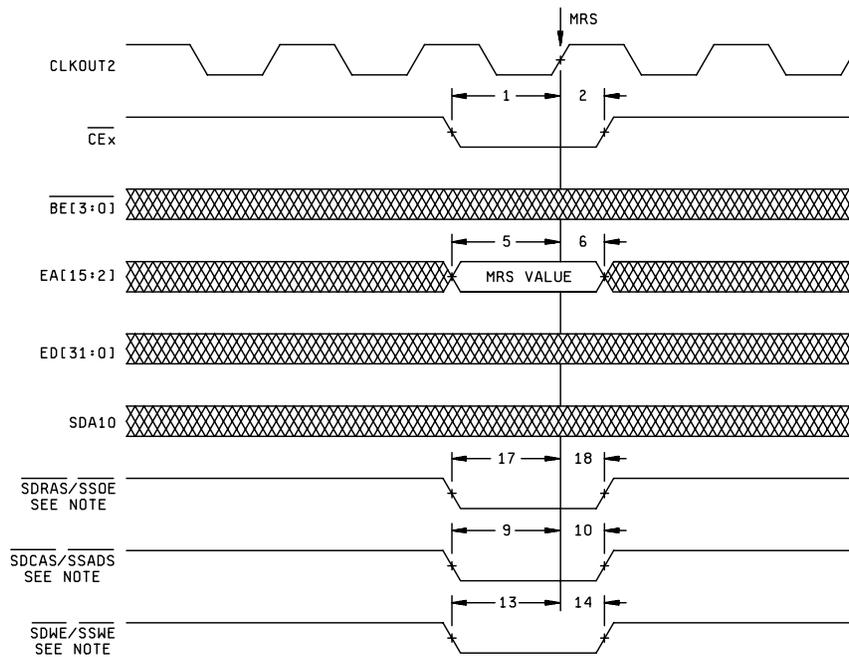
FIGURE 5. Timing waveforms. - Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
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SDRAM REF COMMAND

$\overline{\text{SDCAS}}/\overline{\text{SSADS}}$, $\overline{\text{SDRAS}}/\overline{\text{SSOE}}$, and $\overline{\text{SDWE}}/\overline{\text{SSWE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDRAS}}$ and $\overline{\text{SDWE}}$, respectively during SDRAM accesses.

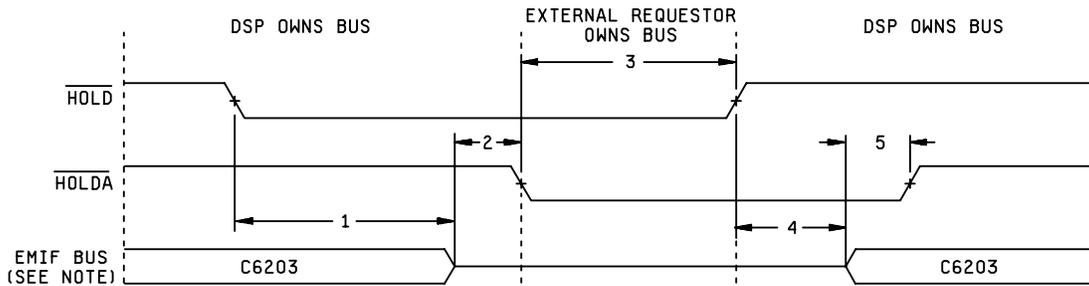


SDRAM MRS COMMAND

$\overline{\text{SDCAS}}/\overline{\text{SSADS}}$, $\overline{\text{SDRAS}}/\overline{\text{SSOE}}$, and $\overline{\text{SDWE}}/\overline{\text{SSWE}}$ operate as $\overline{\text{SDCAS}}$, $\overline{\text{SDRAS}}$ and $\overline{\text{SDWE}}$, respectively during SDRAM accesses.

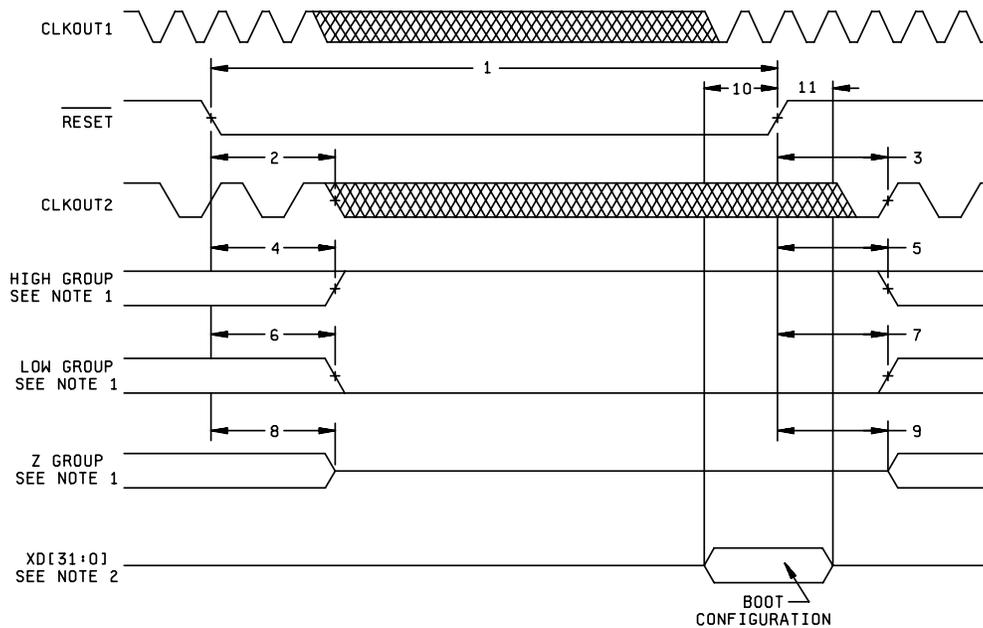
FIGURE 5. Timing waveforms. - Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
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HOLD/HOLDA TIMING

EMIF Bus consists of CE[3:0], BE[3:0], ED[31:0], EA[21:2], ARE, AOE, AWE, SDCAS/SSADS, SDRAS/SSOE, SDWE/SSWE, and SDA10.

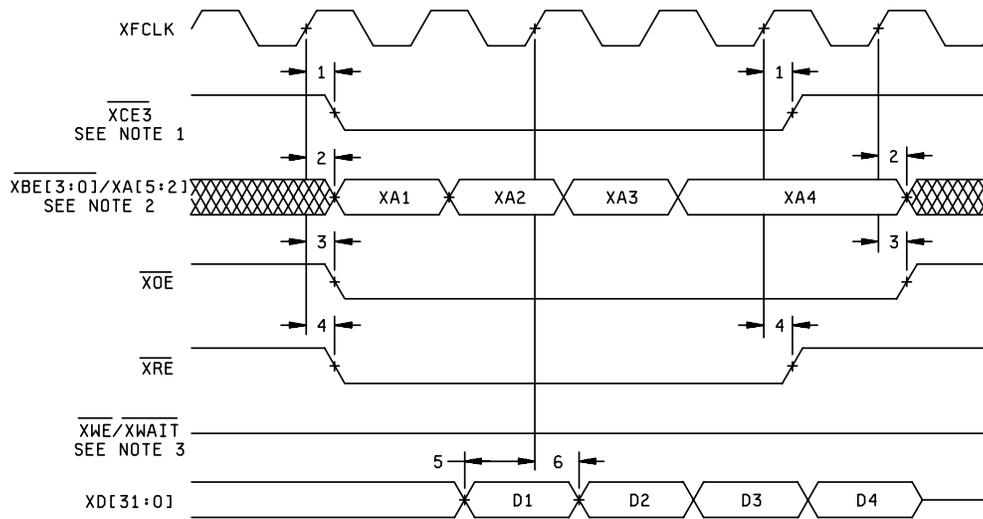
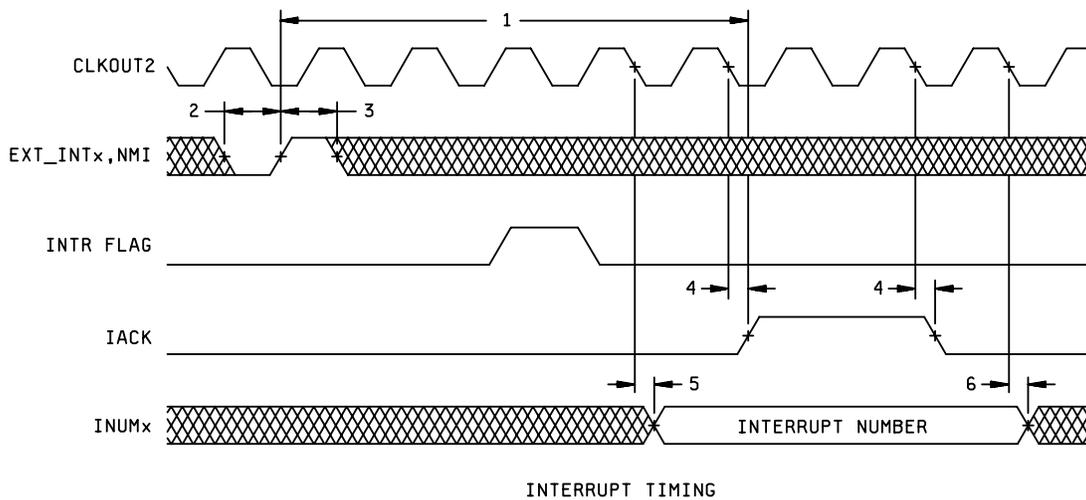


RESET TIMING

1. High group consists of: XFCLK, HOLDA
 Low group consists of: IACK, INUM[3:0], DMAC[3:0], PD, TOUT0, and TOUT1
 Z group consists of: EA[21:2], ED[31:0], CE[3:0], BE[3:0], ARE, AWE, AOE, SDCAS/SSADS, SDRAS/SSOE, SDWE/SSWE, SDA10, CLKX0, CLKX1, CLKX2, FSX0, FSX1, FSX2, DX0, DX1, DX2, CLKR0, CLKR1, CLKR2, FSR0, FSR1, FSR2, XCE[3:0], XBE[3:0]/XA[5:2], XOE, XRE, XWE/XWAIT, XAS, XW/R, XRDY, XBLAST, XHOLD, and XHOLDA
2. XD[31:0] are the boot configuration pins during device reset.

FIGURE 5. Timing waveforms. - Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
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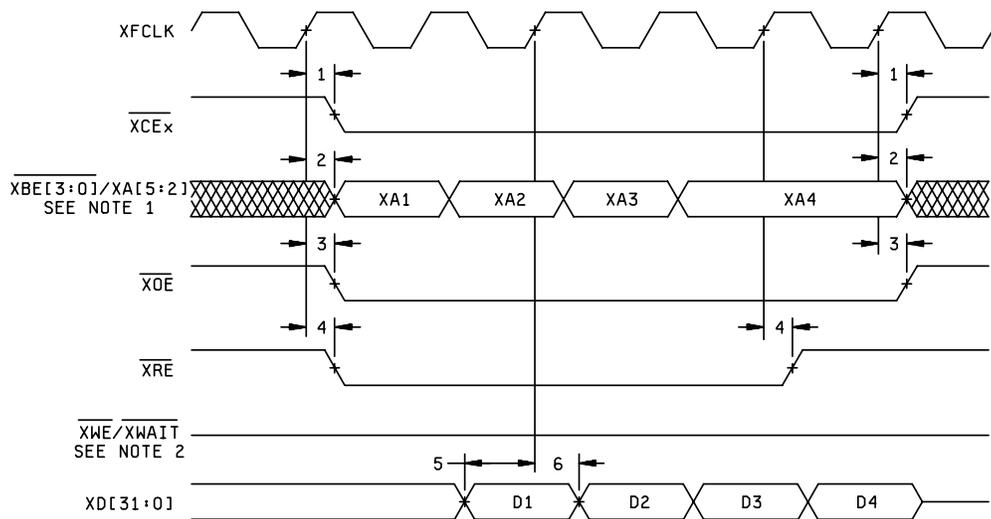


FIFO READ TIMING (GLUELESS READ MODE)

1. FIFO read (glueless) mode only available in XCE3.
2. XBE[3:0]/XA[5:2] operate as address signals XA[5:2] during synchronous FIFO accesses.
3. XWE/XWAIT operates as the write-enable signal XWE during synchronous FIFO accesses.

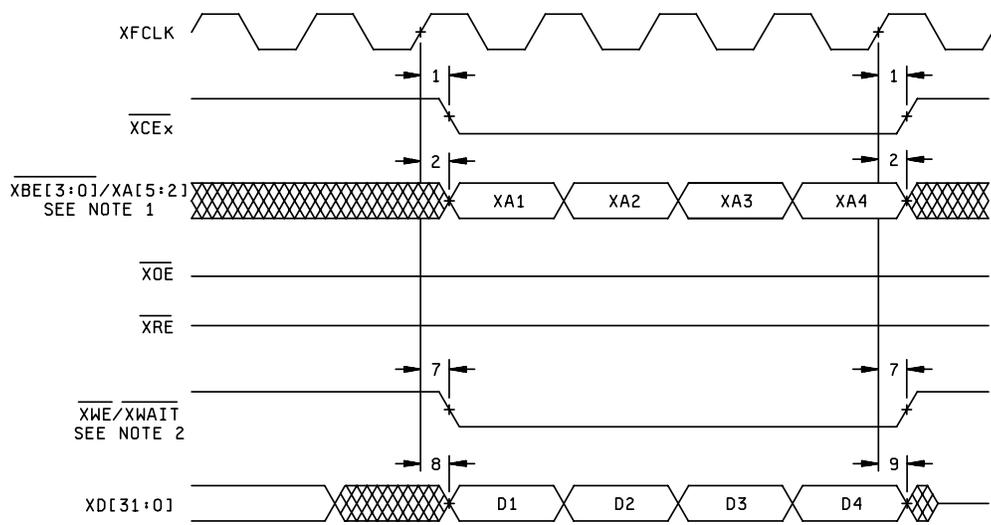
FIGURE 5. Timing waveforms. - Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
		REVISION LEVEL	SHEET 42



FIFO READ TIMING

1. $\overline{XBE}[3:0]/XA[5:2]$ operate as address signals $XA[5:2]$ during synchronous FIFO accesses.
2. $\overline{XWE}/\overline{XWAIT}$ operates as the write-enable signal \overline{XWE} during synchronous FIFO accesses.

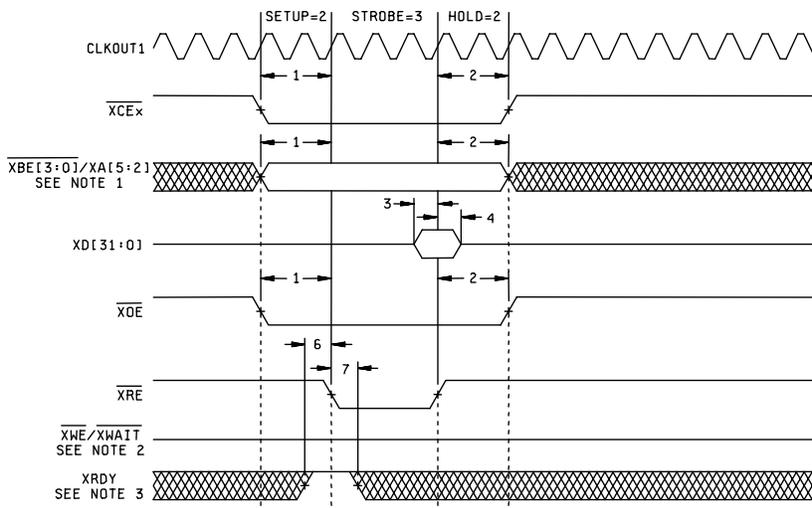


FIFO WRITE TIMING

1. $\overline{XBE}[3:0]/XA[5:2]$ operate as address signals $XA[5:2]$ during synchronous FIFO accesses.
2. $\overline{XWE}/\overline{XWAIT}$ operates as the write-enable signal \overline{XWE} during synchronous FIFO accesses.

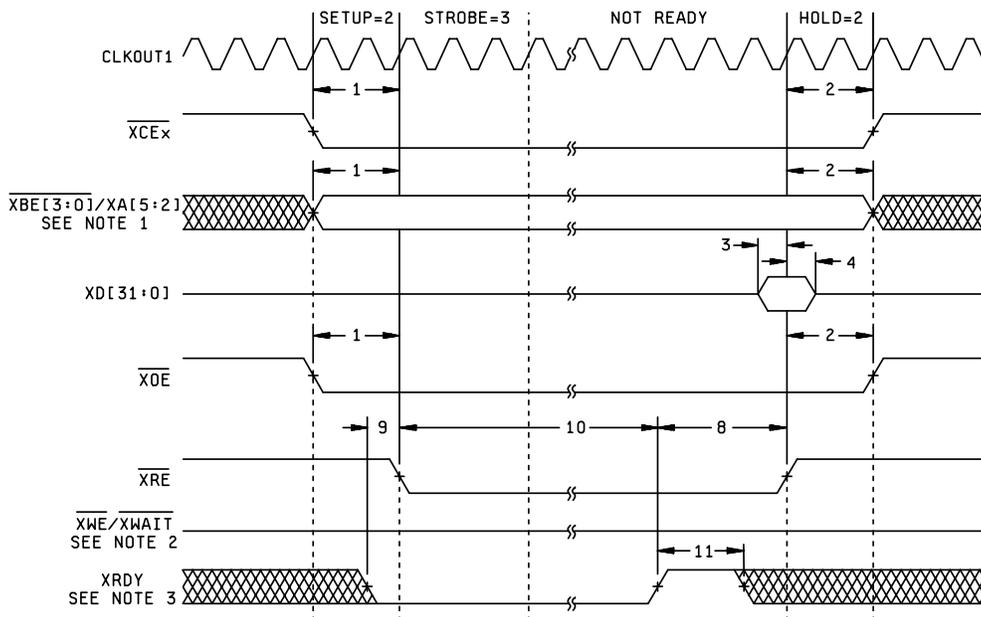
FIGURE 5. Timing waveforms. - Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
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EXPANSION BUS ASYNCHRONOUS PERIPHERAL READ TIMING (XRDY NOT USED)

1. XBE[3:0]/XA[5:2] operate as address signals XA[5:2] during synchronous FIFO accesses.
2. XWE/XWAIT operates as the write-enable signal XWE during synchronous FIFO accesses.
3. XRDY operates as active-high ready input during expansion bus asynchronous peripheral accesses.

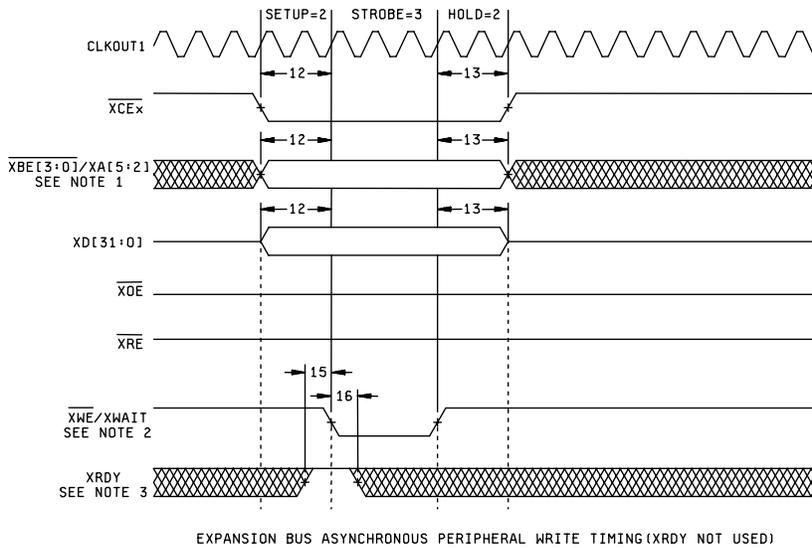


EXPANSION BUS ASYNCHRONOUS PERIPHERAL READ TIMING (XRDY USED)

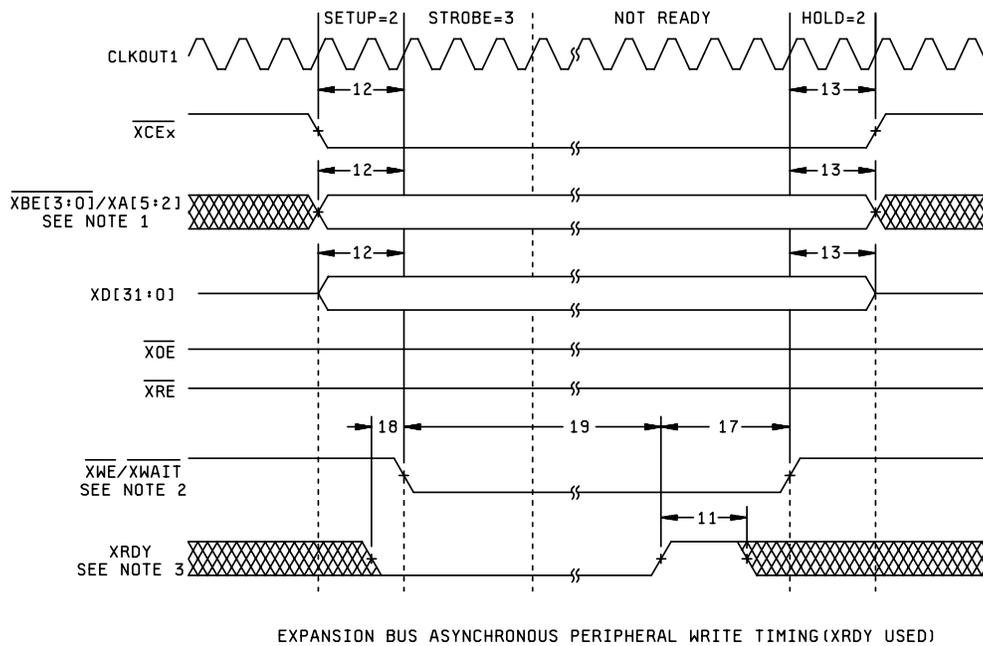
1. XBE[3:0]/XA[5:2] operate as address signals XA[5:2] during synchronous FIFO accesses.
2. XWE/XWAIT operates as the write-enable signal XWE during synchronous FIFO accesses.
3. XRDY operates as active-high ready input during expansion bus asynchronous peripheral accesses.

FIGURE 5. Timing waveforms. - Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
		REVISION LEVEL	SHEET 44



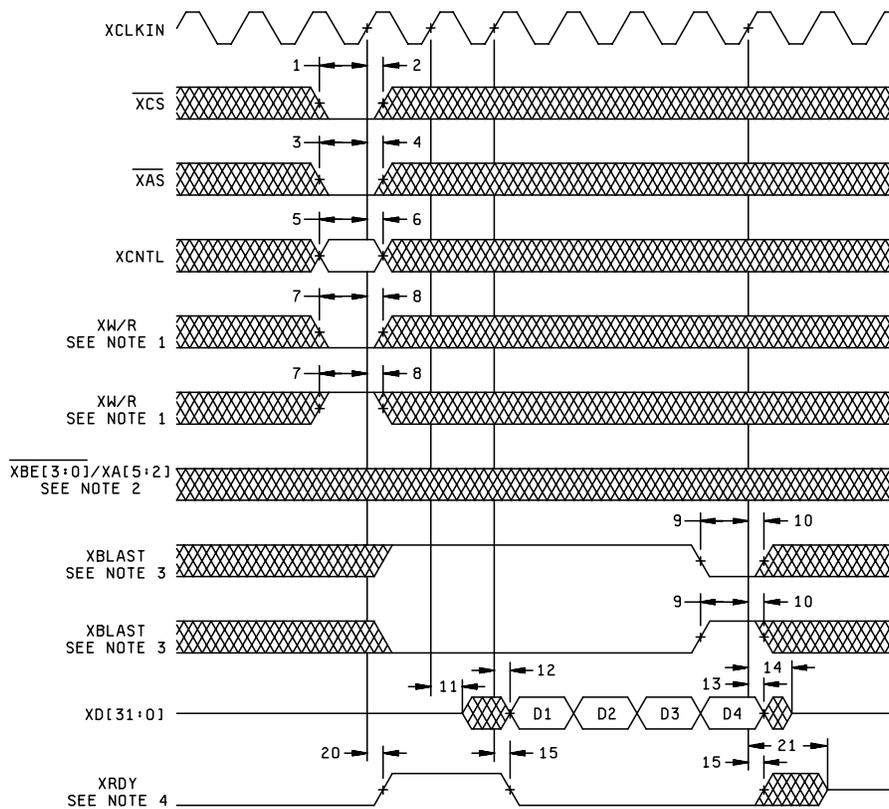
1. XBE[3:0]/XA[5:2] operate as address signals XA[5:2] during synchronous FIFO accesses.
2. XWE/XWAIT operates as the write-enable signal XWE during synchronous FIFO accesses.
3. XRDY operates as active-high ready input during expansion bus asynchronous peripheral accesses.



1. XBE[3:0]/XA[5:2] operate as address signals XA[5:2] during synchronous FIFO accesses.
2. XWE/XWAIT operates as the write-enable signal XWE during synchronous FIFO accesses.
3. XRDY operates as active-high ready input during expansion bus asynchronous peripheral accesses.

FIGURE 5. Timing waveforms. - Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A	5962-00510
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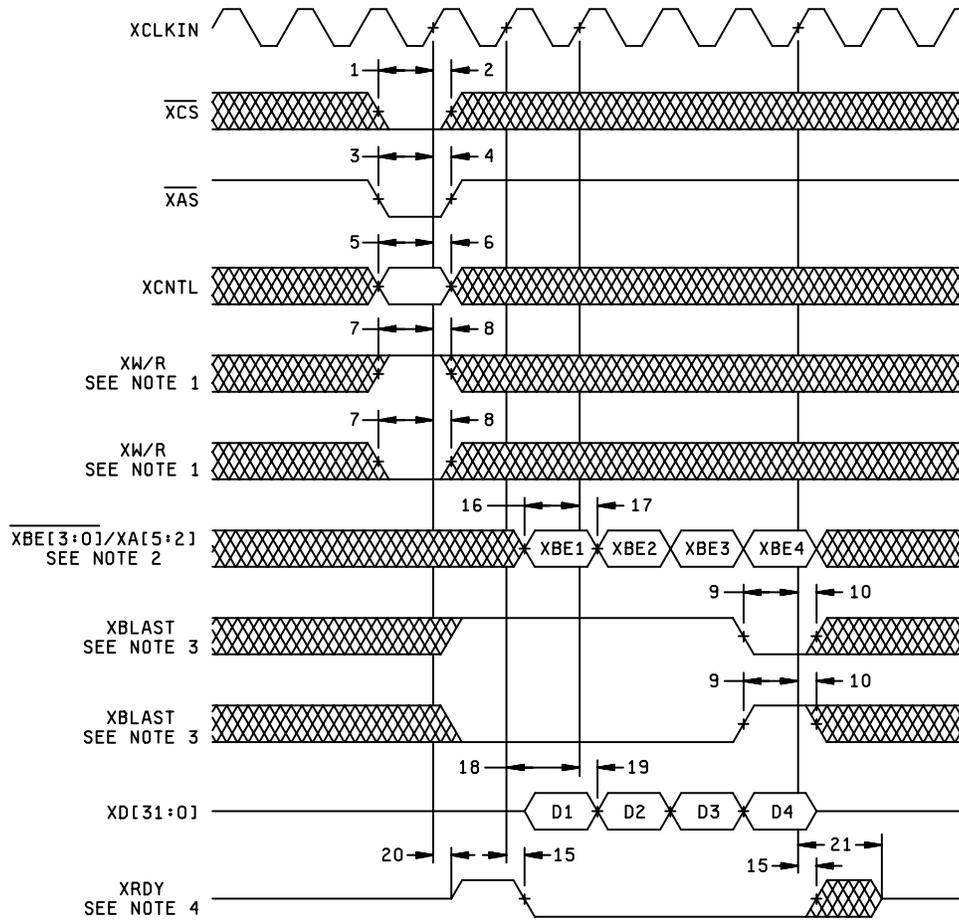


EXTERNAL HOST AS BUS MASTER-READ

1. XW/R input/output polarity selected at boot.
2. XBE[3:0]/XA[5:2] operate as byte-enables XBE[3:0] during host-port accesses.
3. XBLAST input polarity selected at boot.
4. XRDY operates as active-low ready input/output during host-port accesses.

FIGURE 5. Timing waveforms. – Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
		REVISION LEVEL	SHEET 46

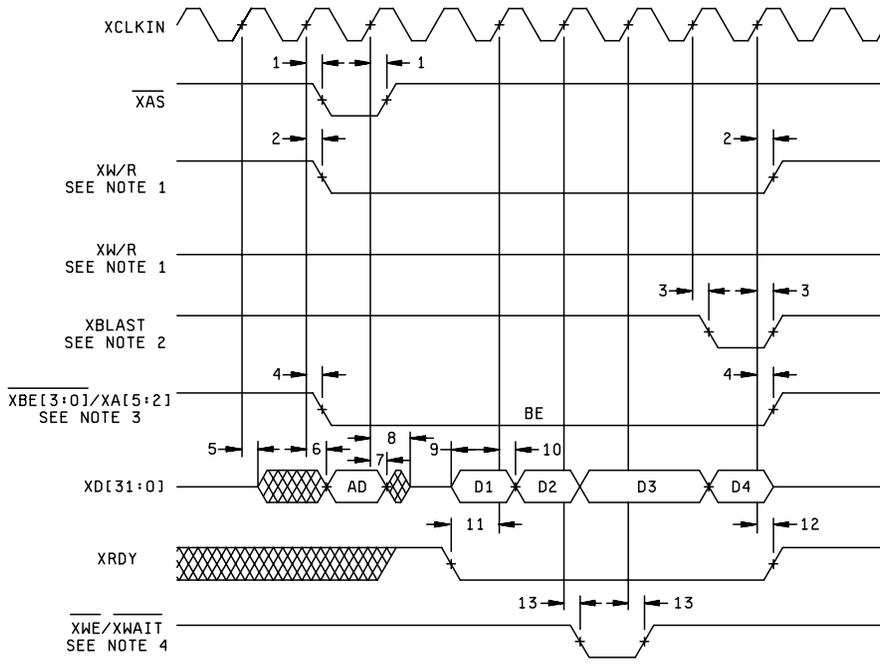


EXTERNAL HOST BUS MASTER-WRITE

1. XW/R input/output polarity selected at boot.
2. XBE[3:0]/XA[5:2] operate as byte-enables XBE[3:0] during host-port accesses.
3. XBLAST input polarity selected at boot.
4. XRDY operates as active-low ready input/output during host-port accesses.

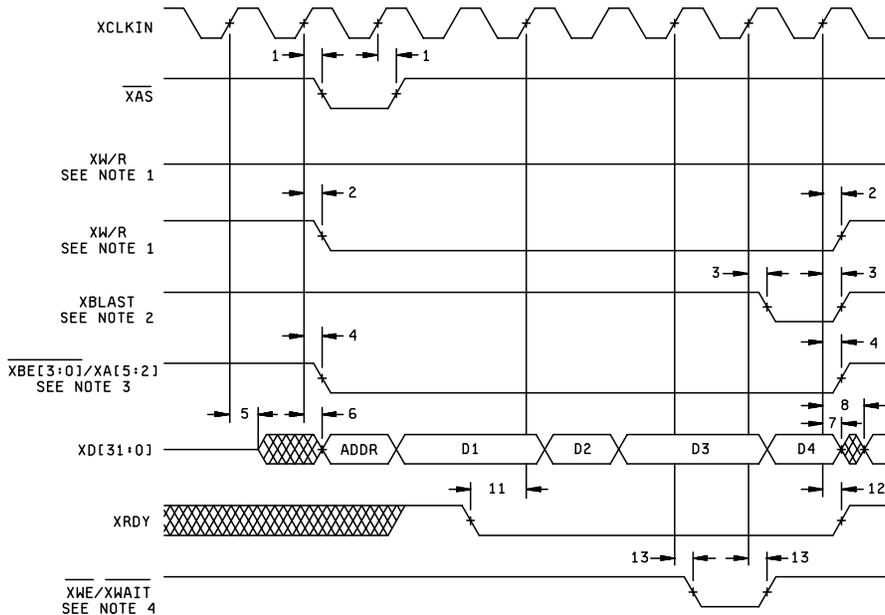
FIGURE 5. Timing waveforms. - Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
		REVISION LEVEL	SHEET 47



BUS MASTER-READ

1. XW/R input/output polarity selected at boot.
2. XBLAST output polarity is always active low.
3. XBE[3:0]/XA[5:2] operate as byte-enables XBE[3:0] during host-port accesses.
4. XWE/XWAIT operates as XWAIT output signal during host-port accesses.

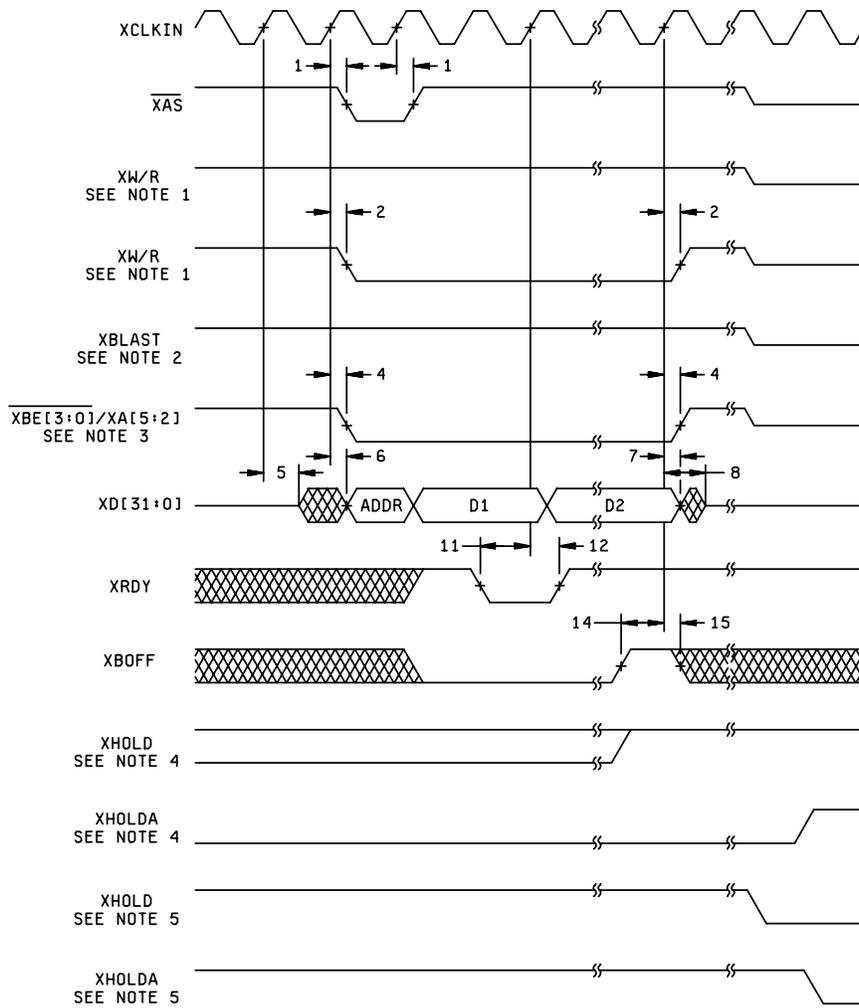


BUS MASTER-WRITE

1. XW/R input/output polarity selected at boot.
2. XBLAST output polarity is always active low.
3. XBE[3:0]/XA[5:2] operate as byte-enables XBE[3:0] during host-port accesses.
4. XWE/XWAIT operates as XWAIT output signal during host-port accesses.

FIGURE 5. Timing waveforms. – Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
		REVISION LEVEL	SHEET 48

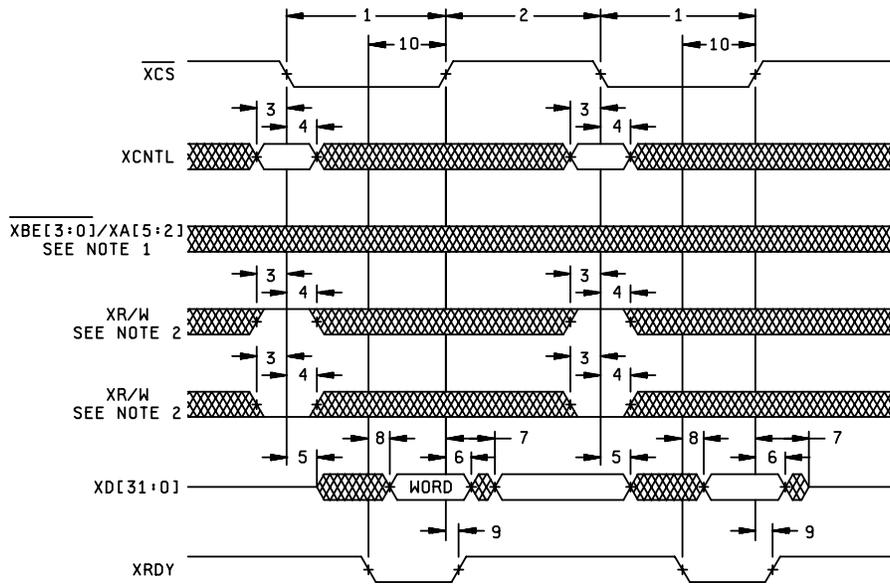


BUS MASTER-BOFF OPERATION
SEE NOTE 6

1. XW/R input/output polarity selected at boot.
2. XBLAST output polarity is always active low.
3. XBE[3:0]/XA[5:2] operate as byte-enables XBE[3:0] during host-port accesses.
4. Internal arbiter enabled.
5. External arbiter enabled.
6. This diagram illustrates XBOFF timing.

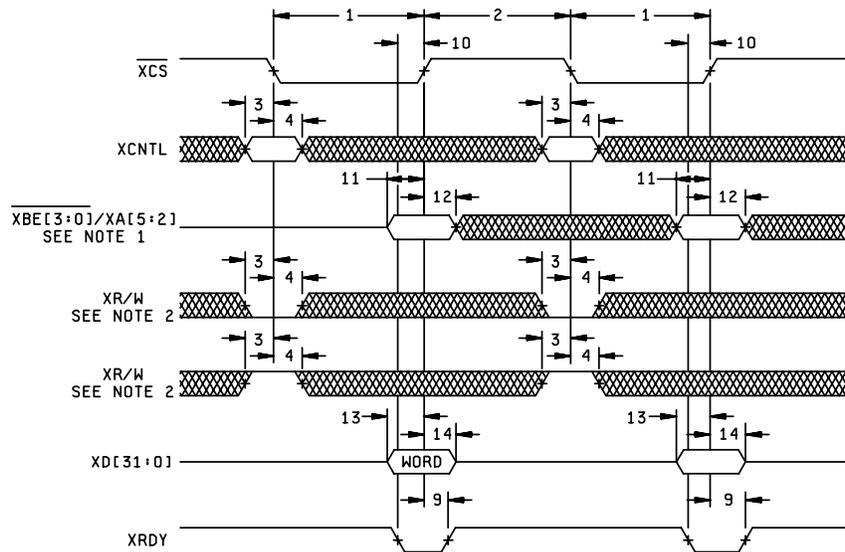
FIGURE 5. Timing waveforms. – Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
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EXTERNAL DEVICE AS ASYNCHRONOUS MASTER-READ

1. $\overline{XBE[3:0]}/XA[5:2]$ operate as byte-enables $\overline{XBE[3:0]}$ during host-port accesses.
2. XW/R input/output polarity selected at boot.

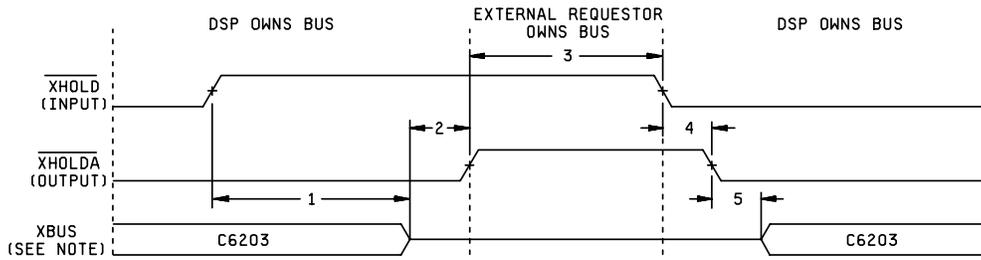


EXTERNAL DEVICE AS ASYNCHRONOUS MASTER-WRITE

1. $\overline{XBE[3:0]}/XA[5:2]$ operate as byte-enables $\overline{XBE[3:0]}$ during host-port accesses.
2. XW/R input/output polarity selected at boot.

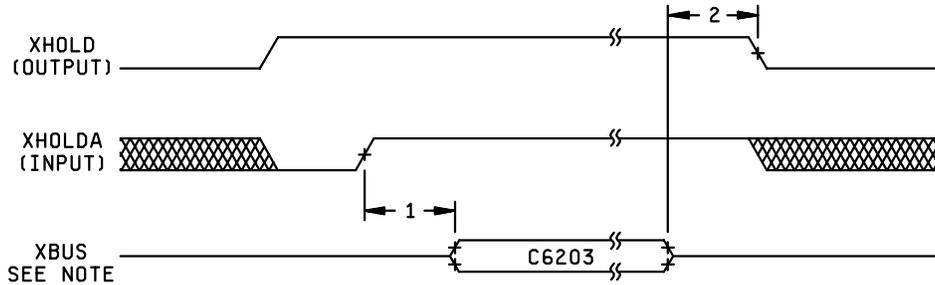
FIGURE 5. Timing waveforms. – Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00510
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EXPANSION BUS ARBITRATION-INTERNAL ARBITER ENABLE

Bus consists of $\overline{XBE}[3:0]/XA[5:2]$, \overline{XAS} , XW/R , and $XBLAST$.



EXPANSION BUS ARBITRATION-INTERNAL ARBITER DISABLED

Bus consists of $\overline{XBE}[3:0]/XA[5:2]$, \overline{XAS} , XW/R , and $XBLAST$.

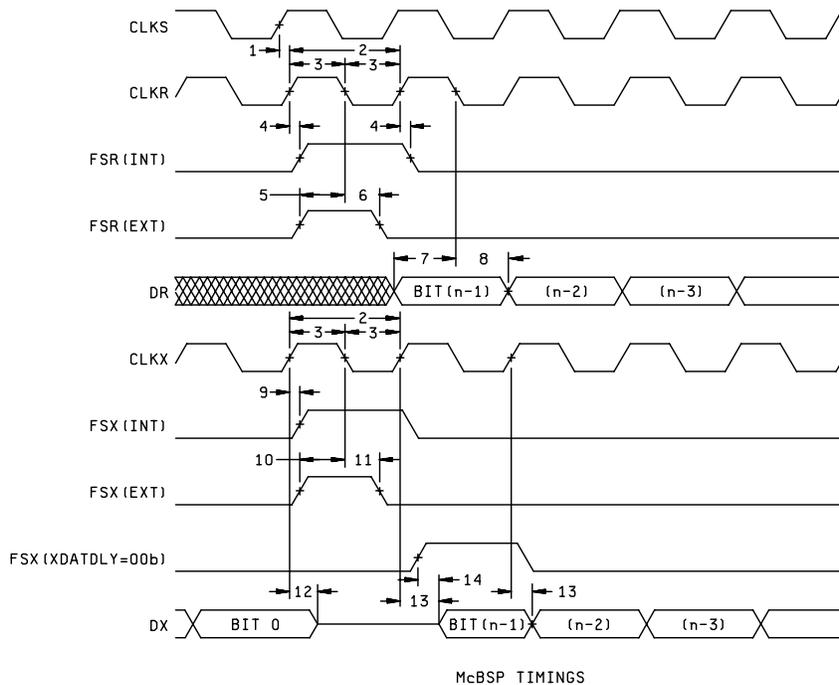


FIGURE 5. Timing waveforms. – Continued

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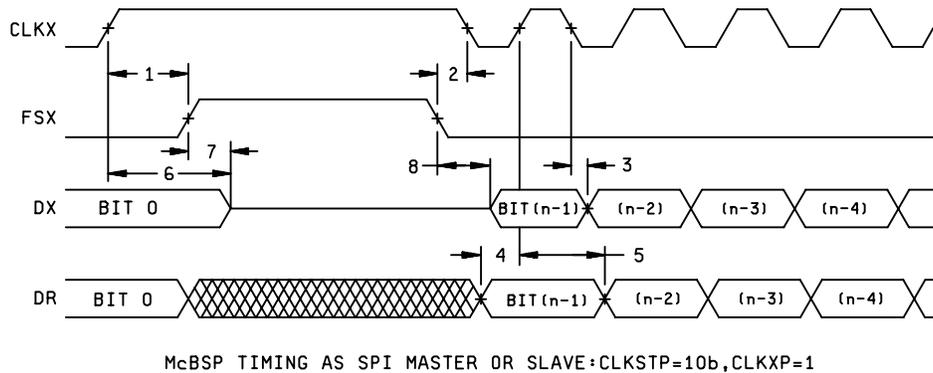
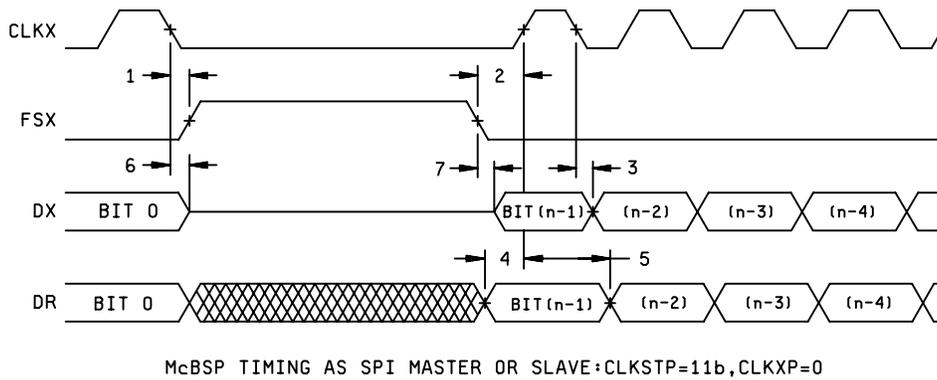
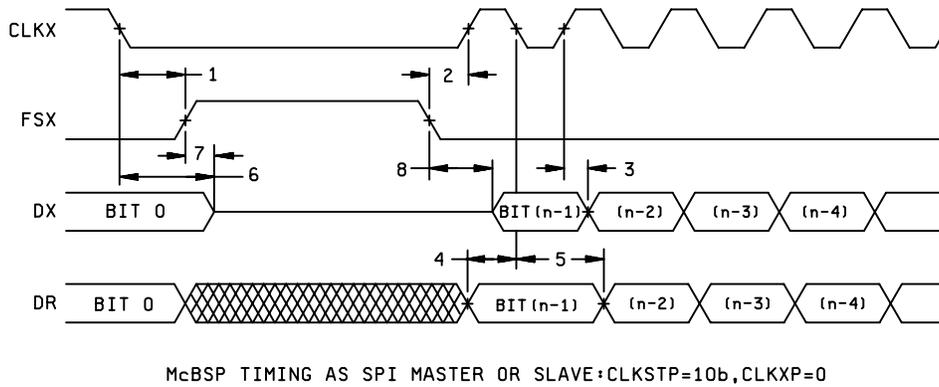
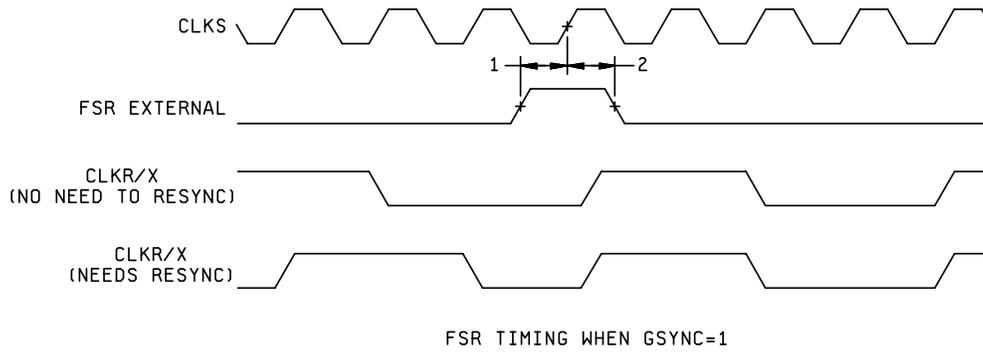
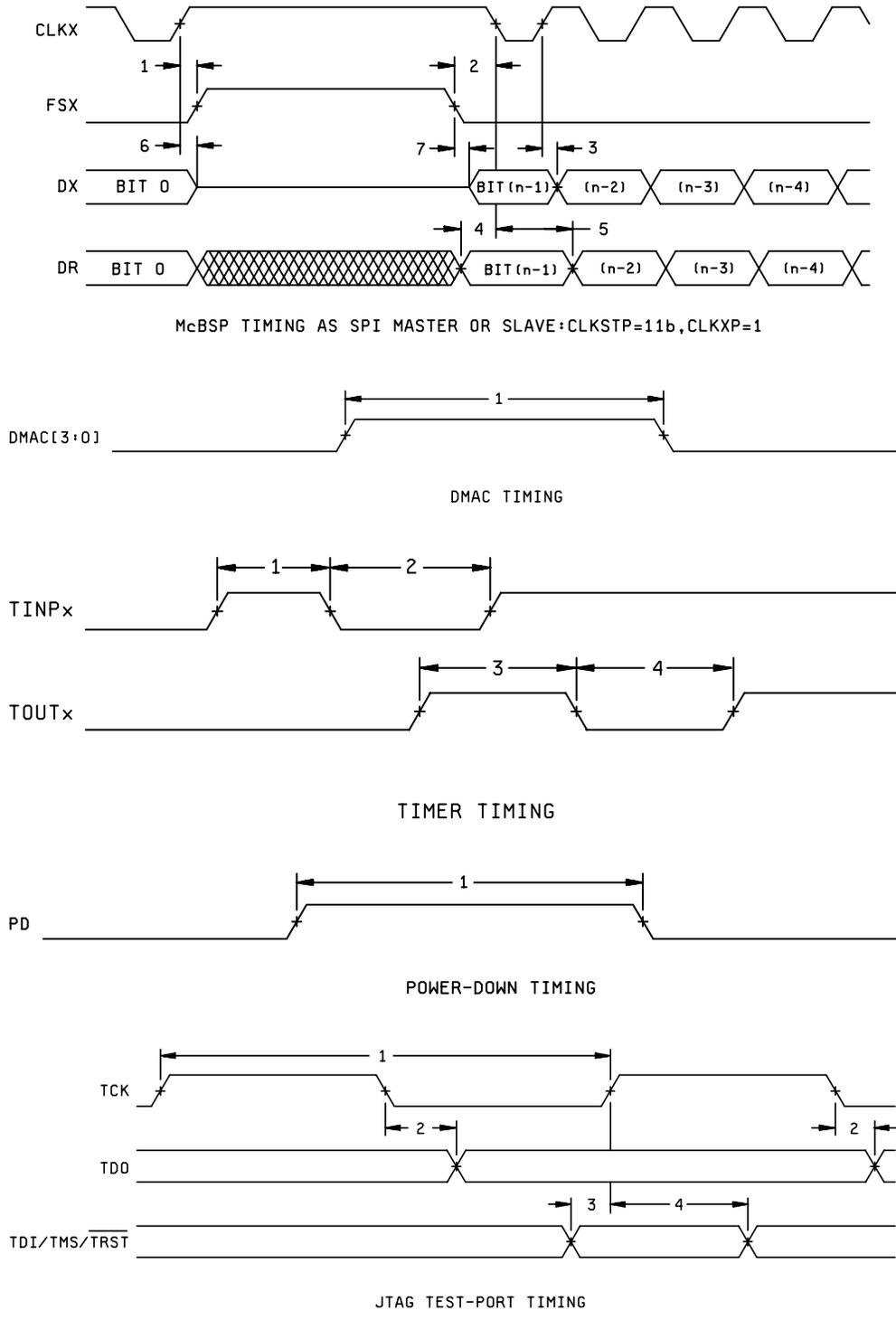


FIGURE 5. Timing waveforms. – Continued

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McBSP TIMING AS SPI MASTER OR SLAVE:CLKSTP=11b,CLKXP=1

DMAC TIMING

TIMER TIMING

POWER-DOWN TIMING

JTAG TEST-PORT TIMING

FIGURE 5. Timing waveforms. – Continued

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
 - (2) T_A = +125°C, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroup 4 (C_{IN} , C_{OUT}) shall be measured only for the initial test and after process or design changes which may affect input capacitance. One pin of each input/output driver (buffer) type shall be tested on each sample device. A minimum sample size of 5 devices with zero rejects shall be required.
- c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7	1, 7	1, 7
Final electrical parameters (see 4.2)	<u>1</u> / 1,2,3,7,8,9,10,11	<u>1</u> /1,2,3,7,8,9, 10,11	<u>2</u> / 1,2,3,7,8, 9,10,11
Group A test requirements (see 4.4)	1,2,3,7,8,9,10,11	1,2,3,7,8,9, 10,11	1,2,3,7,8,9, 10,11
Group C end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)			

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

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6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-07-23

Approved sources of supply for SMD 5962-00510 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-0051001QXA	01295	SMJ320C6203

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

01295

Vendor name
and address

Texas Instruments Incorporated
13500 N. Central Expressway
P.O. Box 655303
Dallas, TX 75265
Point of contact: 6412 Highway 75 South
Sherman, TX 75090-0084

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