

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to MIL-PRF-38535 requirements. - CFS	03-06-26	Thomas M. Hess

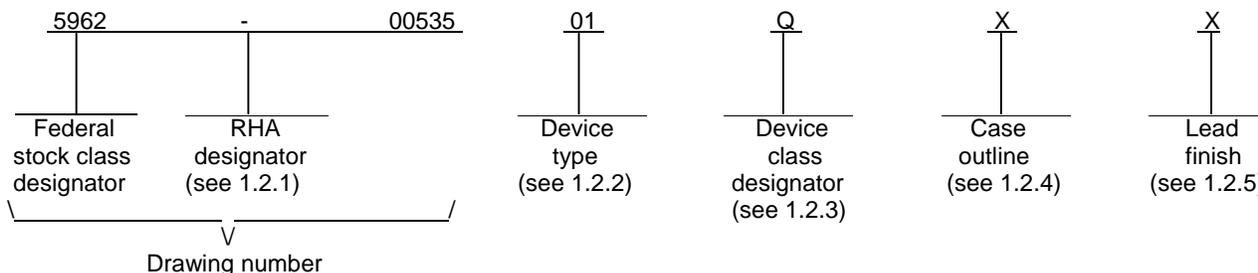
REV																					
SHEET																					
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32			
REV STATUS OF SHEETS				REV				A	A	A	A	A	A	A	A	A	A	A	A	A	
				SHEET				1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Thanh V. Nguyen	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 http://www.dscc.dla.mil		
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thanh V. Nguyen			
	APPROVED BY Thomas M. Hess	MICROCIRCUIT, DIGITAL, CMOS, PCI BRIDGE/ MEMORY CONTROLLER, MONOLITHIC SILICON		
	DRAWING APPROVAL DATE 00-11-21	SIZE A	CAGE CODE 67268	5962-00535
	REVISION LEVEL A	SHEET 1 OF 32		

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	PC106A-66	PCI bridge/memory controller
02	PC106A-83	PCI bridge/memory controller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	303	Ceramic column grid array

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 2

1.3 Absolute maximum ratings. ^{1/}

Supply voltage range (V_{CC}).....	-0.3 V dc to +3.6 V dc
PLL supply voltage range (AV_{CC})	-0.3 V dc to +3.6 V dc
DC input voltage range (V_{IN}).....	-0.3 V dc to +5.5 V dc
Maximum power dissipation (P_D):	
Device types 01	1.4 W
Device types 02	2.4 W
Storage temperature range (T_{STG}).....	-55°C to +150°C
Lead temperature (soldering, 10 seconds).....	+300°C
Thermal resistance, junction-to-case (θ_{JC})	0.1°C/W
Thermal resistance, junction-to-column (θ_{JS})	4.0°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}).....	+3.135 V dc to +3.465 V dc
PLL supply voltage range (AV_{CC})	+3.135 V dc to +3.465 V dc
Logic high input voltage range (V_{IH})	2.4 V dc to 5.5 V dc
Logic low input voltage range (V_{IL})	GND to 0.8 V dc
System clock input high voltage (CV_{IH})	2.4 V dc to 5.5 V dc
System clock input low voltage (CV_{IL})	GND to 0.4 V dc
Minimum high level output voltage (V_{OH}).....	2.4 V dc
Maximum low level output voltage (V_{OL}).....	0.5 V dc
Frequency of operation (f_{OP}):	
Device type 01	66 MHz
Device type 02	83 MHz
Case operating temperature range (T_C)	-55°C to +125°C
Maximum operating junction temperature (T_J)	+126°C
Minimum operating case temperature (T_C).....	-55°C

^{1/} Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 3

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 4

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance interface. The boundary-scan interface of the device is a fully compliant implementation of the IEEE 1149.1 standard.

3.11.1 Test access port. The device has five dedicated JTAG signals which are described in the following table. The TDI and TDO scan ports are used to scan instructions as well as data into the various scan registers for JTAG operations. The scan operation is controlled by the test access port (TAP) controller which in turn is controlled by the TMS input sequence. The scan data is latched in at the rising edge of TCK.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 5

IEEE interface pin descriptions

Signal name	Input/Output	Weak pullup provided	IEEE 1149.1 function
TDI	Input	Yes	Serial scan input signal
TDO	Output	No	Serial scan output signal
TMS	Input	Yes	TAP controller mode signal
TCK	Input	Yes	Scan clock
$\overline{\text{TRST}}$	Input	Yes	TAP controller reset

$\overline{\text{TRST}}$ is a JTAG optional signal which is used to reset the TAP controller asynchronously. The $\overline{\text{TRST}}$ signal assures that the JTAG logic does not interfere with the normal operation of the chip, and can be asserted coincident with the $\overline{\text{HRESET}}$.

3.11.2 TAP controller. The TAP (Tap Access Port) controller is a state machine that controls the JTAG scan protocol. The TAP controller implements 16 states specified by the IEEE 1149.1 specification. The TAP controller state machine is clocked by TCK and the state transitions are controlled by the TMS input.

3.11.3 JTAG instructions. The device supports the three required JTAG instructions: BYPASS, SAMPLE/PRELOAD, and EXTEST which are controlled by an 8-bit instruction register. These instructions are scanned in serially (LSB first) via the TDI pin. The table of the JTAG instructions for the device is given below.

JTAG instructions

Instruction	Encoding	Test data register accessed
BYPASS	11111111	Bypass register
SAMPLE/PRELOAD	11000000	Boundary-scan register
EXTEST	00000000	Boundary-scan register

The BYPASS instruction. The bypass register contains a single shift-register stage and is used to provide a minimum-length serial path between the TDI and the TDO pins of a component when no test operation of that component is required. This allows more rapid movement of test data to and from other components on a board that are required to perform test operations.

The SAMPLE/PRELOAD instruction. The mandatory SAMPLE/PRELOAD instruction allows a snapshot of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the boundary-scan shift register prior to selection of the other boundary-scan test instructions.

The EXTEST instruction. The mandatory EXTEST instruction allows testing of off-chip circuitry and board level interconnections. Data would typically be loaded onto the latched parallel outputs of boundary-scan shift-register stages using the SAMPLE/PRELOAD instruction prior to selection of the EXTEST instruction.

NOTE: Following use of the EXTEST instruction, the on-chip system logic may be in an indeterminate state that will persist until a system reset is applied. Therefore, the on-chip system logic may need to be reset on return to normal (i.e., nontest) operation.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 6

TABLE I. Electrical performance characteristics.

Test	Symbol and test no.	Test conditions -55°C ≤ T _C ≤ +125°C +3.135 V ≤ V _{CC} , AV _{CC} ≤ +3.465 V unless otherwise specified	Device type	Group A Subgroups	Limits		Unit
					Min	Max	
Input high voltage (all inputs except SYSCLK)	V _{IH}		All	1, 2, 3	2.0	5.5	V
Input low voltage (all inputs except SYSCLK)	V _{IL}		All	1, 2, 3	0.0	0.8	
SYSCLK input high voltage	CV _{IH}		All	1, 2, 3	2.4	5.5	V
SYSCLK input low voltage	CV _{IL}		All	1, 2, 3	0.0	0.4	
Output high voltage	V _{OH1}	I _{OH} = -7 mA	All	1, 2, 3	2.4		V
Output low voltage	V _{OL1}	I _{OL} = 7 mA	All	1, 2, 3		0.5	
PCI 3.3 V signaling output high voltage	V _{OH2}	I _{OH} = -0.5 mA	All	1, 2, 3	2.7		V
PCI 3.3 V signaling output high voltage	V _{OL2}	I _{OL} = 1.5 mA	All	1, 2, 3		0.3	
Input leakage current <u>1/</u>	I _{IN}	V _{IN} = 3.3 V	All	1, 2, 3		15	μA
High-Z (off-state) leakage current <u>1/</u>	I _{TSI}	V _{IN} = 3.3 V	All	1, 2, 3 1, 2, 3		15	μA
Input capacitance	C _{IN}	V _{IN} = 0.0 V, f = 1 MHz See 4.4.1c	All	4		7.0	pF
Functional test		See 4.4.1b	All	7, 8			

Clock AC timing specifications

60x processor bus (core) frequency <u>2/</u>			01	9, 10, 11	16.67	66.0	MHz
			02		16.67	83.3	
VCO frequency <u>2/</u>			All	9, 10, 11	120	200	MHz
SYSCLK frequency <u>2/</u>			All	9, 10, 11	16.67	33.33	MHz
SYSCLK cycle time	1	See figure 4	All	9, 10, 11	30.0	60.0	ns
SYSCLK rise and fall time <u>3/</u>	2, 3		All	9, 10, 11		2.0	ns
SYSCLK duty cycle measured at 1.4 V <u>4/</u>	4		All	9, 10, 11	40	60	%
SYSCLK jitter <u>5/</u>			All	9, 10, 11		±200	ps
106 internal PLL relock time <u>4/ 6/</u>			All	9, 10, 11		100	μs

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 7

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions -55°C ≤ T _C ≤ +125°C +3.135 V ≤ V _{CC} , AV _{CC} ≤ +3.465 V unless otherwise specified	Device Type	Group A Subgroups	Limits		Unit
					Min	Max	
Input AC timing specifications							
Group I input signals valid to 60x bus clock (input setup) <u>7/ 8/ 9/</u>	10a	See figure 4	01	9, 10, 11	4.0		ns
			02		3.5		
Group II input signals valid to 60x bus clock (input setup) <u>7/ 8/ 10/</u>	10a		01	9, 10, 11	3.5		ns
			02		3.5		
Group III input signals valid to 60x bus clock (input setup) <u>7/ 8/ 11/</u>	10a		01	9, 10, 11	3.0		ns
			02		2.5		
Group IV input signals valid to 60x bus clock (input setup) <u>7/ 8/ 12/</u>	10a		01	9, 10, 11	5.0		ns
			02		4.0		
Group V input signals valid to SYSCLK clock (input setup) <u>13/ 14/</u>	10b		01	9, 10, 11	7.0		ns
			02		7.0		
Group VI input signals valid to SYSCLK clock (input setup) <u>13/ 15/</u>	10b	01	9, 10, 11	7.0		ns	
		02		7.0			
60x bus clock to group I – VI inputs invalid (input hold) <u>9/ 10/ 11/ 12/</u>	11a		All	9, 10, 11	0.0		ns
SYSCLK to group I – VI inputs invalid (input hold) <u>14/ 15/</u>	11b		All	9, 10, 11	-0.5		ns
$\overline{\text{HRST}}$ pulse width			All	9, 10, 11	255 t _{SYSCLK} + 100 μs		μs
Mode select inputs valid $\overline{\text{HRST}}$ (input setup) <u>16/ 17/ 18/</u>	10c		All	9, 10, 11	3 t _{SYSCLK}		ns
$\overline{\text{HRST}}$ to mode select inputs invalid (input hold) <u>16/ 18/</u>	11c		All	9, 10, 11	1.0		ns

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 8

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions -55°C ≤ T _C ≤ +125°C +3.135 V ≤ V _{CC} , AV _{CC} ≤ +3.465 V unless otherwise specified	Device type	Group A Subgroups	Limits		Unit
					Min	Max	
Output AC timing specifications							
SYSCLK to output driven (output enable time) <u>18/</u>	12	See figure 4	01	9, 10, 11	2.0		ns
			02		2.0		
SYSCLK to output valid for \overline{TS} and \overline{ARTRY} <u>8/ 19/ 20/ 21/</u>	13a	See figure 4	01	9, 10, 11		7.0	ns
			02			6.0	
SYSCLK to output valid for all non-PCI signals except \overline{TS} , \overline{ARTRY} , \overline{RAS} [0-7], \overline{CAS} [0-7], and \overline{DWE} [0-2] <u>8/ 19/ 20/ 22/</u>	13b	See figure 4	01	9, 10, 11		7.0	ns
			02			6.0	
SYSCLK to output valid for \overline{RAS} [0-7] and \overline{CAS} [0-7] <u>8/ 19/ 20/</u>	14a	See figure 4	01	9, 10, 11		7.0	ns
			02			6.0	
SYSCLK to output valid for PCI signals <u>20/ 23/</u>	14b	See figure 4	01	9, 10, 11		11.0	ns
			02			11.0	
SYSCLK to output invalid for all non-PCI signals (output hold) <u>24/ 25/</u>	15a	See figure 4	01	9, 10, 11	1.0		ns
			02		1.0		
SYSCLK to output invalid for PCI signals (output hold) <u>24/</u>	15b	See figure 4	01	9, 10, 11	1.0		ns
			02		1.0		
SYSCLK to \overline{ARTRY} high impedance before precharge (output hold) <u>18/</u>	18	See figure 4	01	9, 10, 11		8.0	ns
			02			8.0	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 9

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions -55°C ≤ T _C ≤ +125°C +3.135 V ≤ V _{CC} , AV _{CC} ≤ +3.465 V unless otherwise specified	Device type	Group A Subgroups	Limits		Unit
					Min	Max	
Output AC timing specifications – Continued							
SYSCLK to $\overline{\text{ARTRY}}$ precharge enable) <u>17/ 18/</u>	19	See figure 4	All	9, 10, 11	0.4 t _{SYSCLK} + 2.0		ns
SYSCLK to $\overline{\text{ARTRY}}$ high impedance after precharge <u>17/ 18/</u>	21		All	9, 10, 11		1.5 t _{SYSCLK} + 8.0	ns
JTAG AC timing specifications (independent of SYSCLK)							
TCK frequency of operation			All	9, 10, 11	0.0	25.0	MHz
TCK cycle time	1	See figure 4	All	9, 10, 11	40.0		ns
TCK clock pulse width measured at 1.4 V	2		All	9, 10, 11	20.0		ns
TCK rise and fall times	3		All	9, 10, 11	0.0	3.0	ns
$\overline{\text{TRST}}$ setup time to TCK rising edge <u>26/</u>	4		All	9, 10, 11	10.0		ns
$\overline{\text{TRST}}$ assert time	5		All	9, 10, 11	10.0		ns
Boundary scan input data setup time <u>27/</u>	6		All	9, 10, 11	5.0		ns
Boundary scan input data hold time <u>27/</u>	7		All	9, 10, 11	15.0		ns
TCK to output data valid <u>28/</u>	8		All	9,10,11	0.0	30.0	ns
TCK to output high impedance <u>28/</u>	9		All	9,10,11	0.0	30.0	ns
TMS, TDI data setup time	10		All	9,10,11	5.0		ns
TMS, TDI data hold time	11		All	9,10,11	15.0		ns
TCK to TDO data valid	12		All	9,10,11	0.0	15.0	ns
TCK to TDO high impedance	13		All	9,10,11	0.0	15.0	ns

See footnotes on next sheet.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 10

TABLE I. Electrical performance characteristics - Continued.

- 1/ Excludes test signals ($\overline{\text{LSSD_MODE}}$ and JTAG signals).
- 2/ Caution: The SYSCLK frequency and PLL[0-3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
- 3/ Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4V.
- 4/ Timing is guaranteed by design and characterization, and is not tested.
- 5/ The total input jitter (short-term and long-term combined) must be under ± 200 ps.
- 6/ PLL relock time is the maximum amount of time required for PLL lock after a stable V_{CC} , AV_{CC} , and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during the sleep and suspend power-saving modes. Also note that $\overline{\text{HRST}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time (100 μs) during the power-on reset sequence.
- 7/ All inputs specifications are measured from the TTL level (0.8 V or 2.0 V) of the signal in question to the 1.4 V of the rising edge of the input SYSCLK. Both input and output timings are measured at the pin.
- 8/ Processor and memory interface signals are specified from the rising edge of the 60x bus clock (which is internally synchronized to SYSCLK).
- 9/ Group I input signals include the following processor, L2, and memory interface signals: $\overline{\text{A}}[0-31]$, $\overline{\text{PAR}}[0-7]/\overline{\text{AR}}[1-8]$, $\overline{\text{BR}}[0-4]$, $\overline{\text{BRL2}}$, $\overline{\text{XATS}}$, $\overline{\text{LBCLAIM}}$, $\overline{\text{ADS}}$, $\overline{\text{BA0}}$, $\overline{\text{TV}}$, and $\overline{\text{HIT}}$ (when configured for external L2).
- 10/ Group II input signals include the following processor and memory interface signals: $\overline{\text{TBST}}$, $\overline{\text{TT}}[0-4]$, $\overline{\text{TSIZ}}[0-2]$, $\overline{\text{WT}}$, $\overline{\text{CI}}$, $\overline{\text{GBL}}$, $\overline{\text{AACK}}$, and $\overline{\text{TA}}$.
- 11/ Group III input signals include the following processor and memory interface signals: $\overline{\text{DL}}[0-3]$ and $\overline{\text{DH}}[0-31]$.
- 12/ Group IV input signals include the following processor and L2 interface signals: $\overline{\text{TS}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DIRTY_IN}}$, and $\overline{\text{HIT}}$ (when configured for internal L2 controller).
- 13/ PCI 3.3 V signaling environment signals are measured from 1.65 V ($V_{CC}/2$) on the rising edge of SYSCLK to $V_{OH} = 3.0$ V or $V_{OL} = 0.3$ V. PCI 5.0 V signaling environment signals are measured from 1.65 V ($V_{CC}/2$) on the rising edge of SYSCLK to $V_{OH} = 2.4$ V or $V_{OL} = 0.55$ V.
- 14/ Group V input signals include the following bussed PCI interface signals: $\overline{\text{FRAME}}$, $\overline{\text{C/BE}}[0-3]$, $\overline{\text{AD}}[0-31]$, $\overline{\text{DEVSEL}}$, $\overline{\text{IRDY}}$, $\overline{\text{TRDY}}$, $\overline{\text{STOP}}$, $\overline{\text{PAR}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, $\overline{\text{LOCK}}$, $\overline{\text{FLSHREQ}}$, and $\overline{\text{ISA_MASTER}}$.
- 15/ Group VI input signal is the point-to-point PCI $\overline{\text{GNT}}$ input signal.
- 16/ The setup and hold time is with respect to the rising edge of $\overline{\text{HRST}}$. Mode select inputs include the $\overline{\text{RCS0}}$, $\overline{\text{FOE}}$, and $\overline{\text{DBG0}}$ configuration inputs.
- 17/ t_{SYSCLK} is the period of the external clock (SYSCLK) in nanoseconds (ns). When the unit is given as t_{SYSCLK} , the numbers given in the table I must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.

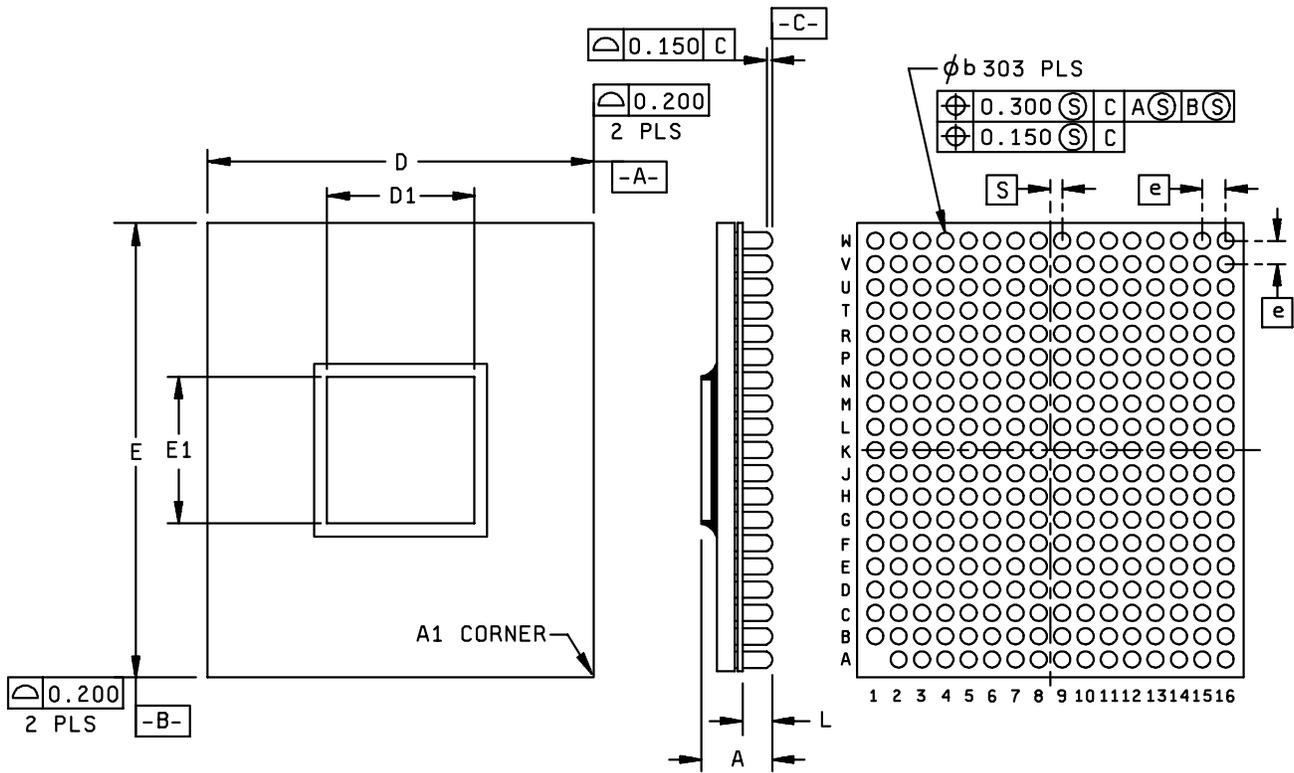
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 11

TABLE I. Electrical performance characteristics - Continued.

- 18/ These values are guaranteed by design, and are not tested.
- 19/ All output specifications are measured from the 1.4 V on the rising edge of the appropriate clock to the TTL level (0.8 V or 2.0 V) of the signal in question. Both input and output timings are measured at the pin.
- 20/ The maximum timing specifications assume $C_L = 50$ pF.
- 21/ The shared outputs \overline{TS} and \overline{ARTRY} require pull-up resistors to hold them negated when there is no bus master driving them.
- 22/ When the device is configured for asynchronous L2 cache SRAMs, the \overline{DWE} [0-2] signals have a maximum SYSCLK to output valid time of $(0.5 \times t_{PROC}) + 8.0$ ns (where t_{PROC} is the 60x bus clock cycle time).
- 23/ PCI 3.3 V signaling environment signals are measured from 1.65 V ($V_{CC}/2$) on the rising edge of SYSCLK to $V_{OH} = 3.0$ V or $V_{OL} = 0.3$ V.
- 24/ The minimum timing specification assumes $C_L = 0$ pF.
- 25/ PCI devices which require more than the PCI-specified hold time of $t_h = 0$ ns or systems where clock skew approaches the PCI-specified allowance of 2 ns may not work with the device.
- 26/ \overline{TRST} is an asynchronous signal. The setup time is for test purposes only.
- 27/ Non-test signal input timing with respect to TCK.
- 28/ Non-test signal output timing with respect to TCK.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 12

Case X



Symbol	Millimeters	
	Min	Max
A	3.840 BSC	
D	21.000 BSC	
D1	6.200 BSC	
e	1.270 BSC	
E	25.000 BSC	
E1	7.600 BSC	
L	1.545	1.695
S	0.635 BSC	
φb	0.790	0.990

FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 13

Case X							
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
A2	$\overline{\text{MEMACK}}$	B11	AD11	D4	AD0	E13	$\overline{\text{MDLE}} / \overline{\text{SDCAS}}$
A3	$\overline{\text{FLSHREQ}}$	B12	AD7	D5	AD4	E14	$\overline{\text{CAS7}} / \overline{\text{DQM7}}$
A4	AD31	B13	TDI	D6	$\overline{\text{C/BE0}}$	E15	NMI
A5	AD27	B14	AD1	D7	AD10	E16	$\overline{\text{CAS3}} / \overline{\text{DQM3}}$
A6	$\overline{\text{C/BE3}}$	B15	PAR7/AR8	D8	AD14	F1	A18
A7	AD20	B16	PAR4/AR5	D9	AD17	F2	$\overline{\text{ARTRY}}$
A8	AD16	C1	A24	D10	AD21	F3	TSIZ2
A9	$\overline{\text{STOP}}$	C2	A25	D11	AD24	F4	A21
A10	$\overline{\text{FRAME}}$	C3	A27	D12	AD28	F5	V _{CC}
A11	AD13	C4	AD2	D13	$\overline{\text{FOE}}$	F6	V _{SS}
A12	AD9	C5	AD6	D14	TMS	F7	V _{CC}
A13	AD5	C6	AD8	D15	PAR1/AR2	F8	$\overline{\text{DEVSEL}}$
A14	AD3	C7	AD12	D16	PAR0/AR1	F9	$\overline{\text{PERR}}$
A15	$\overline{\text{GNT}}$	C8	$\overline{\text{C/BE1}}$	E1	A19	F10	V _{SS}
A16	PAR6/AR7	C9	$\overline{\text{C/BE2}}$	E2	A20	F11	V _{CC}
B1	A26	C10	AD19	E3	A22	F12	V _{SS}
B2	A28	C11	AD23	E4	A29	F13	TCK
B3	$\overline{\text{ISA_MASTER}} / \overline{\text{BERR}}$	C12	AD26	E5	A31	F14	$\overline{\text{CAS6}} / \overline{\text{DQM6}}$
B4	$\overline{\text{REQ}}$	C13	AD30	E6	V _{CC}	F15	$\overline{\text{BCTL1}}$
B5	AD29	C14	PAR5/AR6	E7	V _{SS}	F16	$\overline{\text{BCTL0}}$
B6	AD25	C15	PAR3/AR4	E8	$\overline{\text{IRDY}}$	G1	TT0
B7	AD22	C16	PAR2/AR3	E9	$\overline{\text{SERR}}$	G2	A17
B8	AD18	D1	A23	E10	V _{CC}	G3	TSIZ0
B9	$\overline{\text{TRDY}}$	D2	$\overline{\text{AACK}}$	E11	V _{SS}	G4	TSIZ1
B10	AD15	D3	A30	E12	TDO	G5	V _{SS}

FIGURE 2. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 14

Case X							
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
G6	V _{CC}	H15	$\overline{\text{CAS1}}/\overline{\text{DQM1}}$	K8	V _{SS}	M1	TT4
G7	V _{SS}	H16	$\overline{\text{QREQ}}$	K9	AV _{CC}	M2	A3
G8	$\overline{\text{LOCK}}$	J1	$\overline{\text{TEA}}$	K10	V _{CC}	M3	$\overline{\text{GBL}}$
G9	PAR	J2	A10	K11	$\overline{\text{RAS7}}/\overline{\text{CS7}}$	M4	$\overline{\text{WT}}$
G10	V _{CC}	J3	A12	K12	$\overline{\text{RAS4}}/\overline{\text{CS4}}$	M5	V _{CC}
G11	$\overline{\text{LSSD_MODE}}$	J4	A13	K13	$\overline{\text{RAS2}}/\overline{\text{CS2}}$	M6	V _{SS}
G12	V _{CC}	J5	A6	K14	$\overline{\text{RAS3}}/\overline{\text{CS3}}$	M7	V _{CC}
G13	$\overline{\text{CAS5}}/\overline{\text{DQM5}}$	J6	A11	K15	MA10/ SDMA10/AR18	M8	NC
G14	$\overline{\text{CAS4}}/\overline{\text{DQM4}}$	J7	V _{SS}	K16	MA11/ SDMA11/AR19	M9	NC
G15	RTC	J8	V _{CC}	L1	TT3	M10	V _{SS}
G16	$\overline{\text{CAS2}}/\overline{\text{DQM2}}$	J9	V _{SS}	L2	A4	M11	V _{CC}
H1	TT1	J10	$\overline{\text{CKE}}/\overline{\text{DBGLB}}$	L3	$\overline{\text{BR0}}$	M12	V _{SS}
H2	A16	J11	$\overline{\text{MCP}}$	L4	$\overline{\text{TBST}}$	M13	DL18
H3	A14	J12	$\overline{\text{RAS6}}/\overline{\text{CS6}}$	L5	$\overline{\text{DBG0}}$	M14	$\overline{\text{RAS0}}/\overline{\text{CS0}}$
H4	A15	J13	$\overline{\text{RCS1}}$	L6	SYSCLK	M15	MA7/ SDMA7/AR15
H5	V _{CC}	J14	$\overline{\text{PPEN}}$	L7	V _{SS}	M16	MA8/ SDMA8/AR16
H6	V _{SS}	J15	$\overline{\text{CAS0}}/\overline{\text{DQM0}}$	L8	V _{CC}	N1	$\overline{\text{TA}}$
H7	V _{CC}	J16	MA12/ SDMA12/AR20	L9	V _{SS}	N2	A2
H8	NC	K1	TT2	L10	$\overline{\text{RAS5}}/\overline{\text{CS5}}$	N3	$\overline{\text{CI}}$
H9	NC	K2	A5	L11	$\overline{\text{CKO}}/\overline{\text{DWE2}}$	N4	$\overline{\text{LBCLAIM}}$
H10	$\overline{\text{PIRQ}}/\overline{\text{SDRAS}}$	K3	$\overline{\text{BG0}}$	L12	V _{CC}	N5	V _{SS}
H11	$\overline{\text{DWE1}}/\overline{\text{DBG3}}$	K4	A7	L13	$\overline{\text{RAS1}}/\overline{\text{CS1}}$	N6	V _{CC}
H12	V _{SS}	K5	A8	L14	$\overline{\text{QACK}}$	N7	V _{SS}
H13	$\overline{\text{TRST}}$	K6	A9	L15	MA9/ SDMA9/AR17	N8	DH22
H14	$\overline{\text{SUSPEND}}$	K7	V _{CC}	L16	$\overline{\text{HRST}}$	N9	DL7

FIGURE 2. Terminal connections - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 15

Case X							
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
N10	V _{CC}	R4	$\overline{\text{DIRTY_OUT}} / \overline{\text{BG1}}$	T14	DH0	V8	DH20
N11	V _{SS}	R5	$\overline{\text{TWE}} / \overline{\text{BG2}}$	T15	$\overline{\text{WE}}$	V9	DH24
N12	V _{CC}	R6	V _{CC}	T16	MA2/ SDMA2/AR10	V10	DH26
N13	DH15	R7	V _{SS}	U1	DL20	V11	DH28
N14	DL17	R8	DL5	U2	DL21	V12	DH30
N15	MA0/SDBA1 SDMA0/AR0	R9	DL9	U3	DH6	V13	DL31
N16	MA6/ SDMA6/AR14	R10	V _{CC}	U4	$\overline{\text{DBG1}} / \overline{\text{TOE}}$	V14	DL29
P1	$\overline{\text{XATS}} / \overline{\text{SDM}} / \overline{\text{AT}}$	R11	V _{SS}	U5	$\overline{\text{DOE}} / \overline{\text{DBGL2}}$	V15	DL27
P2	A1	R12	DL16	U6	DL0	V16	DL24
P3	$\overline{\text{DWE0}} / \overline{\text{DBG2}}$	R13	DH1	U7	DL2	W1	DH7
P4	BA1/ $\overline{\text{BAA}}$ / $\overline{\text{BGL2}}$	R14	DH2	U8	DL4	W2	DH9
P5	V _{CC}	R15	$\overline{\text{RCS0}}$	U9	DL10	W3	DH11
P6	V _{SS}	R16	MA3/ SDMA3/AR11	U10	DL12	W4	DH13
P7	V _{CC}	T1	$\overline{\text{DCS}} / \overline{\text{BG3}}$	U11	PLL0	W5	DH15
P8	DL6	T2	DL19	U12	PLL2	W6	DH17
P9	DL8	T3	$\overline{\text{DIRTY_IN}} / \overline{\text{BR1}}$	U13	DL14	W7	DH19
P10	V _{SS}	T4	$\overline{\text{HIT}}$	U14	DL25	W8	DH21
P11	V _{CC}	T5	$\overline{\text{BA0}} / \overline{\text{BR3}}$	U15	DL23	W9	DH23
P12	V _{SS}	T6	$\overline{\text{TV}} / \overline{\text{BR2}}$	U16	MA1/ SDMA0/AR9	W10	DH25
P13	DH3	T7	DL1	V1	DL22	W11	DH27
P14	DH4	T8	DL3	V2	DH8	W12	DH29
P15	MA4/ SDMA4/AR12	T9	DL11	V3	DH10	W13	DH31
P16	MA5/ SDMA5/AR13	T10	DL13	V4	DH12	W14	DL30
R1	$\overline{\text{TS}}$	T11	PLL1	V5	DH14	W15	DL28
R2	A0	T12	PLL3	V6	DH16	W16	DL26
R3	$\overline{\text{ADS}} / \overline{\text{DALE}} / \overline{\text{BRL2}}$	T13	DL15	V7	DH18		

FIGURE 2. Terminal connections - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 16

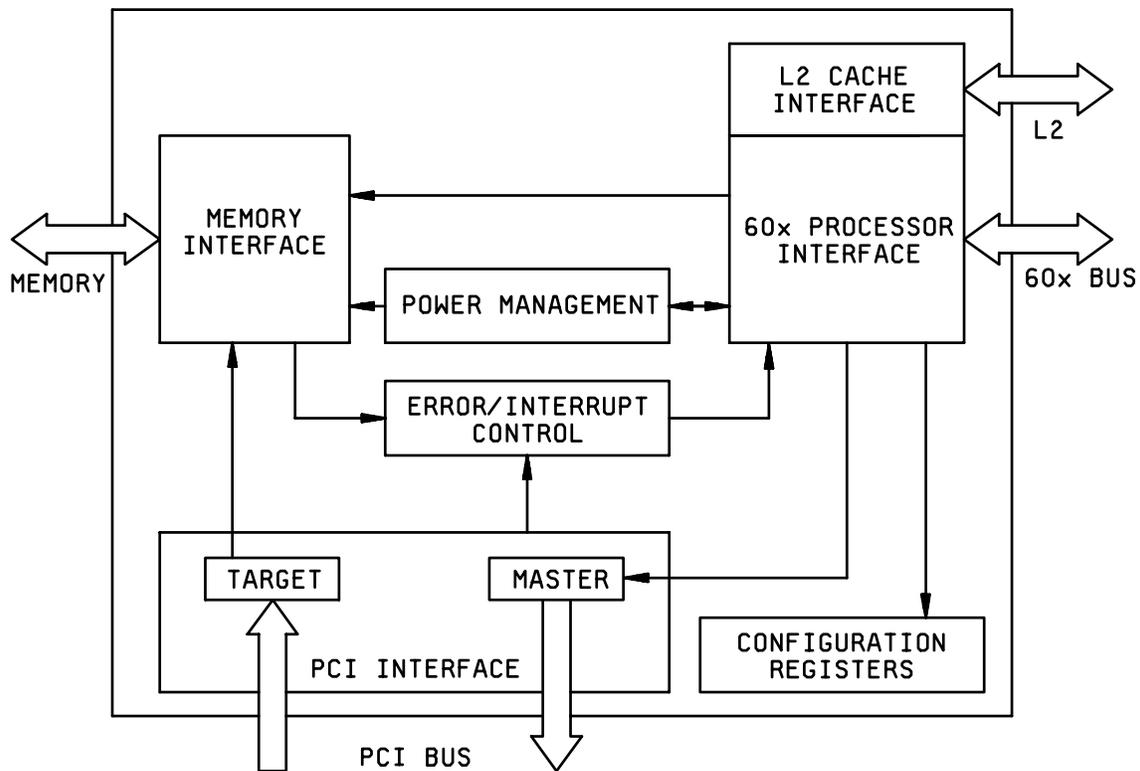
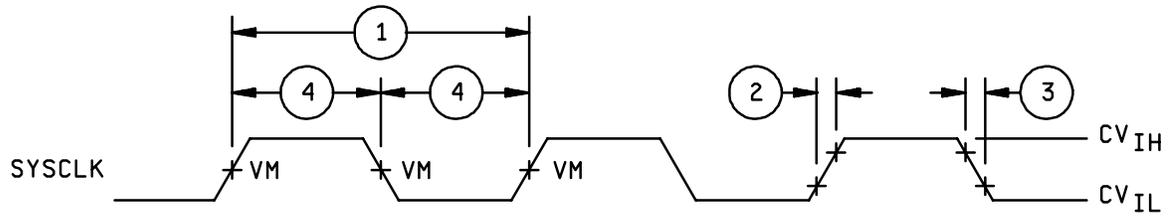


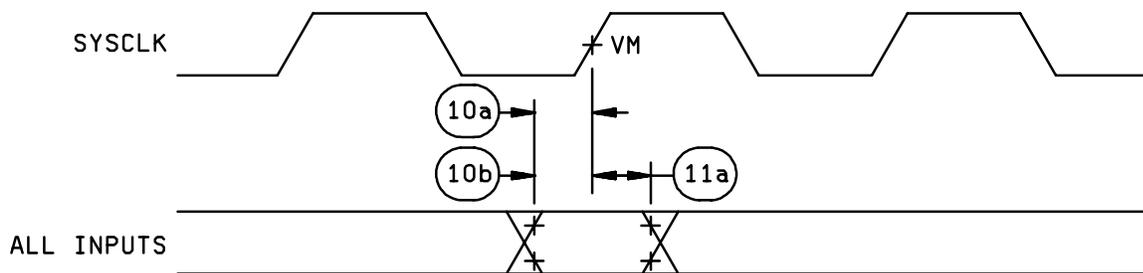
FIGURE 3. Block diagram.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 17

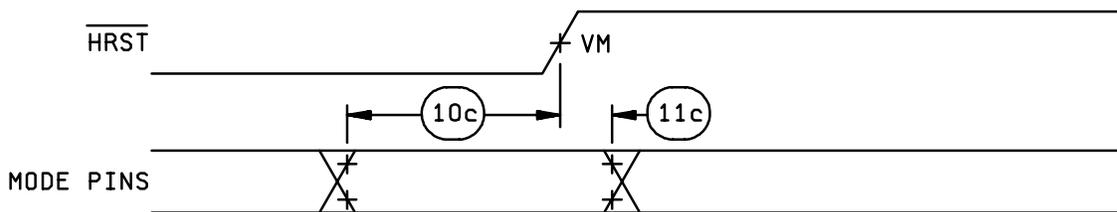
SYSCLK INPUT TIMING DIAGRAM



INPUT TIMING DIAGRAM



MODE SELECT INPUT TIMING DIAGRAM

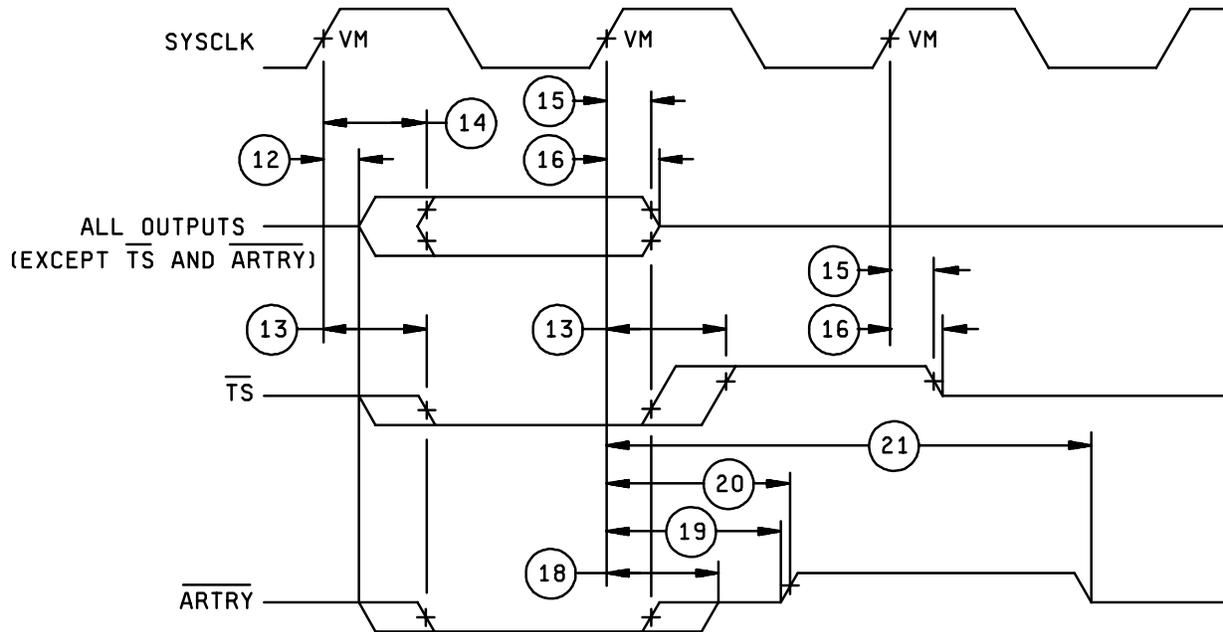


NOTE: VM = 1.4 V.

FIGURE 4. Timing waveforms.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 18

OUTPUT TIMING DIAGRAM

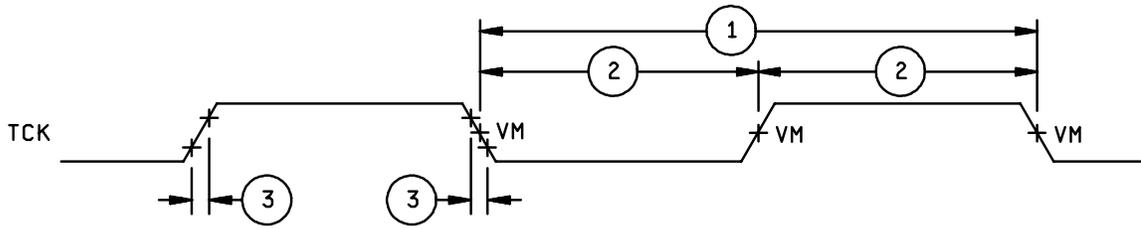


NOTE: VM = 1.4 V.

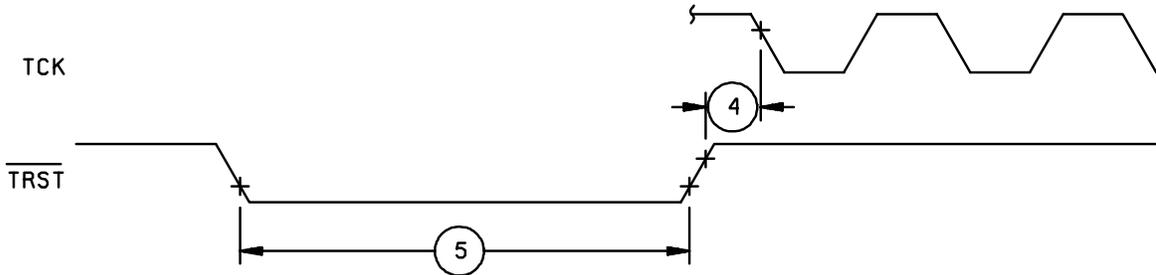
FIGURE 4. Timing waveforms - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 19

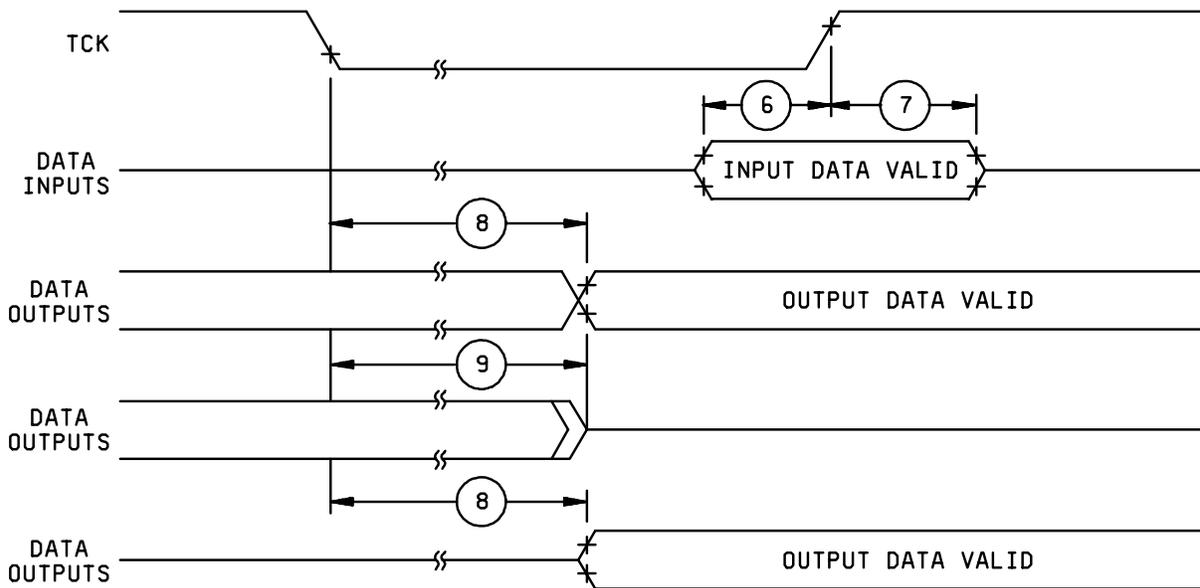
JTAG CLOCK INPUT TIMING DIAGRAM



TRST TIMING DIAGRAM



BOUNDARY-SCAN TIMING DIAGRAM



NOTE: VM = 1.4 V.

FIGURE 4. Timing waveforms - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 20

TEST ACCESS PORT TIMING DIAGRAM

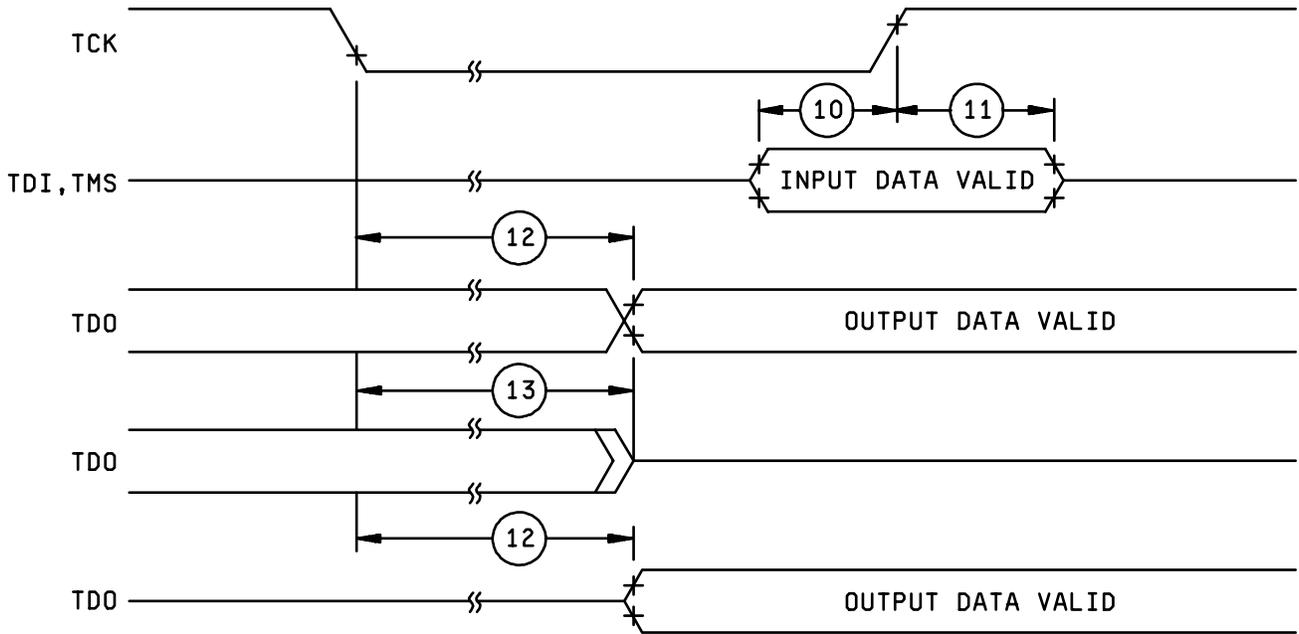


FIGURE 4. Timing waveforms - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 21

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample of 5 devices with zero failures shall be required.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 22

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 <u>1</u> /	1, 2, 3, 7, 8, 9, 10, 11 <u>1</u> /	1, 2, 3, 7, 8, 9, 10, 11 <u>2</u> /
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 23

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and table III herein.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-00535
		REVISION LEVEL A	SHEET 24

TABLE III. Pin description.

Signal	Signal Name	I/O	Signal Description																		
60x processor interface signals																					
A[0-31]	Address bus	O	Specifies the physical address for 60x bus snooping																		
		I	Specifies the physical address of the bus transaction. For burst reads, the address is aligned to the critical double-word address that missed in the instruction or data cache. For burst writes, the address is aligned to the double-word address of the cache line being pushed from the data cache.																		
$\overline{\text{AACK}}$	Address acknowledge	O	Indicates that the address tenure of a transaction is terminated. On the cycle following the assertion of $\overline{\text{AACK}}$, the bus master releases the address-tenure-related signals to a high impedance-state and samples $\overline{\text{ARTRY}}$.																		
		I	Indicates that an externally-controlled L2 cache is terminating the address tenure. On the cycle following the assertion of $\overline{\text{AACK}}$, the bus master releases the address-tenure-related signals to a high-impedance state and samples $\overline{\text{ARTRY}}$.																		
$\overline{\text{ARTRY}}$	Address retry	O	Indicates that the initiating 60x bus master must retry the current address tenure.																		
		I	During a snoop operation, indicates that the 60x either requires the current address tenure to be retried due to a pipeline collision or needs to perform a snoop copy-back operation. During normal 60x bus cycles in a multiprocessor system, indicates that the other 60x or external L2 controller requires the address tenure to be retried.																		
$\overline{\text{BG0}}$	Bus grant 0	O	Indicates that the primary 60x may, with the proper qualification, begin a bus transaction and assume mastership of the address bus.																		
$\overline{\text{BR0}}$	Bus request 0	I	Indicates that the primary 60x requires the bus for a transaction.																		
$\overline{\text{CI}}$	Cache inhibit	I/O	Indicates that an access is caching-inhibited.																		
$\overline{\text{DBG0}}$	Data bus grant 0	O	Indicates that the 60x may, with the proper qualification, assume mastership of the data bus.																		
$\overline{\text{DBGLB}}$	Local bus slave data bus grant	O	Indicates that the 60x processor is prepared to accept data and the local bus slave should drive the data bus.																		
DH[0-31], DL[0-31]	Data bus		The data bus is comprised of two halves - data bus high (DH[0-31]) and data bus low (DL[0-31]). The data bus has the following byte lane assignments: <table border="0" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="text-align: left;"><u>Data Byte</u></th> <th style="text-align: left;"><u>Byte Lane</u></th> </tr> </thead> <tbody> <tr><td>DH[0-7]</td><td>0</td></tr> <tr><td>DH[8-15]</td><td>1</td></tr> <tr><td>DH[16-23]</td><td>2</td></tr> <tr><td>DH[24-31]</td><td>3</td></tr> <tr><td>DL[0-7]</td><td>4</td></tr> <tr><td>DL[8-15]</td><td>5</td></tr> <tr><td>DL[16-23]</td><td>6</td></tr> <tr><td>DL[24-31]</td><td>7</td></tr> </tbody> </table>	<u>Data Byte</u>	<u>Byte Lane</u>	DH[0-7]	0	DH[8-15]	1	DH[16-23]	2	DH[24-31]	3	DL[0-7]	4	DL[8-15]	5	DL[16-23]	6	DL[24-31]	7
		<u>Data Byte</u>	<u>Byte Lane</u>																		
		DH[0-7]	0																		
DH[8-15]	1																				
DH[16-23]	2																				
DH[24-31]	3																				
DL[0-7]	4																				
DL[8-15]	5																				
DL[16-23]	6																				
DL[24-31]	7																				
O	Represents the value of data being driven by the device.																				
I	Represents the state of data being driven by a 60x processor, the local bus slave, the L2 cache, or the memory subsystem.																				

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MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

5962-00535

REVISION LEVEL
A

SHEET
25

TABLE III. Pin description - Continued.

Signal	Signal Name	I/O	Signal Description
60x processor interface signals – Continued			
$\overline{\text{GBL}}$	Global	I/O	Indicates that an access is global and hardware needs to enforce coherency.
$\overline{\text{LBCLAIM}}$	Local bus slave cycle claim	I	Indicates that the local bus slave claims the transaction and is responsible for driving $\overline{\text{TA}}$ during the data tenure.
$\overline{\text{MCP}}$	Machine check	O	Indicates that the device detected a catastrophic error and the 60x processor should initiate a machine check exception.
$\overline{\text{TA}}$	Transfer acknowledge	O	Indicates that the data has been latched for a write operation, or that the data is valid for a read operation, thus terminating the current data beat. If it is the last (or only) data beat, this also terminates the data tenure.
		I	Indicates that the external L2 cache or local bus slave has latched data for a write operation, or is indicating the data is valid for a read operation. If it is the last (or only) data beat, then the data tenure is terminated.
$\overline{\text{TBST}}$	Transfer burst	O	Indicates that a burst transfer is in progress.
		I	Indicates that a burst transfer is in progress.
$\overline{\text{TEA}}$	Transfer error acknowledge	O	Indicates that a bus error has occurred. Assertion of $\overline{\text{TEA}}$ terminates the transaction in progress. An unsupported memory transaction, such as a direct-store access or a graphics read or write, causes the assertion of $\overline{\text{TEA}}$ (provided $\overline{\text{TEA}}$ is enabled).
$\overline{\text{TS}}$	Transfer start	O	Indicates that the device has started a bus transaction, and that the address and transfer attribute signals are valid. Note that the device only initiates a transaction to broadcast the address of a PCI access to memory for snooping purposes.
		I	Indicates that a 60x bus master has begun a transaction, and that the address and transfer attribute signals are valid.
TSIZ[0-2]	Transfer size	O	Specifies the data transfer size for the 60x bus transaction.
		I	Specifies the data transfer size for the 60x bus transaction.
TT[0-4]	Transfer type	O	Specifies the type of 60x bus transfer in progress.
		I	Specifies the type of 60x bus transfer in progress.
$\overline{\text{WT}}$	Write-through	I/O	Indicates that an access is write-through.
$\overline{\text{XATS}}$	Extended address transfer start	I	Indicates that the 60x has started a direct-store access (using the extended transfer protocol). Since direct-store accesses are not supported by the device, the device automatically asserts when $\overline{\text{TEA}}$ and $\overline{\text{XATS}}$ is asserted (provided $\overline{\text{TEA}}$ is enabled).

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

5962-00535

REVISION LEVEL
A

SHEET
26

TABLE III. Pin description - Continued.

Signal	Signal name	I/O	Signal description
Internal L2 controller signals			
$\overline{\text{ADS}}$ $\overline{\text{DALE}}$ $\overline{\text{BRL2}}$	Address strobe	O	For a burst SRAM configuration, indicates to the burst SRAM that the address is valid to be latched.
$\overline{\text{BA0}}$ $\overline{\text{BR3}}$	Burst address 0	I/O	For an asynchronous SRAM configuration, indicates bit 0 of the burst address counter.
$\overline{\text{BA1}}$ $\overline{\text{BAA}}$ $\overline{\text{BGL2}}$	Burst address 1	O	For an asynchronous SRAM configuration, indicates bit 1 of the burst address counter.
$\overline{\text{BAA}}$ $\overline{\text{BA1}}$ $\overline{\text{BGL2}}$	Bus address advance	O	For a burst SRAM configuration, indicates that the burst RAMs should increment their internal addresses.
$\overline{\text{DALE}}$ $\overline{\text{ADS}}$ $\overline{\text{BRL2}}$	Data address latch enable	O	For an asynchronous SRAM configuration, indicates that the external address latch should latch the current 60x bus address.
$\overline{\text{DCS}}$ $\overline{\text{BG3}}$	Data RAM chip select	O	Enables the L2 data RAMs for a read or write operation.
$\overline{\text{DIRTY_IN}}$ $\overline{\text{BR1}}$	Dirty in	I	Indicates that the selected L2 cache line is modified. The polarity of $\overline{\text{DIRTY_IN}}$ is programmable.
$\overline{\text{DIRTY_OUT}}$ $\overline{\text{BG1}}$	Dirty out	O	Indicates that the L2 cache line should be marked as modified. The polarity of $\overline{\text{DIRTY_OUT}}$ is programmable.
$\overline{\text{DOE}}$ $\overline{\text{DBGL2}}$	Data RAM output enable	O	Indicates that the L2 data RAMs should drive the data bus.
$\overline{\text{DWE}} [0-2]$ $\overline{\text{DBG2}}$ $\overline{\text{DBG3}}$	Data RAM write enable	O	Indicates that a write to the L2 data RAMs is in progress. Multiple pins are provided to reduce loading.
$\overline{\text{HIT}}$	Hit	I	Indicates that the L2 cache has detected a hit. The polarity of $\overline{\text{HIT}}$ is programmable.
$\overline{\text{TOE}}$ $\overline{\text{DBG1}}$	Tag output enable	O	Indicates that the tag RAM should drive the L2 tag address onto the address bus.
$\overline{\text{TV}}$ $\overline{\text{BR2}}$	Tag valid	I/O	Indicates that the current L2 cache line should be marked valid. The polarity of $\overline{\text{TV}}$ is programmable
$\overline{\text{TWE}}$ $\overline{\text{BG2}}$	Tag write enable	O	Indicates that the L2 tag address, valid, and dirty bits should be updated.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

5962-00535

REVISION LEVEL
A

SHEET
27

TABLE III. Pin description - Continued.

Signal	Signal name	I/O	Signal description
External L2 controller signals			
$\overline{\text{BGL2}}$ $\overline{\text{BA1}}$ $\overline{\text{BAA}}$	External L2 bus grant	O	Indicates that the external L2 controller has been granted mastership of the 60x address bus.
$\overline{\text{BRL2}}$ $\overline{\text{ADS}}$ $\overline{\text{DALE}}$	External L2 bus request	I	Indicates that the external L2 controller requires mastership of the 60x bus for a transaction.
$\overline{\text{DBGL2}}$ $\overline{\text{DOE}}$	External L2 data bus grant	O	Indicates that the external L2 controller has been granted mastership of the 60x data bus.
$\overline{\text{HIT}}$	External L2 hit	I	Indicates that the current transaction is claimed by the external L2 controller. The external L2 controller will assert $\overline{\text{AACK}}$ and $\overline{\text{TA}}$ for the transaction.
Multiple processor interface signals			
$\overline{\text{BG1}}$ $\overline{\text{DIRTY_OUT}}$	Bus grant 1	O	Indicates that processor 1 may, with the proper qualification, begin a 60x bus transaction and assume mastership of the address bus.
$\overline{\text{BG2}}$ $\overline{\text{TWE}}$	Bus grant 2	O	Indicates that processor 2 may, with the proper qualification, begin a 60x bus transaction and assume mastership of the address bus.
$\overline{\text{BG3}}$ $\overline{\text{DCS}}$	Bus grant 3	O	Indicates that processor 3 may, with the proper qualification, begin a 60x bus transaction and assume mastership of the address bus.
$\overline{\text{BR1}}$ $\overline{\text{DIRTY_IN}}$	Bus request 1	I	Indicates that processor 1 requires mastership of the 60x bus for a transaction.
$\overline{\text{BR2}}$ $\overline{\text{TV}}$	Bus request 2	I	Indicates that processor 2 requires mastership of the 60x bus for a transaction.
$\overline{\text{BR3}}$ $\overline{\text{BA0}}$	Bus request 3	I	Indicates that processor 3 requires mastership of the 60x bus for a transaction.
$\overline{\text{DBG1}}$ $\overline{\text{TOE}}$	Data bus grant 1	O	Indicates that processor 1 may, with the proper qualification, assume mastership of the 60x data bus.
$\overline{\text{DBG2}}$ $\overline{\text{DWE0}}$	Data bus grant 2	O	Indicates that processor 2 may, with the proper qualification, assume mastership of the 60x data bus.
$\overline{\text{DBG3}}$ $\overline{\text{DWE1}}$	Data bus grant 3	O	Indicates that processor 3 may, with the proper qualification, assume mastership of the 60x data bus.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

5962-00535

REVISION LEVEL
A

SHEET
28

TABLE III. Pin description - Continued.

Signal	Signal name	I/O	Signal description
Memory interface signals			
AR0 MA0	ROM address 0	O	Represents address bit 0 of the 8-bit ROM/Flash. Note that AR0 is only supported for ROM bank 0 when configured for an 8-bit ROM/Flash data bus width. The extra address bit allows for up to 2 Mbytes of ROM when using the 8-bit wide data path. Bits 1-8 of the ROM address are provided by AR[1-8] and bits 9-20 of the ROM address are provided by AR[9-20].
AR[1-8] PAR[0-7]	ROM address 1-8	O	Represents bits 1-8 of the ROM/Flash address. The other ROM address bits are provided by AR0 and AR[9-20].
AR9-AR20 MA[1-12]	ROM address 9-20	O	Represents bits 9-20 of the ROM/Flash address (the 12 lowest order bits, with AR20 as the least significant bit (LSB)). Bits 0-8 of the ROM address are provided by AR0 and AR[1-8].
$\overline{\text{BCTL}}$ [0-1]	Buffer control 0-1	O	Used to control external data bus buffers (directional control and high-impedance state) between the 60x bus and memory. Note that external data buffers may be optional for lightly loaded data buses, but buffers are required whenever an L2 cache and ROM/Flash (on the 60x/memory bus) are both in the system or when ECC is used.
$\overline{\text{CAS}}$ [0-7]	Column address strobe 0-7	O	Indicates a memory column address is valid and selects one of the columns in the row. $\overline{\text{CAS0}}$ connects to the most significant byte select. $\overline{\text{CAS7}}$ connects to the least significant byte select.
$\overline{\text{FOE}}$	Flash output enable	O	Enables Flash output for the current read access.
MA0, MA[1-12] AR0, AR[9-20]	Memory address 0-12	O	Represents the row/column multiplexed physical address for DRAMs or EDOs (MA0 is the most significant address bit; MA12 is the least significant address bit). Note that MA0 also functions as the ROM address signal AR0 and MA[1-12] function as the ROM address signals AR[9-20].
$\overline{\text{MDLE}}$	Memory data latch enable	O	Enables the external, latched data buffer for read operations, if such a buffer is used in the system.
PAR[0-7] AR[1-8]	Data parity/ECC	O I	Represents the byte parity or ECC being written to memory (PAR0 is the most significant bit). Represents the byte parity or ECC being read from memory (PAR0 is the most significant bit).
$\overline{\text{PPEN}}$	Parity path read enable	O	Enables external parity/ECC bus buffer or latch for memory read operations.
$\overline{\text{RAS}}$ [0-7]	Row address strobe 0-7	O	Indicates a memory row address is valid and selects one of the rows in the bank.
$\overline{\text{RCS0}}$	ROM/Flash bank 0 select	O	Selects ROM/Flash bank 0 for a read access or Flash bank 0 for a read or write access.
$\overline{\text{RCS1}}$	ROM/Flash bank 1 select	O	Selects ROM/Flash bank 1 for a read access or Flash bank 1 for a read or write access
RTC	Real-time clock	I	External clock source for the memory refresh logic when the device is in the suspend power saving mode.
$\overline{\text{WE}}$	Write enable	O	Enables writing to DRAM, EDO, or Flash.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

5962-00535

REVISION LEVEL
A

SHEET
29

TABLE III. Pin description - Continued.

Signal	Signal name	I/O	Signal description
PCI bus interface signals			
AD[31-0]	Address/data	I/O	Represents the physical address during the address phase of a transaction. During the data phase(s) of a PCI transaction, AD[31-0] contain data. AD[7-0] define the least significant byte and AD[31-24] the most significant byte.
$\overline{C/BE}$ [3-0]	Command/byte enable	O	During the address phase, $\overline{C/BE}$ [3-0] define the PCI bus command. During the data phase, $\overline{C/BE}$ [3-0] are used as byte enables. Byte enables determine which byte lanes carry meaningful data. $\overline{C/BE0}$ applies to the least significant byte.
		I	During the address phase, $\overline{C/BE}$ [3-0] indicates the PCI bus command that another master is sending. During the data phase $\overline{C/BE}$ [3-0] indicate which byte lanes are valid.
\overline{DEVSEL}	Device select	O	Indicates that the device has decoded the address and is the target of the current access.
		I	Indicates that some PCI agent (other than the device) has decoded its address as the target of the current access.
$\overline{FLSHREQ}$	Flush request	I	Indicates that a device needs to have the device flush all of its current operations.
\overline{FRAME}	Frame	O	Indicates that the device, acting as a PCI master, is initiating a bus transaction.
		I	Indicates that another PCI master is initiating a bus transaction.
\overline{GNT}	PCI bus grant	I	Indicates that the device has been granted control of the PCI bus. Note that \overline{GNT} is a point-to-point signal. Every master has its own \overline{GNT} signal.
\overline{IRDY}	Initializer ready	O	Indicates that the device, acting as a PCI master, can complete the current data phase of a PCI transaction. During a write, the device asserts \overline{IRDY} to indicate that valid data is present on AD[31-0]. During a read, the device asserts \overline{IRDY} to indicate that it is prepared to accept data.
		I	Indicates another PCI master is able to complete the current data phase of the transaction.
$\overline{ISA_MASTER}$	ISA master	I	Indicates that an ISA master is requesting system memory.
\overline{LOCK}	Lock	I	Indicates that a master is requesting exclusive access to memory, which may require multiple transactions to complete.
\overline{MEMACK}	Memory acknowledge	O	Indicates that the device has flushed all of its current operations and has blocked all 60x transfers except snoop copy-back operations. The device asserts \overline{MEMACK} in response to assertion of $\overline{FLSHREQ}$, after the flush is complete.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

5962-00535

REVISION LEVEL
A

SHEET
30

TABLE III. Pin description - Continued.

Signal	Signal name	I/O	Signal description
PCI bus interface signals - Continued			
PAR	Parity	O	Asserted indicates odd parity across the AD[31-0] and $\overline{C/BE}$ [3-0] signals during address and data phases. Negated indicates even parity.
		I	Asserted indicates odd parity driven by another PCI master or the PCI target during read data phases. Negated indicates even parity.
\overline{PERR}	Parity error	O	Indicates that another PCI agent detected a data parity error.
		I	Indicates that another PCI agent detected a data parity error.
\overline{PIRQ}	Modified memory interrupt request	O	In emulation mode, indicates that a PCI write has occurred to system memory that has not been recorded by software.
\overline{REQ}	PCI bus request	O	Indicates that the device is requesting control of the PCI bus to perform a transaction. Note that \overline{REQ} is a point-to-point signal. Every master has its own \overline{REQ} signal.
\overline{SERR}	System error	O	Indicates that an address parity error or some other system error (where the result will be a catastrophic error) was detected.
		I	Indicates that another target has detected a catastrophic error.
\overline{STOP}	Stop	O	Indicates that the device, acting as the PCI target, is requesting that the PCI bus master stop the current transaction.
		I	Indicates that some other PCI agent is requesting that the PCI initiator stop the current transaction.
\overline{TRDY}	Target ready	O	Indicates that the device, acting as a PCI target, can complete the current data phase of a PCI transaction. During a read, the device asserts \overline{TRDY} to indicate that valid data is present on AD[31-0]. During a write, the device asserts \overline{TRDY} to indicate that it is prepared to accept data.
		I	Indicates that another PCI target is able to complete the current data phase of a transaction.
Interrupt, clocking, and power management signals			
\overline{CKO} $\overline{DWE2}$	Test clock	O	CKO provides a means to monitor the internal PLL output or the bus clock frequency. The CKO clock should be used for testing purposes only. It is not intended as a reference clock signal.
\overline{HRST}	Hard reset	I	Initiates a complete hard reset of the device. During assertion, all bidirectional signals are released to a high-impedance state and all output signals are either in a high-impedance or inactive state.
NMI	Nonmaskable interrupt	I	Indicates that an external device (typically an interrupt controller) has detected a catastrophic error. In response, the device asserts \overline{MCP} on the 60x processor bus.
\overline{QACK}	Quiescent acknowledge	O	Indicates that the device is in a low-power state. All bus activity that requires snooping has terminated, and the 60x processor may enter a low-power state.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

5962-00535

REVISION LEVEL
A

SHEET
31

TABLE III. Pin description - Continued.

Signal	Signal name	I/O	Signal description
Interrupt, clocking, and power management signals - Continued			
$\overline{\text{QREQ}}$	Quiescent request	I	Indicates that a 60x processor is requesting that all bus activity involving snoop operations pause or terminate so that the 60x processor may enter a low-power state.
$\overline{\text{SUSPEND}}$	Suspend	I	Activates the suspend power-saving mode.
SYSCLK	System clock	I	SYSCLK sets the frequency of operation for the PCI bus, and provides a reference clock for the phase-locked loop (PLL) in the device. SYSCLK is used to synchronize bus operations.
IEEE 1149.1 boundary-scan signals			
TCK	JTAG test clock	I	Input signals to the test access port (TAP) are clocked in on the rising edge of TCK. Changes to the TAP output signals occur on the falling edge of TCK. The test logic allows TCK to be stopped.
TDO	JTAG test data output	O	The contents of the selected internal instructions or data register are shifted out onto this signal on the falling edge of TCK. TDO will remain in a high-impedance state except when scanning of data is in progress.
TDI	JTAG test data input	I	The value presented on this signal on the rising edge of TCK is clocked into the selected JTAG test instruction or data register.
TMS	JTAG test mode select	I	This signal is decoded by the internal JTAG TAP controller to distinguish the primary operation of the test support circuitry.
$\overline{\text{TRST}}$	JTAG test reset	I	This input causes asynchronous initialization of the internal JTAG TAP controller.
Configuration signals			
Signal		I/O	Configuration
$\overline{\text{DBG0}}$		I	High - configures the device for address map A. Low - configures the device for address map B.
$\overline{\text{FOE}}$		I	High - configures ROM bank 0 for an 8-bit data bus width. Low - configures ROM bank 0 for an 64-bit data bus width. Note that the data bus width for ROM bank 1 is always 64 bits.
PLL[0-3]		I	High/Low - configuration for the PLL clock mode.
$\overline{\text{RCS0}}$		I	High - indicates ROM is located on the 60x processor/memory data bus. Low - indicates ROM is located on the PCI bus.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

5962-00535

REVISION LEVEL
A

SHEET
32

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 03-06-26

Approved sources of supply for SMD 5962-00535 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and/or QML-38535 during the next revision. MIL-HDBK-103 and/or QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and/or QML-38535.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-0053501QXA	F8385	TSPC106AMGSB/Q66CG
5962-0053502QXA	F8385	TSPC106AMGSB/Q83CG

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

F8385

Vendor name
and address

Atmel Grenoble
Avenue de Rochepleine, BP123
38521 Saint-Egreve, France

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