

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Paragraph 1.2.2, Circuit functions for device types 03 and 04, remove +5 V logic. Paragraph 1.4, correct Transceiver supply voltage range (V <sub>CC</sub> ) to +4.75 V dc to +5.25 V dc, for all device types. Table I, conditions column, remove V <sub>CC</sub> throughout. Table I, conditions column, correct +5 V logic = +5.25 V throughout.	01-10-02	Raymond Monnin

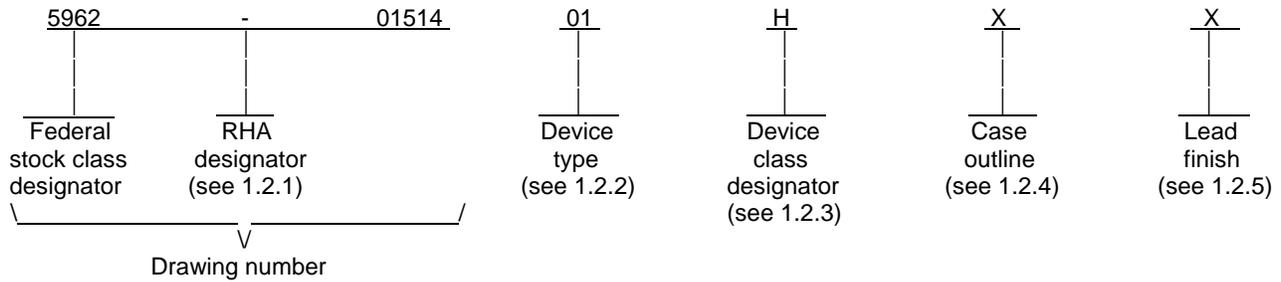
REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A	A	A									
SHEET	15	16	17	18	19	20	21	22	23	24	25									
REV STATUS OF SHEETS				REV	A			A	A	A	A	A	A	A	A	A	A	A	A	A
				SHEET	1			2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Gary Zahn	<p align="center"><b>DEFENSE SUPPLY CENTER COLUMBUS</b>  <b>POST OFFICE BOX 3990</b>  <b>COLUMBUS, OHIO 43216-5000</b>  <a href="http://www.dsccl.dla.mil">http://www.dsccl.dla.mil</a></p>																	
<p align="center"><b>STANDARD MICROCIRCUIT DRAWING</b></p> <p align="center">THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Michael C. Jones																		
	APPROVED BY Raymond Monnin	<p align="center">MICROCIRCUIT, HYBRID, LINEAR,  MIL-STD-1553, BC/RTU/MT, MULTIPLEXED  TERMINAL</p>																	
	DRAWING APPROVAL DATE 01-08-01																		
	REVISION LEVEL A		SIZE A	CAGE CODE 67268	<p align="center"><b>5962-01514</b></p>														
SHEET			1 OF 25																

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	BU-61865X3	MIL-STD-1553, BC/RT/MT, 64K RAM, +5 V transceiver, +5 V logic, +5 V RAM
02	BU-61865X4	MIL-STD-1553, BC/RT/MT, 64K RAM, +5 V transceiver, +5 V logic, +5 V RAM, McAir compatible
03	BU-61864X3	MIL-STD-1553, BC/RT/MT, 64K RAM, +5 V transceiver, +3.3 V logic, +5 V RAM
04	BU-61864X4	MIL-STD-1553, BC/RT/MT, 64K RAM, +5 V transceiver, +3.3 V logic, +5 V RAM, McAir compatible
05	BU-61745X3	MIL-STD-1553, RT, 4K RAM, +5 V transceiver, +5 V logic
06	BU-61745X4	MIL-STD-1553, RT, 4K RAM, +5 V transceiver, +5 V logic, McAir compatible
07	BU-61743X3	MIL-STD-1553, RT, 4K RAM, +5 V transceiver, +3.3 V logic
08	BU-61743X4	MIL-STD-1553, RT, 4K RAM, +5 V transceiver, +3.3 V logic, McAir compatible
09	BU-61705X3	MIL-STD-1553, Simple system RT, +5 V transceiver. +5 V logic
10	BU-61705X4	MIL-STD-1553, Simple system RT, +5 V transceiver. +5 V logic, McAir compatible
11	BU-61703X3	MIL-STD-1553, Simple system RT, +5 V transceiver. +3.3 V logic
12	BU-61703X4	MIL-STD-1553, Simple system RT, +5 V transceiver. +3.3 V logic, McAir compatible
13	BU-61845X3	MIL-STD-1553, BC/RT/MT, 4K RAM, +5 V transceiver, +5 V logic
14	BU-61845X4	MIL-STD-1553, BC/RT/MT, 4K RAM, +5 V transceiver, +5 V logic, McAir compatible
15	BU-61843X3	MIL-STD-1553, BC/RT/MT, 4K RAM, +5 V transceiver, +3.3 V logic
16	BU-61843X4	MIL-STD-1553, BC/RT/MT, 4K RAM, +5 V transceiver, +3.3 V logic, McAir compatible

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1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

<u>Device class</u>	<u>Device performance documentation</u>
K	Highest reliability class available. This level is intended for use in space applications.
H	Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required.
G	Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C, and D).
E	Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance.
D	Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
M	See figure 1	72	Quad flat package with lead forming
T	See figure 1	72	Quad flat package with tie bars

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. <sup>1/</sup>

Transceiver supply voltage range ( $V_{CC}$ ) .....	-0.3 V dc to +7.0 V dc
+5 V RAM supply voltage range (Device types 01 through 04) .....	-0.3 V dc to +6.0 V dc
Logic supply voltage range:	
+5 V logic (Device types 01, 02, 05, 06, 09, 10, 13, and 14) .....	-0.3 V dc to +6.0 V dc
+3.3 V logic (Device types 03, 04, 07, 08, 11, 12, 15, and 16) .....	-0.3 V dc to +6.0 V dc
Voltage input range for +5 V logic (Device types 01, 02, 05, 06, 09, 10, 13, and 14) .....	-0.3 V dc to +6.0 V dc
Voltage input range for +3.3 V logic (Device types 03, 04, 07, 08, 11, 12, 15, and 16) ....	-0.3 V dc to +6.0 V dc
Power dissipation ( $P_D$ ): <sup>2/</sup> <sup>3/</sup> <sup>4/</sup>	
Device types 01, 03, 05, 07, 09, 11, 13, and 15 .....	1.22 W
Device types 02, 04, 06, 08, 10, 12, 14, and 16 .....	1.48 W
Storage temperature range .....	-65°C to +150°C
Lead temperature (soldering, 10 seconds).....	+300°C
Thermal resistance, junction to case( $\theta_{JC}$ ).....	20°C/W <sup>3/</sup>

<sup>1/</sup> Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

<sup>2/</sup> Applies up to  $T_C = +125^\circ\text{C}$ .

<sup>3/</sup> Hottest die.

<sup>4/</sup> Assumes 100 percent transmitter duty cycle on one channel and 0 percent duty cycle on the other channel.

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1.4 Recommended operating conditions.

Transceiver supply voltage range ( $V_{CC}$ ) .....	+4.75 V dc to +5.25 V dc
+5 V RAM supply voltage range (Device types 01 through 04) .....	+4.5 V dc to +5.5 V dc
Logic supply voltage range:	
+5 V logic (Device types 01, 02, 05, 06, 09, 10, 13, and 14) .....	+4.5 V dc to +5.5 V dc
+3.3 V logic (Device types 03, 04, 07, 08, 11, 12, 15, and 16) .....	+3.0 V dc to +3.6 V dc
Minimum logic high input voltage ( $V_{IH}$ ) .....	2.1 V dc
Maximum logic low input voltage ( $V_{IL}$ ) .....	0.7 V dc
Operating frequency ( $F_{OP}$ ) .....	10, 12, 16, or 20 MHz
Case operating temperature range ( $T_C$ ) .....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.  
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Furthermore, the manufacturer may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

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3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Pin functions. The pin functions shall be as specified in table III.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked in MIL-HDBK-103 and QML-38534.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2)  $T_A$  as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
<b>Supply current drain (Total)</b>							
Supply current, Idle <u>1/</u>	I <sub>CC1</sub>	+5 V logic = +5.25 V for device types 01, 02, 05, 06, 09, 10, 13 and 14. +3.3 V logic = +3.6 V for device types 03, 04, 07, 08, 11, 12, 15, and 16.	1,2,3	01,02, 09-12	5	180	mA
				03,04	5	120	
				05,06, 13,14	5	160	
				07,08, 15,16	5	100	
Supply current, channel A = 25% duty cycle channel B = idle <u>1/</u>	I <sub>CC2</sub>	+5 V logic = +5.25 V for device types 01, 02, 05, 06, 09, 10, 13, and 14. +3.3 V logic = +3.6 V for device types 03, 04, 07, 08, 11, 12, 15, and 16.	1,2,3	01,02, 09-12	5	296	mA
				03,04	5	236	
				05,06, 13,14	5	226	
				07,08, 15,16	5	216	
Supply current, channel A = idle channel B = 25% duty cycle <u>1/</u>	I <sub>CC3</sub>	+5 V logic = +5.25 V for device types 01, 02, 05, 06, 09, 10, 13, and 14. +3.3 V logic = +3.6 V for device types 03, 04, 07, 08, 11, 12, 15, and 16.	1,2,3	01,02, 09-12	5	296	mA
				03,04	5	236	
				05,06, 13,14	5	226	
				07,08, 15,16	5	216	
<b>Logic</b>							
Low level input current (All signals except CLK_IN)	I <sub>IL</sub>	+5 V logic = +5.25 V, V <sub>IN</sub> = 0.4 V	1,2,3	01,02, 05,06, 09,10, 13,14	-350	-50	μA
		+3.3 V logic = +3.6 V, V <sub>IN</sub> = 0.4 V	1,2,3	03,04, 07,08, 11,12, 15,16	-350	-33	μA
See footnotes at end of table.							
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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logic - Continued.							
High level input current (All signals except CLK_IN)	I <sub>IH</sub>	+5 V logic = +5.25 V, V <sub>IN</sub> = 2.7 V	1,2,3	01,02, 05,06, 09,10, 13,14	-350	-50	μA
		+3.3 V logic = +3.6 V, V <sub>IN</sub> = 2.7 V	1,2,3	03,04, 07,08, 11,12, 15,16	-350	-33	μA
Output voltage low (All signals except CLK_IN)	V <sub>OL</sub>	+5 V logic = +5.25 V, V <sub>IH</sub> = 2.7 V, V <sub>IL</sub> = 0.2 V, I <sub>OL</sub> = max	1,2,3	01,02, 05,06, 09,10, 13,14		0.4	V
		+3.3 V logic = +3.6 V, V <sub>IH</sub> = 2.7 V, V <sub>IL</sub> = 0.2 V, I <sub>OL</sub> = max	1,2,3	03,04, 07,08, 11,12, 15,16		0.4	V
Output voltage high (All signals except CLK_IN)	V <sub>OH</sub>	+5 V logic = +4.75 V, V <sub>IH</sub> = 2.7 V, V <sub>IL</sub> = 0.2 V, I <sub>OH</sub> = max	1,2,3	01,02, 05,06, 09,10, 13,14	2.4		V
		+3.3 V logic = +3.0 V, V <sub>IH</sub> = 2.7 V, V <sub>IL</sub> = 0.2 V, I <sub>OH</sub> = max	1,2,3	03,04, 07,08, 11,12, 15,16	2.4		V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Pulse widths.							
$\overline{IOEN}$ low pulse width (memory read)	t <sub>PW1</sub>	+5 V logic = +5.25 V for device types 01, 02, 05, 06, 09, 10, 13, and 14. +3.3 V logic = +3.6 V for device types 03, 04, 07, 08, 11, 12, 15, and 16.	9,10,11	01-08	475	625	ns
$\overline{READYD}$ low pulse width (memory read)	t <sub>PW2</sub>			All	225	375	ns
$\overline{MEMOE}$ low pulse width (memory read)	t <sub>PW3</sub>			All	350	500	ns
$\overline{MEMWR}$ low pulse width (memory write)	t <sub>PW4</sub>			All	37	87	ns
$\overline{INCMD}$ low pulse width (receive command)	t <sub>PW5</sub>			All	45.4	47.5	μs
$\overline{INCMD}$ low pulse width (transmit command)	t <sub>PW6</sub>			All	45.4	47.5	μs
$\overline{INT}$ low pulse width	t <sub>PW7</sub>			01-08	450	550	ns
$\overline{DTREQ}$ low pulse width	t <sub>PW8</sub>			All	2.07	2.19	μs
$\overline{DTACK}$ low pulse width	t <sub>PW9</sub>			All	2.0	2.23	μs
Functional tests		+5 V logic = +5.25 V for device types 01, 02, 05, 06, 09, 10, 13, and 14. +3.3 V logic = +3.6 V for device types 03, 04, 07, 08, 11, 12, 15, and 16. See 4.3.1b.	7,8	All			Pass/ fail
Receiver/Transmitter.							
Receiver threshold	V <sub>TH</sub>	+5 V logic = +5.25 V for device types 01, 02, 05, 06, 09, 10, 13, and 14. +3.3 V logic = +3.6 V for device types 03, 04, 07, 08, 11, 12, 15, and 16. Transformer coupled into a 70 Ω resistive load	4,5,6	All	200	860	mVp-p
Transmitter differential output voltage	V <sub>O</sub>		4,5,6	All	18	27	Vp-p
Transmitter output rise time	t <sub>R</sub>		4,5,6	All	100	300	ns
Transmitter output fall time	t <sub>F</sub>		4,5,6	All	100	300	ns
Transmitter output offset voltage <sup>1/</sup>	V <sub>OS</sub>		4,5,6	All	-250	+250	mVp-p
<sup>1/</sup> Measured at the following pins: Case outlines M and T: pins 20, 37, and 72. <sup>2/</sup> Parameter shall be tested as part of the initial characterization of these devices and after design and process changes. Parameter shall be guaranteed to the limits specified in table I for all lots not specifically tested.							
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Case outline M.

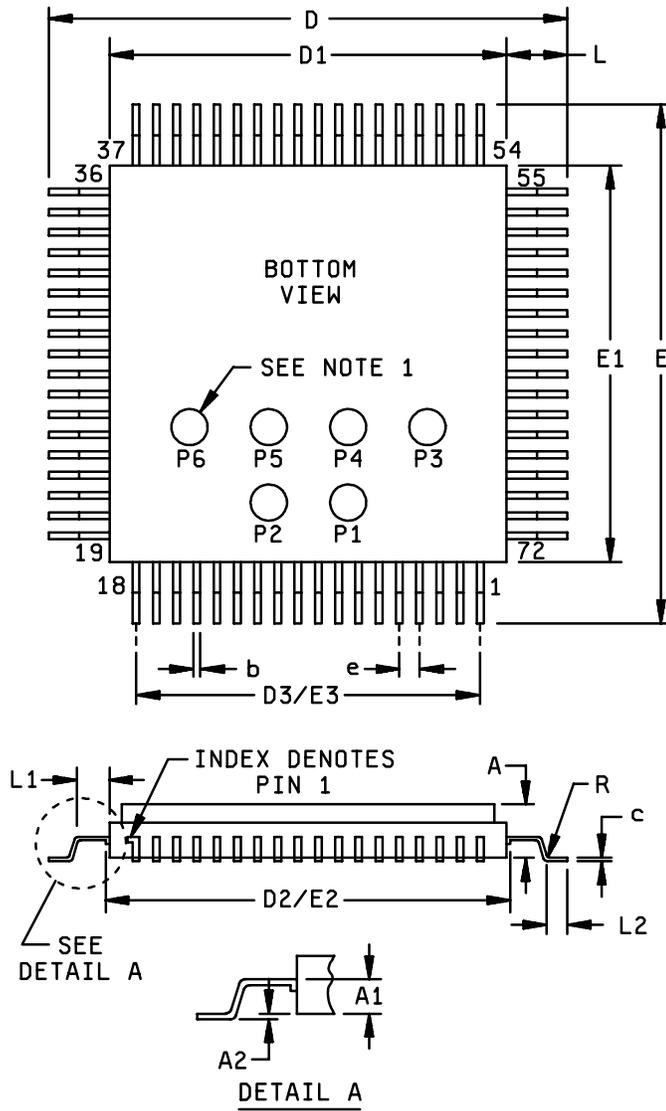


FIGURE 1. Case outline(s).

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Case outline M.

Symbol	Millimeters		Inches	
	Minimum	Maximum	Minimum	Maximum
A	---	3.94	---	0.155
A1	1.14	1.40	0.045	0.055
A2	0.05	0.41	0.002	0.016
b	0.41	0.51	0.016	0.020
c	0.20	0.30	0.008	0.012
e	1.14	1.40	0.045	0.055
D/E	34.54	35.56	1.360	1.400
D1/E1	25.15	25.65	0.990	1.010
D2/E2	25.65	26.37	1.010	1.038
D3/E3	18.35	25.40	0.842	0.858
L	4.57	5.08	0.180	0.200
L1	2.03	---	0.080	---
L2	1.27	---	0.050	---
R	---	0.30	---	0.012

NOTES:

1. There are six test pads located on the bottom of the package. Each pad measures 0.100 inch (2.54 mm) in diameter. These pads are recessed so as to not interfere when mounting the package.
2. The U.S. government preferred system of measurement is the metric SI. This case outline was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
3. Package material is Alumina (AL<sub>2</sub>O<sub>3</sub>).

FIGURE 1. Case outline(s) - Continued.

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Case outline T.

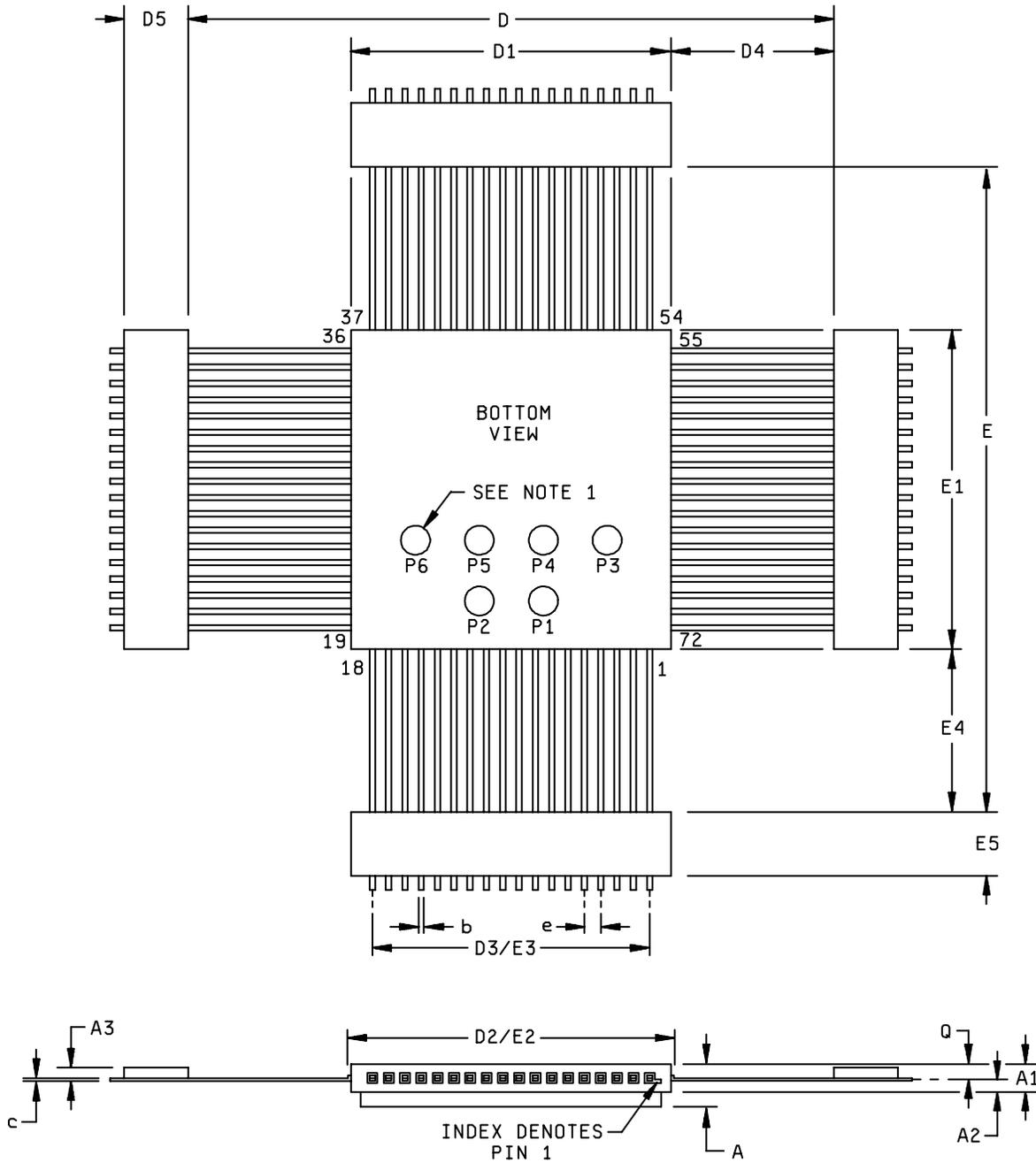


FIGURE 1. Case outline(s) - Continued.

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Case outline T - Continued.

Symbol	Millimeters		Inches	
	Minimum	Maximum	Minimum	Maximum
A	---	3.94	---	0.155
A1	2.03	2.54	0.080	0.100
A2	1.14	1.40	0.045	0.055
A3	0.76	1.02	0.030	0.040
b	0.41	0.51	0.016	0.020
c	0.20	0.30	0.008	0.012
e	1.14	1.40	0.045	0.055
D/E	50.42	51.18	1.985	2.015
D1/E1	25.15	25.65	0.990	1.010
D2/E2	25.65	26.37	1.010	1.038
D3/E3	18.35	25.40	0.842	0.858
D4/E4	12.19	13.21	0.480	0.520
D5/E5	4.95	5.21	0.195	0.205

NOTES:

1. There are six test pads located on the bottom of the package. Each pad measures 0.100 inch (2.54 mm) in diameter. These pads are recessed so as to not interfere when mounting the package.
2. The U.S. government preferred system of measurement is the metric SI. This case outline was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
3. Package material is Alumina (AL<sub>2</sub>O<sub>3</sub>).

FIGURE 1. Case outline(s) - Continued.

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Device types	01 through 08 and 13 through 16		
Case outlines	M and T		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	<u>MEM/REG</u>	37	+5 V / +3.3 V LOGIC
2	MSTCLR	38	D1
3	A11	39	D4
4	A10	40	RTADP
5	TX/RX_A	41	RTAD1
6	<u>A8</u>	42	D0
7	TX/RX_A	43	D2
8	A14/CLK_SEL_0	44	D3
9	A4	45	D5
10	A3	46	D8
11	A7	47	D7
12	A2	48	D13
13	TX/RX_B	49	D12
14	ADDR_LAT/MEMOE	50	D14
15	<u>A0</u>	51	D9
16	TX/RX_B	52	D11
17	LOGIC GND	53	D15
18	LOGIC GND	54	D10
19	LOGIC GND	55	<u>TRANSPARENT/BUFFERED</u>
20	+5 V V <sub>CC</sub> CH B	56	<u>READYD</u>
21	RTAD2	57	<u>INT</u>
22	<u>A6</u>	58	IOEN
23	MEMWR/ZEROWAIT	59	TX_INH_A
		60	TX_INH_B
24	<u>DTREQ/16/8-bit</u>		
25	INCMD/MCRST	61	<u>SELECT</u>
26	+5 V RAM / UPADDREN	62	<u>STRBD</u>
27	<u>A1</u>	63	<u>RD/WR</u>
28	<u>MENENA_IN/TRIGGER_SEL</u>	64	DTGRT/MSB/LSB
29	DTACK/POLARITY_SEL	65	LOGIC GND
30	CLOCK_IN	66	A15 / CLK_SEL_1
31	RT_AD_LAT	67	LOGIC GND
		68	A5
32	<u>SSFLAG/EXT_TRIG</u>	69	A9
33	RTAD0	70	A12 / RTBOOT
34	RTAD3	71	A13 / +5 V / +3.3 V LOGIC
35	RTAD4	72	+5 V V <sub>CC</sub> CH A
36	D6		

NOTES:

1. For device types 01, 02, 03, and 04; pin 8 is A14. For device types 05 through 08 and 13 through 16; pin 8 can be either A14 or CLK-SEL-0.
2. For device types 01, 02, 03, and 04; pin 26 is +5 V RAM. For device types 05 through 08 and 13 through 16; pin 26 is UPADDREN.
3. For device types 01, 02, 03, and 04; pin 66 is A15. For device types 05 through 08 and 13 through 16; pin 66 can be either A15 or CLK-SEL-1.
4. For device types 01, 02, 03, and 04; pin 70 is A12. For device types 05 through 08 and 13 through 16; pin 70 can be either A12 or RTBOOT.
5. For device types 01, 02, 03, and 04; pin 71 is A13. For device types 05 through 08 and 13 through 16; pin 71 can be either A13 or +5 V or +3.3 V LOGIC.

FIGURE 2. Terminal connections.

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Device types	09 through 12		
Case outlines	M and T		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{\text{RT\_AD\_ERR}}$	37	+5 V / +3.3 V LOGIC
2	$\overline{\text{MSTCLR}}$	38	D1
3	$\overline{\text{L\_BO}}$	39	D4
4	$\overline{\text{T/R}}$	40	RTADP
5	$\overline{\text{TX/RX\_A}}$	41	RTAD1
6	$\overline{\text{SA3}}$	42	D0
7	$\overline{\text{TX/RX\_A}}$	43	D2
8	$\overline{\text{CLK\_SEL\_0}}$	44	D3
9	WC4	45	D5
10	WC3	46	D8
11	SA2	47	D7
12	WC2	48	D13
13	$\overline{\text{TX/RX\_B}}$	49	D12
14	$\overline{\text{MEMOE}}$	50	D14
15	$\overline{\text{WC0}}$	51	D9
16	$\overline{\text{TX/RX\_B}}$	52	D11
17	GND	53	D15
18	GND	54	$\overline{\text{D10}}$
19	GND	55	BUSY
20	+5 V $V_{CC}$ CH B	56	$\overline{\text{RTACTIVE}}$
21	RTAD2	57	HS_FAIL
22	$\overline{\text{SA1}}$	58	$\overline{\text{RT\_FAIL}}$
23	$\overline{\text{MEMWR}}$	59	TX_INH
24	$\overline{\text{DTREQ}}$	60	$\overline{\text{GBR}}$
25	INCMD	61	$\overline{\text{SRV\_RQST}}$
26	GND	62	$\overline{\text{ILLEGAL}}$
27	$\overline{\text{WC1}}$	63	BRO_ENA
28	$\overline{\text{MSG\_ERR}}$	64	$\overline{\text{DTGRT}}$
29	$\overline{\text{DTACK}}$	65	GND
30	CLOCK_IN	66	CLK_SEL_1
31	$\overline{\text{RT\_AD\_LAT}}$	67	GND
32	$\overline{\text{SSFLAG}}$	68	SA
33	RTAD0	69	$\overline{\text{SA4}}$
34	RTAD3	70	AUTO_CFG
35	RTAD4	71	GND
36	D6	72	+5 V $V_{CC}$ CH A

NOTES:

1. For device types 09 and 10, pin 37 is +5 V LOGIC. For device types 11 and 12, pin 37 is +3.3 V LOGIC.

FIGURE 2. Terminal connections - Continued.

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TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,2,3,4,5,6,7,8,9,10,11
Final electrical parameters	1*,2,3,4,5,6,7,8,9,10,11
Group A test requirements	1,2,3,4,5,6,7,8,9,10,11
Group C end-point electrical parameters	1,2,3,4,5,6,7,8,9,10,11
End-point electrical parameters for radiation hardness assurance (RHA) devices	Not applicable

\* PDA applies to subgroup 1.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 7 and 8 shall consist of verifying the functionality of the device. It forms a part of the vendors test tape and shall be maintained and available from the approved source of supply.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test, method 1005 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
  - (2) T<sub>A</sub> as specified in accordance with table I of method 1005 of MIL-STD-883.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-PRF-38534.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Post Office Box 3990, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

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TABLE III. Pin functions.

Terminal symbol	I/O	Description
Power supply and ground connections.		
+5 V V <sub>CC</sub> CH A	-	+5 V power supply connection for the A channel transceiver.
+5 V V <sub>CC</sub> CH B	-	+5 V power supply connection for the B channel transceiver.
+5 V / +3.3 V LOGIC	-	+5 V Logic power supply connection for device types 01, 02, 05, 06, 09, 10, 13, and 14. +3.3 V Logic power supply connection for device types 03, 04, 07, 08, 11, 12, 15, and 16.
+5 V RAM	-	+5 V power supply connection for device types 01 through 04. For device types 05 through 08 and 13 through 16 this pin assumes the function UPADDREN.
LOGIC GND	-	Logic ground. Power supply return for the digital logic section. (For device types 01 through 08 and 13 through 16).
GND	-	Ground. (For device types 09 through 12).
MIL-STD-1553 Isolation transformer interface.		
TX/RX_A	I/O	Transmit/receive transceiver-A. Noninverted input/output to the coupling transformer that connects to the A channel of the 1553 bus.
$\overline{\text{TX/RX}}_A$	I/O	Transmit/receive transceiver-A. Inverted input/output to the coupling transformer that connects to the A channel of the 1553 bus.
TX/RX_B	I/O	Transmit/receive transceiver-B. Noninverted input/output to the coupling transformer that connects to the B channel of the 1553 bus.
$\overline{\text{TX/RX}}_B$	I/O	Transmit/receive transceiver-B. Inverted input/output to coupling transformer that connects to channel B of the 1553 bus.
Remote terminal (RT) address.		
RTAD4 (MSB)	I	Remote terminal address bit 4.
RTAD3	I	Remote terminal address bit 3.
RTAD2	I	Remote terminal address bit 2.
RTAD1	I	Remote terminal address bit 1.
RTAD0 (LSB)	I	Remote terminal address bit 0.
RTADP	I	Remote terminal address parity input.
RT_AD_LATCH	I	RT Address Latch. Input signal used to control the device type's internal RT Address Latch. A logic 0 configures the device type to have a hardwired ( transparent ) RT address. A logic 1 configures the device type for the latched RT address mode. The value presented on the RTAD4, RTAD0, RTADP inputs is latched on the rising edge of RT_AD_LAT.
$\overline{\text{RT\_AD\_ERR}}$	O	Remote Terminal Address Error. An output signal that reflects the parity combination of the RTAD4 through 0 inputs and RTADP input. A high level indicates odd (correct) parity. A low level indicates even (incorrect) parity. If RT_AD_ERR is low, then the device type will not recognize any valid Command Word received to its own RT address. (For device types 09, 10, 11, and 12).

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TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description															
Data bus.																	
D15 (MSB)	I/O	Data bus bit 15.															
D14	I/O	Data bus bit 14.															
D13	I/O	Data bus bit 13.															
D12	I/O	Data bus bit 12.															
D11	I/O	Data bus bit 11.															
D10	I/O	Data bus bit 10.															
D9	I/O	Data bus bit 9.															
D8	I/O	Data bus bit 8.															
D7	I/O	Data bus bit 7.															
D6	I/O	Data bus bit 6.															
D5	I/O	Data bus bit 5.															
D4	I/O	Data bus bit 4.															
D3	I/O	Data bus bit 3.															
D2	I/O	Data bus bit 2.															
D1	I/O	Data bus bit 1.															
D0 (LSB)	I/O	Data bus bit 0.															
Address bus.																	
A15 or A15/CLK_SEL_1	I/O	<p>For device types 01 through 04 this signal is always configured as address line A15 (MSB).</p> <p>For device types 05 through 08 and 13 through 16, if UPADDREN is connected to logic "1", this signal operates as address line A15 (MSB).</p> <p>For device types 05 through 08 and 13 through 16, if UPADDREN is connected to logic "0", this signal operates as CLK_SEL_1. In this case, A15/CLK_SEL_1 and A14/CLK_SEL_0 are used to select the clock frequency, as follows:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>CLK_SEL_1</th> <th>CLK_SEL_0</th> <th>Clock frequency</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>10 MHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>20 MHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>12 MHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>16 MHz</td> </tr> </tbody> </table>	CLK_SEL_1	CLK_SEL_0	Clock frequency	0	0	10 MHz	0	1	20 MHz	1	0	12 MHz	1	1	16 MHz
CLK_SEL_1	CLK_SEL_0	Clock frequency															
0	0	10 MHz															
0	1	20 MHz															
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TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description															
Address bus - Continued.																	
A14 or A14/CLK_SEL_0	I/O	<p>For device types 01 through 04 this signal is always configured as address line A14.</p> <p>For device types 05 through 08 and 13 through 16, if UPADDREN is connected to logic "1", this signal operates as address line A14.</p> <p>For device types 05 through 08 and 13 through 16, if UPADDREN is connected to logic "0", this signal operates as CLK_SEL_1. In this case, A15/CLK_SEL_1 and A14/CLK_SEL_0 are used to select the clock frequency, as follows:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>CLK_SEL_1</th> <th>CLK_SEL_0</th> <th>Clock frequency</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>10 MHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>20 MHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>12 MHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>16 MHz</td> </tr> </tbody> </table>	CLK_SEL_1	CLK_SEL_0	Clock frequency	0	0	10 MHz	0	1	20 MHz	1	0	12 MHz	1	1	16 MHz
CLK_SEL_1	CLK_SEL_0	Clock frequency															
0	0	10 MHz															
0	1	20 MHz															
1	0	12 MHz															
1	1	16 MHz															
A13 or A13/ +5 V / +3.3 V LOGIC	I/O	<p>For device types 01 through 04 this signal is always configured as address line A13.</p> <p>For device types 05 through 08 and 13 through 16, if UPADDREN is connected to logic "1", this signal operates as address line A13.</p> <p>For device types 05 through 08 and 13 through 16, if UPADDREN is connected to logic "0", then the signal must be connected to +5 V/+3.3 V LOGIC (logic"1").</p>															
A12 or A12 / $\overline{\text{RTBOOT}}$	I/O	<p>For device types 01 through 04 this signal is always configured as address line A12.</p> <p>For device types 05 through 08 and 13 through 16, if UPADDREN is connected to logic "1", this signal operates as address line A12.</p> <p>For device types 05 through 08 and 13 through 16, if UPADDREN is connected to logic "0", then the signal functions as <math>\overline{\text{RTBOOT}}</math>. If <math>\overline{\text{RTBOOT}}</math> is connected to logic "0", the device will initialize in RT mode with the BUSY status word bit set following power turn-on. If <math>\overline{\text{RTBOOT}}</math> is hardwired to logic "1", the device will initialize in either Idle mode (for an RT-only device), or in BC mode (for a BC/RT/MT device).</p>															
A11	I/O	<p>Lower 12 bits of 16-bit bi-directional address bus. In both the buffered and transparent modes, the host processor accesses the device registers and internal RAM by means of A11 through A0 (device types 05 through 08 and 13 through 16). For device types 01 through 04, A15 through A12 are also used for this purpose.</p> <p>In buffered mode, A12 through A0 (or A15 through A0) are inputs only. In the transparent mode, A12 through A0 (or A15 through A0) are inputs during processor accesses and becomes outputs, driving outward (towards the processor) when the 1553 protocol/memory management logic accesses up to 64K words of external RAM.</p> <p>In transparent mode, the address bus is driven outward only when the signal <math>\overline{\text{DTACK}}</math> is low (indicating that the device has control of the RAM interface bus) and <math>\overline{\text{IOEN}}</math> is high, indicating a non-host access. Most of the time, including immediately after power turn-on, A12 through A0 (or A15 through A0) will be in high impedance (input) state</p>															
A10	I/O																
A9	I/O																
A8	I/O																
A7	I/O																
A6	I/O																
A5	I/O																
A4	I/O																
A3	I/O																
A2	I/O																
A1	I/O																
A0 (LSB)	I/O																

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TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
Processor interface control. (device types 01 through 08 and 13 through 16)		
$\overline{\text{SELECT}}$	I	Select. Input from the host processor. When active selects device for operation.
$\overline{\text{STRBD}}$	I	Strobe data. Used in conjunction with $\overline{\text{SELECT}}$ to initiate a data transfer cycle to/from host processor.
$\overline{\text{RD/WR}}$	I	Read/write. Input from the host processor which defines the data bus transfer as a Read or write operation.
$\overline{\text{ADDR\_LAT/MEMOE}}$	I/O	Memory Output Enable or Address Latch. In buffer mode, the ADDR_LAT input is used to configure the buffers for A15 through A0, SELECT, MEM/REG, and MSB/LSB (for 8-bit mode only) in latched mode (when low) or transparent mode (when high). That is the device's internal transparent latches will track the values on A15 through A0, SELESCCT, MEM/REG, and MSB/LSB when ADDR_LAT is high, and latch the values when ADDR_LAT goes low. When interfacing to processors with non-multiplexed address/data bus, ADDR_LAT should be hardwired to logic "1". When interfacing to processors with multiplexed address/data bus, ADDR_LAT should be connected to a signal that indicates a valid address when ADDR_LAT is logic "1". In transparent mode, MEMOE output signal is used to enable data outputs for external RAM read cycles (normally connected to the OE input signal on external RAM chips).
$\overline{\text{MEMWR/ZEROWAIT}}$	O/I	Memory Write or Zero Wait State. In transparent mode, active low output signal asserted low during memory write transfers to strobe data into internal or external RAM (normally connected to the WR signal on external RAM chips). In buffered mode, input signal used to select between the zero wait state mode (ZEROWAIT = logic "0") and the non-zero wait state mode (ZEROWAIT = logic "1").
$\overline{\text{DTREQ/16/8}}$	O/I	Data Transfer Request or 16 Bit/8 Bit Transfer Mode Select. In transparent mode, active low output signal used to request access to the RAM interface bus (address, data, and control buses). In buffered mode, input signal used to select between the 16 bit data transfer mode (16/8 = Logic "1") and the 8 bit data transfer mode (16/8 = Logic "0").
$\overline{\text{DTGRT/MSB/LSB}}$	I	Data Transfer Grant or Most Significant Byte/Least Significant Byte. In 8-bit buffered mode, input signal (MSB/LSB) used to indicate which byte is currently begin transferred (MSB or LSB). The logic sense of MSB/LSB is controlled by the POLARITY_SEL input. MSB/LSB is only used in the 16-bit buffered mode. In transparent mode, active low input signal ( $\overline{\text{DTGRT}}$ ) asserted in response to the DTREQ output to indicate that control of the external processor/RAM bus has been transferred from the host processor to the device type.

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TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
Processor interface control. (device types 01 through 08 and 13 through 16) - Continued.		
$\overline{\text{DTACK/POLARITY\_SEL}}$	O/I	Data Transfer Acknowledge or Polarity Select. In transparent mode, active low output signal used to indicate acceptance of the RAM interface bus in response to a data transfer grant (DTGRT). In 16-bit buffered mode (TRANSPARENT/BUFFERED = logic "0" and 16/8 = logic "1"), input signal used to control the logic sense of the RD/WR signal. If POLARITY_SEL is connected to logic "1", RD/WR should be asserted high (logic "1") for a read operation and low (logic "0") for a write operation. If POLARITY_SEL is connected to logic "0", RD/WR should be asserted low (logic "0") for a read operation and high (logic "1") for a write operation. In 8-bit buffered mode (TRANSPARENT/BUFFERED = logic "0" and 16/8 = logic "0"), input signal used to control the logic sense of the MSB/LSB signal. If POLARITY_SEL is connected to logic "0", MSB/LSB should be asserted low (logic "0") to indicate the transfer of the least significant byte and high (logic "1") to indicate the transfer of the most significant byte. If POLARITY_SEL is connected to logic "1", MSB/LSB should be asserted high (logic "1") to indicate the transfer of the least significant byte and low (logic "0") to indicate the transfer of the most significant byte.
$\overline{\text{MEMENA\_IN/ TRIGGER\_SEL}}$	I	Memory Enable Input or Trigger Select. In transparent mode, active low Chip Select (CS) input to the 4K X 16 of internal shared RAM. If only internal RAM is used connect directly to MEMENA-OUT. In buffered mode, input signal used to indicate the order in which byte pairs are transferred to or from the device by the host processor. This signal has no operation in the 16-bit buffered mode. In the 8-bit buffered mode, TRIGGER_SEL should be asserted high (logic "1") if the byte order for both read operations and write operations is MSB followed LSB. TRIGGER_SEL should be asserted low (logic "0") if the byte order for both read operations and write operations is LSB followed MSB.
$\overline{\text{MEM/REG}}$	I	Memory/register. Input from host processor to select memory or register data transfer.
$\overline{\text{SSFLAG/EXT\_TRIG}}$	I	Sub System Flag or External Trigger Input. In the Remote Terminal mode, if this input is asserted low, the subsystem flag bit will be set in the device's RT Status Word. In the Bus Controller mode if the external BC Start option is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will issue a BC Start command, starting execution of the current BC frame. In the Monitor mode if the external trigger is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will issue a monitor trigger. This input has no effect in RT mode.
$\overline{\text{TRANSPARENT/ BUFFERED}}$	I	Used to select between the transparent and buffered modes for the host processor interface.
$\overline{\text{READYD}}$	O	Ready data. When active indicates data has been received from, or is available to, the CPU.
$\overline{\text{IOEN}}$	O	Input/output enable. Output to enable external buffers/latches connecting the hybrid to the address/data bus.

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TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
Miscellaneous. (device types 01 through 08 and 13 through 16)		
UPADDREN	-	For device types 01 through 04, this pin is connected to +5 V. For device types 05 through 08, this signal is used to control the function of A15 through A12. If UPADDREN is connected to logic "1", these four signals operate as address lines A15 through A12. If UPADDREN is connected to logic "0", A15 and A14 function as CLK_SEL_1 and CLK_SEL_0 respectively. A13 must be connected to V <sub>CC</sub> -LOGIC (+5 V or +3.3 V) and A12 functions as RTBOOT.
CLOCK IN	I	20 MHz, 16 MHz, 12 MHz, or 10 MHz TTL clock input.
$\overline{\text{INCMD/MCRST}}$	O	In-command or Mode Code Reset. Indicates BC to RTU currently in message transfer sequence or resets RT mode command.
$\overline{\text{MSTRCLR}}$	I	Master clear. Power-on reset from host processor.
$\overline{\text{INT}}$	O	Interrupt Request output. Interrupt pulse line to host processor.
TX_INH_A, TX_INH_B	I	Transmitter inhibit inputs for channel A and channel B MIL-STD-1553 transmitters. Normally, these inputs should be connected to logic "0". To force shutdown of channel A and/or channel B, a value of logic "1" should be applied to the respective TX_INH input.
Command / Address Bus. (device types 09 through 12)		
L_BRO	O	Latched Broadcast. A two-staged output signal is latched following receipt of a new command word. For a broadcast command, the signal will output a value of logic "1". For a non-broadcast command, the signal will output a value of logic "0".
T/R	-	Transmit/Receive. A two-state output signal is latched following receipt of a new command word. For a transmit message, the signal will output a logic "1". For a receive message, the signal will output a value of logic "0".
SA4 SA3 SA2 SA1 SA0	O O O O O	Sub-address. These five two-stage output signals are latched following receipt of a new command word. They provide the sub-address field of the received command word.
WC / MC / CWC4 (MSB) WC / MC / CWC3 WC / MC / CWC2 WC / MC / CWC1 WC / MC / CWC0 (LSB)	O O O O O	Word Count/Mode code/Current Word Count. Following receipt of a new command word, these five two-state output signals provide the contents of the command word's Word Count/Mode Code field. For non-mode code receive message, the contents of WC/CWC are updated and incremented to reflect the value of the current data word being transferred to the system (in non-burst mode) or to the internal FIFO (in burst mode). CWC increments from 0 to the value of the Word Count field - 1 during the message. At the end of a non-mode code receive message in burst mode, the contents of CWC will then increment from 0 to the value of the word count field - 1, as each word is transferred from the internal FIFO to the external system over D15 through D0. In burst mode, it takes three clock cycles to transfer each word to the external system. For a non-mode code transmit command, the value of CWC starts from 0 and increments to the value of Word Count - 1, as each word is read from the external system and transferred to the device. For a mode code command, the WC/CWC outputs the command word mode code field, which remains latched through the end of the message (until receipt of a subsequent command word).

**STANDARD  
MICROCIRCUIT DRAWING**

DEFENSE SUPPLY CENTER COLUMBUS  
COLUMBUS, OHIO 43216-5000

SIZE  
**A**

**5962-01514**

REVISION LEVEL  
**A**

SHEET  
**22**

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
DMA Handshake and Transfer Control Signals. (device types 09 through 12)		
$\overline{\text{DTREQ}}$	O	Data Transfer Request. Active low level output signal used to request use of the external system data bus (D15 through D0).
$\overline{\text{DTGRT}}$	I	Data Transfer Grant. Input from the <u>external</u> subsystem that must be asserted low in response to the device asserting $\overline{\text{DTREQ}}$ low in order to enable the device to read data from or write data to the <u>external</u> subsystem. The maximum allowable time from $\overline{\text{DTREQ}}$ to $\overline{\text{DTGRT}}$ is 10 $\mu\text{s}$ . If the device's DMA handshake isn't required, $\overline{\text{DTGRT}}$ may be hardwired to logic "0".
$\overline{\text{DTACK}}$	O	Data Transfer Acknowledge. Active low output signal used to indicate the device's acceptance of the system data bus (D15 through D0), in response to a data transfer grant ( $\overline{\text{DTGRT}}$ ). The device's data transfers over D15 through D0 will be framed by the time that $\overline{\text{DTACK}}$ is asserted low. If <u>AUTO_CFG</u> is strapped to logic "0", there will be a $\overline{\text{DTREQ}}/\overline{\text{DTGRT}}$ handshake cycle after the rising edge of <u>MSTCLR</u> , following power turn-on. After $\overline{\text{DTGRT}}$ is sampled low, $\overline{\text{DTACK}}$ and <u>RTACTIVE</u> will then be asserted low to enable configuration data to be read from an external tri-state buffer. For transmit messages, or a receive messages in non-burst mode, or for receive messages to subaddress 30 assuming the Subaddress 30 Autowrap is disabled, $\overline{\text{DTACK}}$ will be asserted low to indicate the transfer of individual words between the external system and the device. For receive messages in burst mode assuming a valid received message, $\overline{\text{DTACK}}$ will be asserted low after the $\overline{\text{DTREQ}}$ -to- $\overline{\text{DTGRT}}$ handshake following the receipt of the last received data word. It will remain low for the duration of the DMA burst write transfer from the device to the external system. The total time for a burst write transfer is three clock cycles times the number of data words.
$\overline{\text{HS-FAIL}}$	O	Handshake Fail. If this signal is asserted low, this indicates a handshake timeout condition. That is, the system did not respond with a $\overline{\text{DTGRT}}$ in time, following the device's assertion of $\overline{\text{DTREQ}}$ .
$\overline{\text{MEMOE}}$	O	Memory Output Enable. A two-state output signal is used to enable data inputs from the external system to be enabled on to D15 through D0. $\overline{\text{MEMOE}}$ pulses low for three clock cycles for each data word read from the external system. The device latches the data one clock cycle prior to the rising edge of $\overline{\text{MEMOE}}$ .
$\overline{\text{MEMWR}}$	O	Memory Write. Active low two-state output signal (one clock cycle wide) asserted low during device write cycles. Used to transfer data from the device to the external system. The external system may latch data on either the falling or rising edge of $\overline{\text{MEMWR}}$ .

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TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
RT status word inputs. (device types 09 through 12)		
$\overline{\text{ILLEGAL}}$	I	Illegal. Input to the device that is sampled after the Command Word transfer. A logic "0" will cause the Message Error bit in the status response to be set (logic "1"), while a logic "1" on this input will have no effect on the Message Error bit.
$\overline{\text{SRV\_RQST}}$	I	Service Request. When this input is logic "0", the Service Request bit in the device's status word will be logic "1". When this input is logic "1", the Service Request bit in the device's status word will be logic "0".
$\overline{\text{SSFLAG}}$	I	Subsystem Flag. If this input is asserted low, the Subsystem Flag bit will be set in the device's status word.
$\overline{\text{BUSY}}$	I	Busy. If this input is asserted low, the Busy bit will be set to logic "1" in the device's status word. If the Busy bit in the status word is logic "1", the device will not transmit any data words, except for a Transmit last command or Transmit BIT word node command. For a receive command, if the device is Busy, it will transfer data words to the external system (although these transfers may be blocked by means of external logic).
RT activity and message status indicators. (device types 09 through 12)		
RTACTIVE	---	RT Active. This signal will be low (logic "0") following power turn-on, and when the device is reading its Auto-configure word or is performing its internal self-test. After the self-test passes, or if the Auto-configure option is not used, or if Auto-configure is used but bit 5 of the Auto-configure word is logic "1" (meaning for the RT to always go online), RTACTIVE will then transition to logic "1". When this occurs, the device will begin processing messages over the 1553 bus. If Auto-configure is enabled, and bit 5 of the Auto-configure word is logic "0" and self-test fails, then RTACTIVE will remain logic "0". In this case, the device will remain offline and not process any 1553 messages. A failed self-test will cause RTFAIL_L to be asserted low (logic "0"). If the Auto-configure option is used, the external system should enable the configuration bits on D5 through D0, when RTACTIVE and DTACK are both outputting logic "0".
$\overline{\text{INCMD}}$	---	In-command. This two-state output is asserted low whenever a message is being processed by the device.
$\overline{\text{GBR}}$	O	Good Block Received. Low level two-state output pulse (2 clock cycles wide) that is used to indicate to the external system that a valid, legal, non-mode receive command with the correct number of valid data words has been received and transferred to the external system. For non-burst mode, this pulse will occur after the last data word is transferred. Assuming a DTREQ-to-DTGR time of 0, this will be approximately 4 microseconds following the mid-parity bit crossing of the last received data word. For burst mode, the GBR pulse will begin synchronous with the rising edge of DTACK at the end of the burst write transfer.
$\overline{\text{MSE\_ERR}}$	O	Message Error. Active low level two-state output signal used to flag to the external system that there was a message error on the 1553 bus communication (word, gap, or word count error) for a particular message. This output goes low upon detecting the error and is reset following the receipt of the next valid command word (to the RT) from the 1553 bus, or if MSTCLR is asserted low. If this output goes low, all further servicing of the current message is aborted.

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TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
RT activity and message status indicators - Continued. (device types 09 through 12)		
$\overline{\text{RTFAIL}}$	O	<p>Remote Terminal Fail. This two-state output signal will be asserted low following a failure of the built-in self-test performed following power turn-on or as the result of the receipt of an initiate self-test mode command. The built-in off-line self-test includes tests of the Manchester encoder and decoders, transmitter failsafe timer, and RT protocol logic.</p> <p>In addition RTFAIL will be asserted low following a failure of the on-line loop test for any non-broadcast message. The on-line loop test verifies the validity of the received version of all transmitted words (sync, Manchester encoding, bit count, parity), and includes a bit-by-bit comparison and verification of the last transmitted word.</p> <p>If asserted to logic "0", <math>\overline{\text{RTFAIL}}</math> will clear to logic "1" when the device begins transmission of its status word in response to a subsequent valid non-broadcast message.</p>
Command inputs. (device types 09 through 12)		
$\overline{\text{MSTCLR}}$	I	<p>Master Clear. Negative true reset input, asserted low following power turn-on. When coming out of "reset" condition, note that the rise time of <math>\overline{\text{MSTCLR}}</math> must be less than 10 microseconds.</p>
$\overline{\text{AUTO\_CFG}}$	I	<p>Auto-configure. If connected to logic "1", then the auto-configure option is disabled, and the six configuration parameters revert to their default values. Note that the default condition for each configuration parameter is enabled (for MIL-STD-1553A/B protocol selection, -1553B is the default).</p> <p>If <math>\overline{\text{AUTO\_CFG}}</math> is connected to logic "0", then the configuration parameters are transferred over D5 through D0 during a DMA read data transfer, when <math>\overline{\text{RTACTIVE}}</math> and <math>\overline{\text{DTACK}}</math> are logic "0", following <math>\overline{\text{MSTCLR}}</math> transitioning from logic "0" to logic "1". Each of the configuration parameters is enabled if the device reads a value logic "1" for the respective data bit.</p>
$\text{BRO\_ENA}$	I	<p>Broadcast enable. If this input is logic "1", the device will recognize RT address 31 as the broadcast address. If this input is logic "0", the device will not recognize RT address 31 as the broadcast address; however, in this configuration, RT address 31 may be used as a standard RT address.</p>
$\text{TX\_INH}$	I	<p>Transmitter Inhibit input for the MIL-STD-1553 transmitters. For normal operation, this input should be connected to logic "0". To force a shutdown of the Channel A and Channel B transmitters, a value of logic "1" should be applied to this input.</p>

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-10-02

Approved sources of supply for SMD 5962-01514 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE Number	Vendor similar PIN <u>2</u> /
5962-0151401HMA 5962-0151401HMA 5962-0151401HMA 5962-0151401HMA	S7631 S7631 19645 19645	BU-61865G3-150 BU-61865G3-140 BU-61865G3-150 BU-61865G3-140
5962-0151401HMC 5962-0151401HMC 5962-0151401HMC 5962-0151401HMC	S7631 S7631 19645 19645	BU-61865G3-130 BU-61865G3-110 BU-61865G3-130 BU-61865G3-110
5962-0151401HTA 5962-0151401HTA 5962-0151401HTA 5962-0151401HTA	S7631 S7631 19645 19645	BU-61865F3-150 BU-61865F3-140 BU-61865F3-150 BU-61865F3-140
5962-0151401HTC 5962-0151401HTC 5962-0151401HTC 5962-0151401HTC	S7631 S7631 19645 19645	BU-61865F3-130 BU-61865F3-110 BU-61865F3-130 BU-61865F3-110
5962-0151402HMA 5962-0151402HMA 5962-0151402HMA 5962-0151402HMA	S7631 S7631 19645 19645	BU-61865G4-150 BU-61865G4-140 BU-61865G4-150 BU-61865G4-140
5962-0151402HMC 5962-0151402HMC 5962-0151402HMC 5962-0151402HMC	S7631 S7631 19645 19645	BU-61865G4-130 BU-61865G4-110 BU-61865G4-130 BU-61865G4-110
5962-0151402HTA 5962-0151402HTA 5962-0151402HTA 5962-0151402HTA	S7631 S7631 19645 19645	BU-61865F4-150 BU-61865F4-140 BU-61865F4-150 BU-61865F4-140
5962-0151402HTC 5962-0151402HTC 5962-0151402HTC 5962-0151402HTC	S7631 S7631 19645 19645	BU-61865F4-130 BU-61865F4-110 BU-61865F4-130 BU-61865F4-110

See footnotes at end of table.

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5962-0151403HMA 5962-0151403HMA 5962-0151403HMA 5962-0151403HMA	S7631 S7631 19645 19645	BU-61864G3-150 BU-61864G3-140 BU-61864G3-150 BU-61864G3-140
5962-0151403HMC 5962-0151403HMC 5962-0151403HMC 5962-0151403HMC	S7631 S7631 19645 19645	BU-61864G3-130 BU-61864G3-110 BU-61864G3-130 BU-61864G3-110
5962-0151403HTA 5962-0151403HTA 5962-0151403HTA 5962-0151403HTA	S7631 S7631 19645 19645	BU-61864F3-150 BU-61864F3-140 BU-61864F3-150 BU-61864F3-140
5962-0151403HTC 5962-0151403HTC 5962-0151403HTC 5962-0151403HTC	S7631 S7631 19645 19645	BU-61864F3-130 BU-61864F3-110 BU-61864F3-130 BU-61864F3-110
5962-0151404HMA 5962-0151404HMA 5962-0151404HMA 5962-0151404HMA	S7631 S7631 19645 19645	BU-61864G4-150 BU-61864G4-140 BU-61864G4-150 BU-61864G4-140
5962-0151404HMC 5962-0151404HMC 5962-0151404HMC 5962-0151404HMC	S7631 S7631 19645 19645	BU-61864G4-130 BU-61864G4-110 BU-61864G4-130 BU-61864G4-110
5962-0151404HTA 5962-0151404HTA 5962-0151404HTA 5962-0151404HTA	S7631 S7631 19645 19645	BU-61864F4-150 BU-61864F4-140 BU-61864F4-150 BU-61864F4-140
5962-0151404HTC 5962-0151404HTC 5962-0151404HTC 5962-0151404HTC	S7631 S7631 19645 19645	BU-61864F4-130 BU-61864F4-110 BU-61864F4-130 BU-61864F4-110
5962-0151405HMA 5962-0151405HMA 5962-0151405HMA 5962-0151405HMA	S7631 S7631 19645 19645	BU-61745G3-150 BU-61745G3-140 BU-61745G3-150 BU-61745G3-140
5962-0151405HMC 5962-0151405HMC 5962-0151405HMC 5962-0151405HMC	S7631 S7631 19645 19645	BU-61745G3-130 BU-61745G3-110 BU-61745G3-130 BU-61745G3-110
5962-0151405HTA 5962-0151405HTA 5962-0151405HTA 5962-0151405HTA	S7631 S7631 19645 19645	BU-61745F3-150 BU-61745F3-140 BU-61745F3-150 BU-61745F3-140
5962-0151405HTC 5962-0151405HTC 5962-0151405HTC 5962-0151405HTC	S7631 S7631 19645 19645	BU-61745F3-130 BU-61745F3-110 BU-61745F3-130 BU-61745F3-110

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5962-0151406HMA 5962-0151406HMA 5962-0151406HMA 5962-0151406HMA	S7631 S7631 19645 19645	BU-61745G4-150 BU-61745G4-140 BU-61745G4-150 BU-61745G4-140
5962-0151406HMC 5962-0151406HMC 5962-0151406HMC 5962-0151406HMC	S7631 S7631 19645 19645	BU-61745G4-130 BU-61745G4-110 BU-61745G4-130 BU-61745G4-110
5962-0151406HTA 5962-0151406HTA 5962-0151406HTA 5962-0151406HTA	S7631 S7631 19645 19645	BU-61745F4-150 BU-61745F4-140 BU-61745F4-150 BU-61745F4-140
5962-0151406HTC 5962-0151406HTC 5962-0151406HTC 5962-0151406HTC	S7631 S7631 19645 19645	BU-61745F4-130 BU-61745F4-110 BU-61745F4-130 BU-61745F4-110
5962-0151407HMA 5962-0151407HMA 5962-0151407HMA 5962-0151407HMA	S7631 S7631 19645 19645	BU-61743G3-150 BU-61743G3-140 BU-61743G3-150 BU-61743G3-140
5962-0151407HMC 5962-0151407HMC 5962-0151407HMC 5962-0151407HMC	S7631 S7631 19645 19645	BU-61743G3-130 BU-61743G3-110 BU-61743G3-130 BU-61743G3-110
5962-0151407HTA 5962-0151407HTA 5962-0151407HTA 5962-0151407HTA	S7631 S7631 19645 19645	BU-61743F3-150 BU-61743F3-140 BU-61743F3-150 BU-61743F3-140
5962-0151407HTC 5962-0151407HTC 5962-0151407HTC 5962-0151407HTC	S7631 S7631 19645 19645	BU-61743F3-130 BU-61743F3-110 BU-61743F3-130 BU-61743F3-110
5962-0151408HMA 5962-0151408HMA 5962-0151408HMA 5962-0151408HMA	S7631 S7631 19645 19645	BU-61743G4-150 BU-61743G4-140 BU-61743G4-150 BU-61743G4-140
5962-0151408HMC 5962-0151408HMC 5962-0151408HMC 5962-0151408HMC	S7631 S7631 19645 19645	BU-61743G4-130 BU-61743G4-110 BU-61743G4-130 BU-61743G4-110
5962-0151408HTA 5962-0151408HTA 5962-0151408HTA 5962-0151408HTA	S7631 S7631 19645 19645	BU-61743F4-150 BU-61743F4-140 BU-61743F4-150 BU-61743F4-140
5962-0151408HTC 5962-0151408HTC 5962-0151408HTC 5962-0151408HTC	S7631 S7631 19645 19645	BU-61743F4-130 BU-61743F4-110 BU-61743F4-130 BU-61743F4-110

See footnotes at end of table.

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5962-0151409HMA 5962-0151409HMA 5962-0151409HMA 5962-0151409HMA	S7631 S7631 19645 19645	BU-61705G3-150 BU-61705G3-140 BU-61705G3-150 BU-61705G3-140
5962-0151409HMC 5962-0151409HMC 5962-0151409HMC 5962-0151409HMC	S7631 S7631 19645 19645	BU-61705G3-130 BU-61705G3-110 BU-61705G3-130 BU-61705G3-110
5962-0151409HTA 5962-0151409HTA 5962-0151409HTA 5962-0151409HTA	S7631 S7631 19645 19645	BU-61705F3-150 BU-61705F3-140 BU-61705F3-150 BU-61705F3-140
5962-0151409HTC 5962-0151409HTC 5962-0151409HTC 5962-0151409HTC	S7631 S7631 19645 19645	BU-61705F3-130 BU-61705F3-110 BU-61705F3-130 BU-61705F3-110
5962-0151410HMA 5962-0151410HMA 5962-0151410HMA 5962-0151410HMA	S7631 S7631 19645 19645	BU-61705G4-150 BU-61705G4-140 BU-61705G4-150 BU-61705G4-140
5962-0151410HMC 5962-0151410HMC 5962-0151410HMC 5962-0151410HMC	S7631 S7631 19645 19645	BU-61705G4-130 BU-61705G4-110 BU-61705G4-130 BU-61705G4-110
5962-0151410HTA 5962-0151410HTA 5962-0151410HTA 5962-0151410HTA	S7631 S7631 19645 19645	BU-61705F4-150 BU-61705F4-140 BU-61705F4-150 BU-61705F4-140
5962-0151410HTC 5962-0151410HTC 5962-0151410HTC 5962-0151410HTC	S7631 S7631 19645 19645	BU-61705F4-130 BU-61705F4-110 BU-61705F4-130 BU-61705F4-110
5962-0151411HMA 5962-0151411HMA 5962-0151411HMA 5962-0151411HMA	S7631 S7631 19645 19645	BU-61703G3-150 BU-61703G3-140 BU-61703G3-150 BU-61703G3-140
5962-0151411HMC 5962-0151411HMC 5962-0151411HMC 5962-0151411HMC	S7631 S7631 19645 19645	BU-61703G3-130 BU-61703G3-110 BU-61703G3-130 BU-61703G3-110
5962-0151411HTA 5962-0151411HTA 5962-0151411HTA 5962-0151411HTA	S7631 S7631 19645 19645	BU-61703F3-150 BU-61703F3-140 BU-61703F3-150 BU-61703F3-140
5962-0151411HTC 5962-0151411HTC 5962-0151411HTC 5962-0151411HTC	S7631 S7631 19645 19645	BU-61703F3-130 BU-61703F3-110 BU-61703F3-130 BU-61703F3-110

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5962-0151412HMA 5962-0151412HMA 5962-0151412HMA 5962-0151412HMA	S7631 S7631 19645 19645	BU-61703G4-150 BU-61703G4-140 BU-61703G4-150 BU-61703G4-140
5962-0151412HMC 5962-0151412HMC 5962-0151412HMC 5962-0151412HMC	S7631 S7631 19645 19645	BU-61703G4-130 BU-61703G4-110 BU-61703G4-130 BU-61703G4-110
5962-0151412HTA 5962-0151412HTA 5962-0151412HTA 5962-0151412HTA	S7631 S7631 19645 19645	BU-61703F4-150 BU-61703F4-140 BU-61703F4-150 BU-61703F4-140
5962-0151412HTC 5962-0151412HTC 5962-0151412HTC 5962-0151412HTC	S7631 S7631 19645 19645	BU-61703F4-130 BU-61703F4-110 BU-61703F4-130 BU-61703F4-110
5962-0151413HMA 5962-0151413HMA 5962-0151413HMA 5962-0151413HMA	S7631 S7631 19645 19645	BU-61845G3-150 BU-61845G3-140 BU-61845G3-150 BU-61845G3-140
5962-0151413HMC 5962-0151413HMC 5962-0151413HMC 5962-0151413HMC	S7631 S7631 19645 19645	BU-61845G3-130 BU-61845G3-110 BU-61845G3-130 BU-61845G3-110
5962-0151413HTA 5962-0151413HTA 5962-0151413HTA 5962-0151413HTA	S7631 S7631 19645 19645	BU-61845F3-150 BU-61845F3-140 BU-61845F3-150 BU-61845F3-140
5962-0151413HTC 5962-0151413HTC 5962-0151413HTC 5962-0151413HTC	S7631 S7631 19645 19645	BU-61845F3-130 BU-61845F3-110 BU-61845F3-130 BU-61845F3-110
5962-0151414HMA 5962-0151414HMA 5962-0151414HMA 5962-0151414HMA	S7631 S7631 19645 19645	BU-61845G4-150 BU-61845G4-140 BU-61845G4-150 BU-61845G4-140
5962-0151414HMC 5962-0151414HMC 5962-0151414HMC 5962-0151414HMC	S7631 S7631 19645 19645	BU-61845G4-130 BU-61845G4-110 BU-61845G4-130 BU-61845G4-110
5962-0151414HTA 5962-0151414HTA 5962-0151414HTA 5962-0151414HTA	S7631 S7631 19645 19645	BU-61845F4-150 BU-61845F4-140 BU-61845F4-150 BU-61845F4-140
5962-0151414HTC 5962-0151414HTC 5962-0151414HTC 5962-0151414HTC	S7631 S7631 19645 19645	BU-61845F4-130 BU-61845F4-110 BU-61845F4-130 BU-61845F4-110

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING BULLETIN - Continued.

DATE: 01-10-02

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-0151415HMA 5962-0151415HMA 5962-0151415HMA 5962-0151415HMA	S7631 S7631 19645 19645	BU-61843G3-150 BU-61843G3-140 BU-61843G3-150 BU-61843G3-140
5962-0151415HMC 5962-0151415HMC 5962-0151415HMC 5962-0151415HMC	S7631 S7631 19645 19645	BU-61843G3-130 BU-61843G3-110 BU-61843G3-130 BU-61843G3-110
5962-0151415HTA 5962-0151415HTA 5962-0151415HTA 5962-0151415HTA	S7631 S7631 19645 19645	BU-61843F3-150 BU-61843F3-140 BU-61843F3-150 BU-61843F3-140
5962-0151415HTC 5962-0151415HTC 5962-0151415HTC 5962-0151415HTC	S7631 S7631 19645 19645	BU-61843F3-130 BU-61843F3-110 BU-61843F3-130 BU-61843F3-110
5962-0151416HMA 5962-0151416HMA 5962-0151416HMA 5962-0151416HMA	S7631 S7631 19645 19645	BU-61843G4-150 BU-61843G4-140 BU-61843G4-150 BU-61843G4-140
5962-0151416HMC 5962-0151416HMC 5962-0151416HMC 5962-0151416HMC	S7631 S7631 19645 19645	BU-61843G4-130 BU-61843G4-110 BU-61843G4-130 BU-61843G4-110
5962-0151416HTA 5962-0151416HTA 5962-0151416HTA 5962-0151416HTA	S7631 S7631 19645 19645	BU-61843F4-150 BU-61843F4-140 BU-61843F4-150 BU-61843F4-140
5962-0151416HTC 5962-0151416HTC 5962-0151416HTC 5962-0151416HTC	S7631 S7631 19645 19645	BU-61843F4-130 BU-61843F4-110 BU-61843F4-130 BU-61843F4-110

1/ The lead finish shown for each PIN, representing a hermetic package, is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number

Vendor name  
and address

S7631

DDC Ireland, LTD.  
Cork Business & Technology Park  
Model Farm Road  
Cork, Ireland

19645

Data Device Corporation  
105 Wilbur Place  
Bohemia, NY 11716-2482

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