

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R010-91.	91-09-25	Monica L. Poelking
B	Update boilerplate to MIL-PRF-38535 requirements. - CFS	03-08-11	Charles F. Saffle

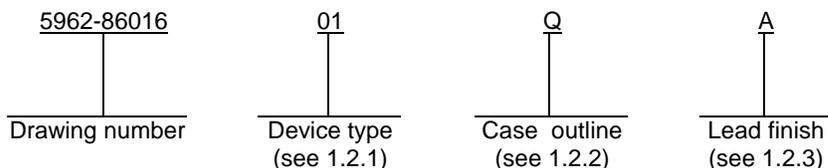
THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B	B	B							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27							
REV STATUS OF SHEETS	REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			
PMIC N/A	PREPARED BY Christopher A. Rauch				<b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 <a href="http://www.dscc.dla.mil">http://www.dscc.dla.mil</a></b>  <b>MICROCIRCUIT, DIGITAL, CMOS, 8-BIT MICROPROCESSOR CPU, MONOLITHIC SILICON</b>															
<b>STANDARD MICROCIRCUIT DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A	CHECKED BY Tim H. Noh																			
	APPROVED BY William K. Heckman																			
	DRAWING APPROVAL DATE 90-12-07																			
	REVISION LEVEL B																			
	SIZE A	CAGE CODE <b>67268</b>	<b>5962-86016</b>																	
	SHEET 1 OF 27																			

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	80C88	8-Bit microprocessor CPU

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line
X	CQCC1-N44	44	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range ( $V_{CC}$ ) (Referenced to ground).....	+8.0 V dc maximum
Input, output, or I/O applied voltage range .....	GND - 0.5 V dc to $V_{CC} + 0.5$ V dc
Storage temperature range.....	-65°C to +150°C
Maximum power dissipation ( $P_D$ ): <u>1/</u>	
Case Q.....	1820 mW
Case X.....	806 mW
Lead temperature (soldering, 10 seconds).....	+300°C
Maximum junction temperature ( $T_J$ ).....	+175°C
Thermal resistance, junction-to-case ( $\theta_{JC}$ ).....	See MIL-STD-1835
Thermal resistance, junction-to-ambient ( $\theta_{JA}$ ):	
Case Q.....	27.5°C/W
Case X.....	62.2°C/W

1.4 Recommended operating conditions.

Supply voltage range ( $V_{CC}$ ).....	+4.5 V dc to +5.5 V dc
Case operating temperature range ( $T_C$ ).....	-55°C to +125°C

1/ Must withstand the added  $P_D$  due to short circuit test e.g.,  $I_{OS}$ .

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE <b>A</b>	<b>5962-86016</b>
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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Switching waveforms and test circuits. The switching waveforms and test circuits shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

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3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 and QML38535 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input voltage	V <sub>IH</sub> <u>1/</u>	V <sub>CC</sub> = 5.5 V	1, 2, 3	All	2.2		V
Low level input voltage	V <sub>IL</sub> <u>1/</u>	V <sub>CC</sub> = 4.5 V	1, 2, 3	All		0.8	V
High level output voltage	V <sub>OH</sub> <u>2/</u>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -2.5 mA	1, 2, 3	All	3.0		V
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -100 μA			4.1		
Low level output voltage	V <sub>OL</sub> <u>2/</u>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = +2.5 mA	1, 2, 3	All		0.4	V
Operating power supply current	I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, f = 5.0 MHz V <sub>IN</sub> = 0 V or 5.5 V Outputs open	1, 2, 3	All		50	mA
Standby power supply current	I <sub>SB</sub> <u>3/</u>	V <sub>CC</sub> = 5.5 V V <sub>IN</sub> = 0 V or 5.5 V Outputs unloaded	1, 2, 3	All		500	μA
Input leakage current	I <sub>LI</sub> <u>4/</u>	V <sub>CC</sub> = 5.5 V V <sub>IN</sub> = 0 V or 5.5 V	1, 2, 3	All	-1.0	+1.0	μA
Output leakage current	I <sub>LO</sub> <u>5/</u>	V <sub>CC</sub> = 5.5 V V <sub>OUT</sub> = 0 V	1, 2, 3	All		-10	μA
Clock input high voltage	V <sub>CH</sub>	V <sub>CC</sub> = 5.5 V	1, 2, 3	All	4.7		V
Clock input low voltage	V <sub>CL</sub>	V <sub>CC</sub> = 4.5 V	1, 2, 3	All		0.8	V
Input current, bus hold high	I <sub>BHH</sub> <u>6/</u>	V <sub>IN</sub> = 3.0 V V <sub>CC</sub> = 4.5 V and 5.5 V	1, 2, 3	All	-40	-400	μA
Input current, bus hold low	I <sub>BHL</sub> <u>7/</u>	V <sub>IN</sub> = 0.8 V V <sub>CC</sub> = 4.5 V and 5.5 V	1, 2, 3	All	40	400	μA
Input capacitance	C <sub>IN</sub>	V <sub>CC</sub> = 4.5 V to 5.5 V All measurements are referenced to GND. See 4.3.1c	4	All		25	pF
Output capacitance	C <sub>OUT</sub>		4	All		25	pF
I/O capacitance	C <sub>I/O</sub>		4	All		25	pF
Functional tests		See 4.3.1d	7, 8	All			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock cycle period	t <sub>CLCL</sub>	C <sub>L</sub> = 100 pF, V <sub>CC</sub> = 4.5 V, f = 1.0 MHz, See figure 3 <u>8/</u>	9, 10, 11	All	200		ns
Clock low time	t <sub>CLCH</sub>		9, 10, 11	All	118		ns
Clock high time	t <sub>CHCL</sub>		9, 10, 11	All	69		ns
Data in setup time	t <sub>DVCL</sub>		9, 10, 11	All	30		ns
Data in hold time	t <sub>CLDX1</sub>		9, 10, 11	All	10		ns
READY setup time into device	t <sub>RYHCH</sub>		9, 10, 11	All	118		ns
READY hold time into device	t <sub>CHRYX</sub>		9, 10, 11	All	30		ns
READY to inactive CLK	t <sub>RYLCL</sub> <u>9/</u>		9, 10, 11	All	-8.0		ns
HOLD setup time	t <sub>HVCH</sub> <u>10/</u>		9, 10, 11	All	35		ns
INTR, NMI, TEST setup time	t <sub>INVCH</sub> <u>11/</u>		9, 10, 11	All	30		ns
RQ/GT setup time	t <sub>GVCH</sub> <u>12/</u>		9, 10, 11	All	30		ns
RQ hold time into device 01	t <sub>CHGX</sub> <u>12/ 13/</u>		9, 10, 11	All	40	t <sub>CHCL</sub> +10	ns
Hold/hold acknowledge time	t <sub>CHSZ</sub> <u>14/</u>		9, 10, 11	All		80	ns
READY active to status passive	t <sub>RYHSH</sub> <u>9/ 12/ 15/</u>		9, 10, 11	All		110	ns
Status active delay	t <sub>CHSV</sub> <u>12/</u>		9, 10, 11	All	10	110	ns
Status inactive delay	t <sub>CLSH</sub> <u>12/ 15/</u>		9, 10, 11	All	10	130	ns
Address valid delay	t <sub>CLAV</sub>	9, 10, 11	All	10	110	ns	
Address hold time	t <sub>CLAX</sub>	9, 10, 11	All	10		ns	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address float delay	t <sub>CLAZ</sub> <u>14/</u>	C <sub>L</sub> = 100 pF, V <sub>CC</sub> = 4.5 V, f = 1.0 MHz, See figure 3 <u>8/</u>	9, 10, 11	All	t <sub>CLAX</sub>	80	ns
ALE width	t <sub>LHLL</sub> <u>10/</u>		9, 10, 11	All	t <sub>CLCH-20</sub>		ns
ALE active delay	t <sub>CLLH</sub> <u>10/</u>		9, 10, 11	All		80	ns
ALE inactive delay	t <sub>CHLL</sub> <u>10/</u>		9, 10, 11	All		85	ns
Address hold time to ALE inactive	t <sub>LLAX</sub> <u>10/</u>		9, 10, 11	All	t <sub>CHCL-10</sub>		ns
Data valid delay	t <sub>CLDV</sub>		9, 10, 11	All	10	110	ns
Data hold time	t <sub>CLDX2</sub> <u>14/</u>		9, 10, 11	All	10		ns
Data hold time after WR	t <sub>WHDX</sub> <u>14/</u>		9, 10, 11	All	t <sub>CLCL-30</sub>		ns
Control active delay 1	t <sub>CVCTV</sub> <u>10/</u>		9, 10, 11	All	10	110	ns
Control active delay 2	t <sub>CHCTV</sub> <u>10/</u>		9, 10, 11	All	10	110	ns
Control inactive delay	t <sub>CVCTX</sub> <u>10/</u>		9, 10, 11	All	10	110	ns
Address float to RD active	t <sub>AZRL</sub> <u>10/ 14/</u>		9, 10, 11	All	0		ns
RD active delay	t <sub>CLRL</sub>		9, 10, 11	All	10	165	ns
RD inactive delay	t <sub>CLRH</sub>		9, 10, 11	All	10	150	ns
RD inactive to next address active	t <sub>RHAV</sub>		9, 10, 11	All	t <sub>CLCL-45</sub>		ns
HLDA valid delay	t <sub>CLHAV</sub> <u>10/</u>		9, 10, 11	All	10	160	ns
GT active delay	t <sub>CLGL</sub> <u>12/</u>		9, 10, 11	All	0	85	ns
GT inactive delay	t <sub>CLGH</sub> <u>12/</u>		9, 10, 11	All	0	85	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
WR width	t <sub>WLWH</sub> 10/	C <sub>L</sub> = 100 pF, V <sub>CC</sub> = 4.5 V, f = 1.0 MHz, See figure 3 8/	9, 10, 11	All	2t <sub>CLCL</sub> -60		ns
Address valid to ALE low	t <sub>AVAL</sub> 10/		9, 10, 11	All	t <sub>CLCH</sub> -60		ns
RD width	t <sub>RLRH</sub>		9, 10, 11	All	2t <sub>CLCL</sub> -75		ns
Output rise time	t <sub>OLOH</sub> 14/	From 0.8 V to 2.0 V See figure 3	9, 10, 11	All		15	ns
Output fall time	t <sub>OHOL</sub> 14/	From 2.0 V to 0.8 V See figure 3	9, 10, 11	All		15	ns

- 1/ MN/MX is a strap option and should be held to V<sub>CC</sub> or GND.
- 2/ Interchanging of force and sense conditions is permitted.
- 3/ Measured during clock high time after HALT instruction execution.
- 4/ Applies to NMI, INTR, CLK, RESET, READY, TEST, and MN/MX inputs only.
- 5/ I<sub>LO</sub> should be measured by putting the pin in a high impedance state and then driving V<sub>OUT</sub> to GND. Applies to DEN, DT/R, IO/M, WR, and RD outputs only.
- 6/ I<sub>BHH</sub> should be measured after raising V<sub>IN</sub> to V<sub>CC</sub> and then lowering to valid input high level of 3.0 V on the following inputs: AD0 thru AD7, A8 thru A15, A16/S3 thru A19/S6, DEN, DT/R, IO/M, WR, HLDA, HOLD, RD, and SSO.
- 7/ I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising to valid input low level of 0.8 V on the following inputs: AD0 thru AD7, A8 thru A15, and A16/S3 thru A19/S6.
- 8/ AC tests apply for both minimum and maximum mode system timing unless otherwise specified.
- 9/ Applies only to T2 state (8.0 ns into T3).
- 10/ Applies to minimum mode timing only.
- 11/ Setup requirement for asynchronous signal only to guaranteed recognition at next clock.
- 12/ Applies to maximum mode timing only.
- 13/ Device 01 actively pulls the RG/GT pin to a logic one on the following clock cycle.
- 14/ If not tested, shall be guaranteed to the limits specified in table I.
- 15/ Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.

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Device type: 01			
Case outline Q			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	21	RESET
2	A14	22	READY
3	A13	23	$\overline{\text{TEST}}$
4	A12	24	$\overline{\text{INTA}}$ (QS1)
5	A11	25	ALE (QS0)
6	A10	26	$\overline{\text{DEN}}$ (S0)
7	A9	27	$\text{DT}/\overline{\text{R}}$ (S1)
8	A8	28	$\text{IO}/\overline{\text{M}}$ (S2)
9	AD7	29	$\overline{\text{WR}}$ (LOCK)
10	AD6	30	HLDA ( $\overline{\text{RQ}}/\overline{\text{GT1}}$ )
11	AD5	31	HOLD ( $\overline{\text{RQ}}/\overline{\text{GT0}}$ )
12	AD4	32	$\overline{\text{RD}}$
13	AD3	33	$\text{MN}/\overline{\text{MX}}$
14	AD2	34	$\overline{\text{SSO}}$ (HIGH)
15	AD1	35	A19/S6
16	AD0	36	A18/S5
17	NMI	37	A17/S4
18	INTR	38	A16/S3
19	CLK	39	A15
20	GND	40	V <sub>CC</sub>

NOTE: Parenthetical references apply to maximum mode only.

FIGURE 1. Terminal connections.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE <b>A</b>		<b>5962-86016</b>
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Device type: 01			
Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	23	NC
2	GND	24	RESET
3	A14	25	READY
4	A13	26	$\overline{\text{TEST}}$
5	A12	27	$\overline{\text{INTA}}$ (QS1)
6	A11	28	ALE (QS0)
7	A10	29	$\overline{\text{DEN}}$ ( $\overline{\text{S0}}$ )
8	A9	30	$\text{DT}/\overline{\text{R}}$ ( $\overline{\text{S1}}$ )
9	A8	31	$\text{IO}/\overline{\text{M}}$ ( $\overline{\text{S2}}$ )
10	AD7	32	$\overline{\text{WR}}$ ( $\overline{\text{LOCK}}$ )
11	AD6	33	HLDA ( $\overline{\text{RQ}}/\overline{\text{GT1}}$ )
12	AD5	34	HOLD ( $\overline{\text{RQ}}/\overline{\text{GT0}}$ )
13	AD4	35	$\overline{\text{RD}}$
14	AD3	36	$\overline{\text{MN}}/\overline{\text{MX}}$
15	AD2	37	$\overline{\text{SSO}}$ (HIGH)
16	AD1	38	A19/S6
17	AD0	39	NC
18	NC	40	A18/S5
19	NMI	41	A17/S4
20	INTR	42	A16/S3
21	CLK	43	A15
22	GND	44	V <sub>CC</sub>

NC = No connection

NOTE: Parenthetical references apply to maximum mode only.

FIGURE 1. Terminal connections - Continued.

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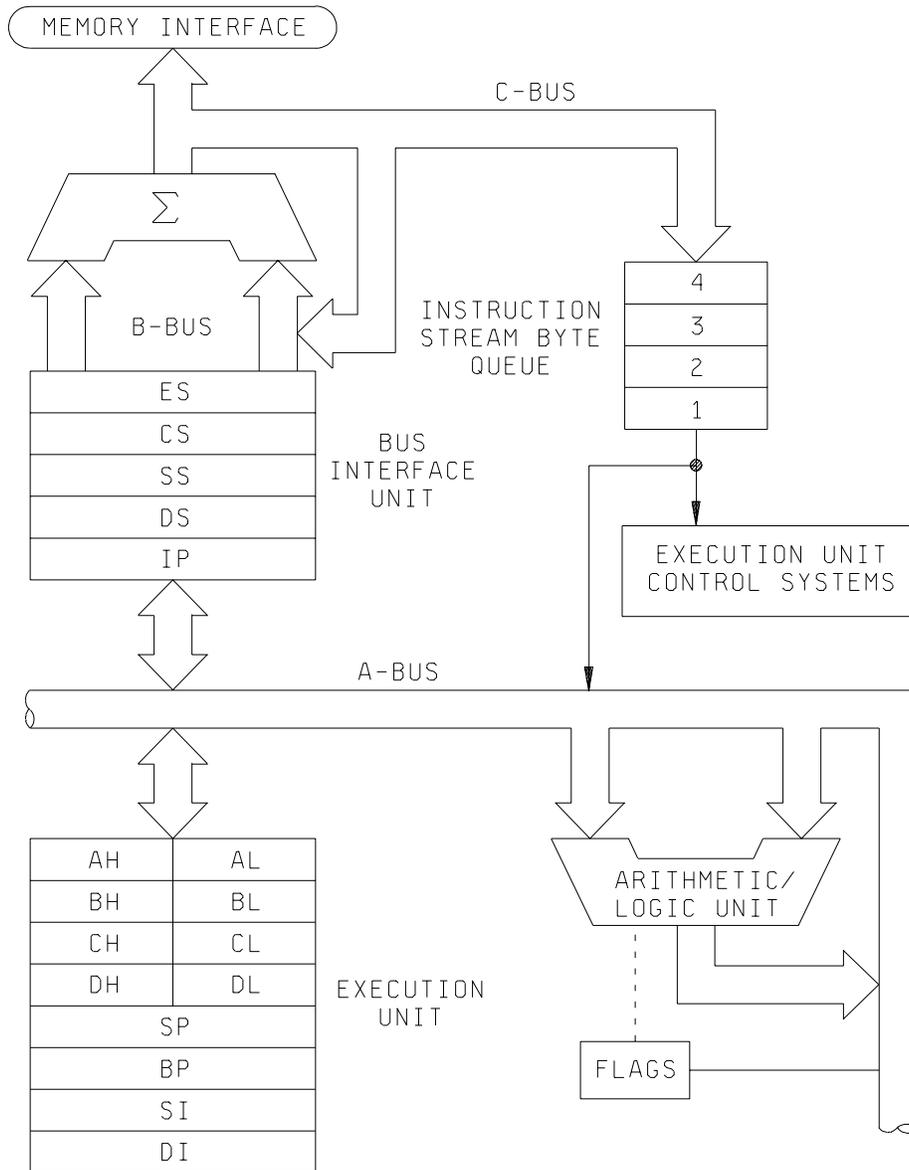
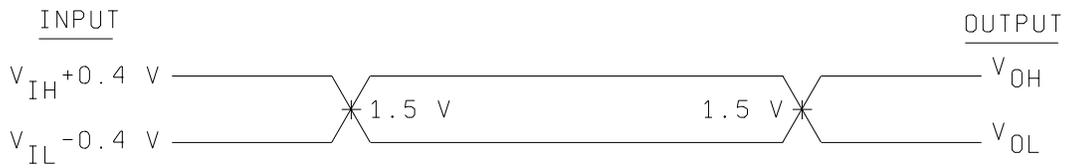
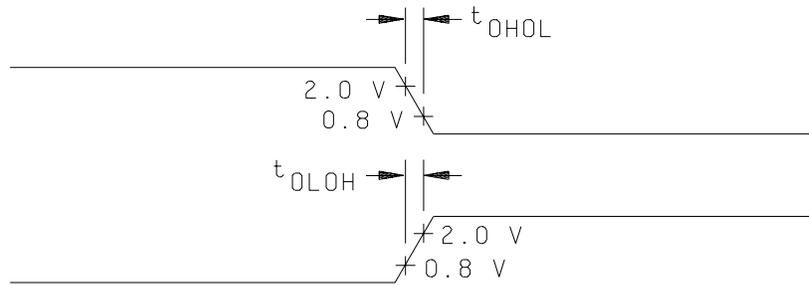
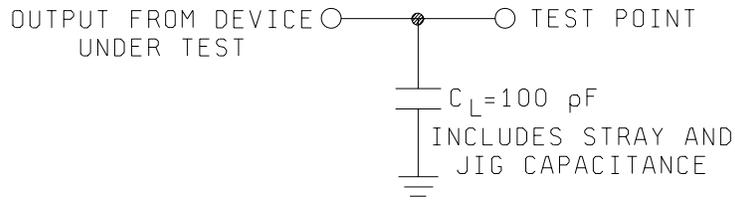


FIGURE 2. Block diagram.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE <b>A</b>		<b>5962-86016</b>
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NOTE: All input signals (other than CLK) must switch between  $V_{IL}(\text{max}) - 0.4 \text{ V}$  and  $V_{IH}(\text{min}) + 0.4 \text{ V}$ . CLK must switch between  $0.4 \text{ V}$  and  $V_{CC} - 0.4 \text{ V}$ . Input rise and fall times are driven at  $1.0 \text{ ns/V}$ .

FIGURE 3. Switching waveforms and test circuits.

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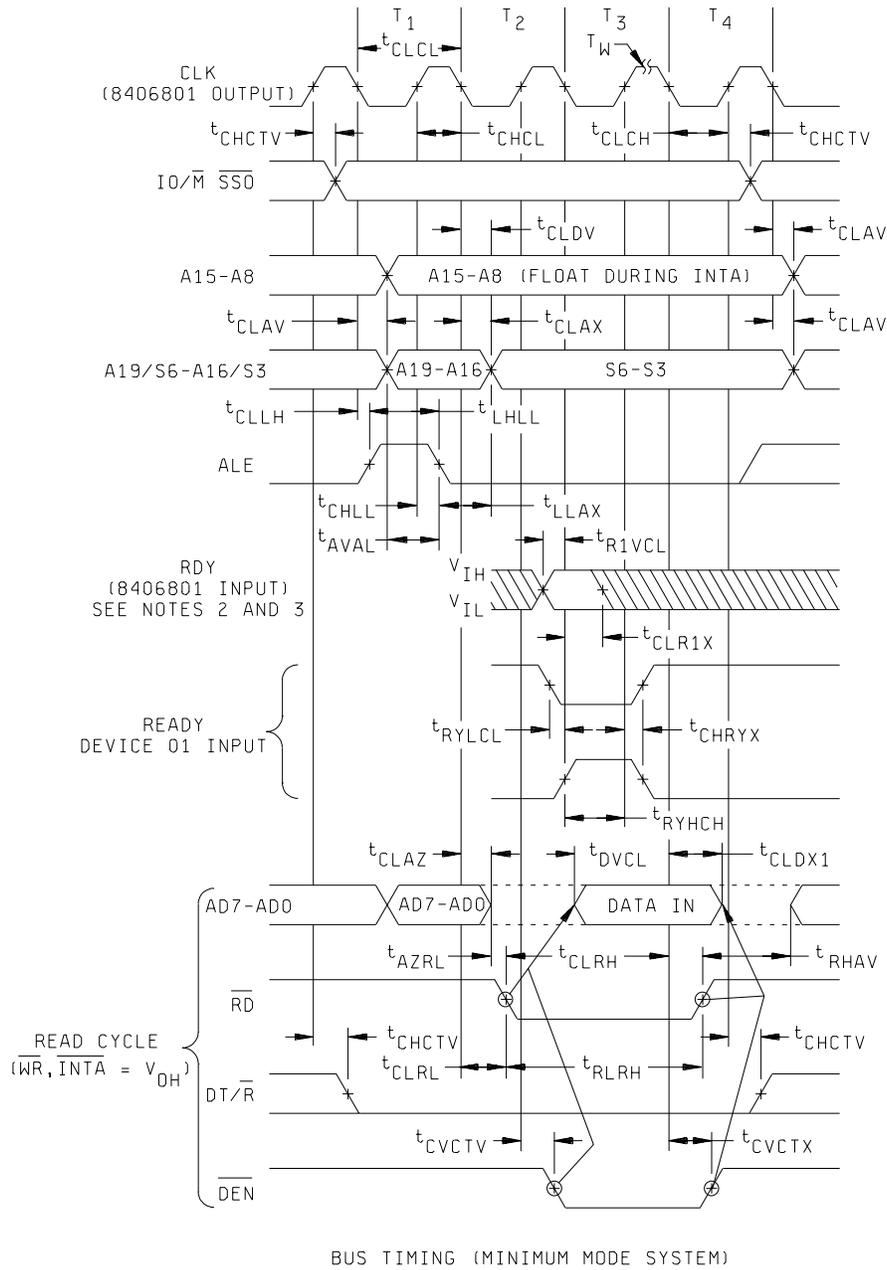


FIGURE 3. Switching waveforms and test circuits - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE <b>A</b>		<b>5962-86016</b>
		REVISION LEVEL <b>B</b>	SHEET <b>13</b>

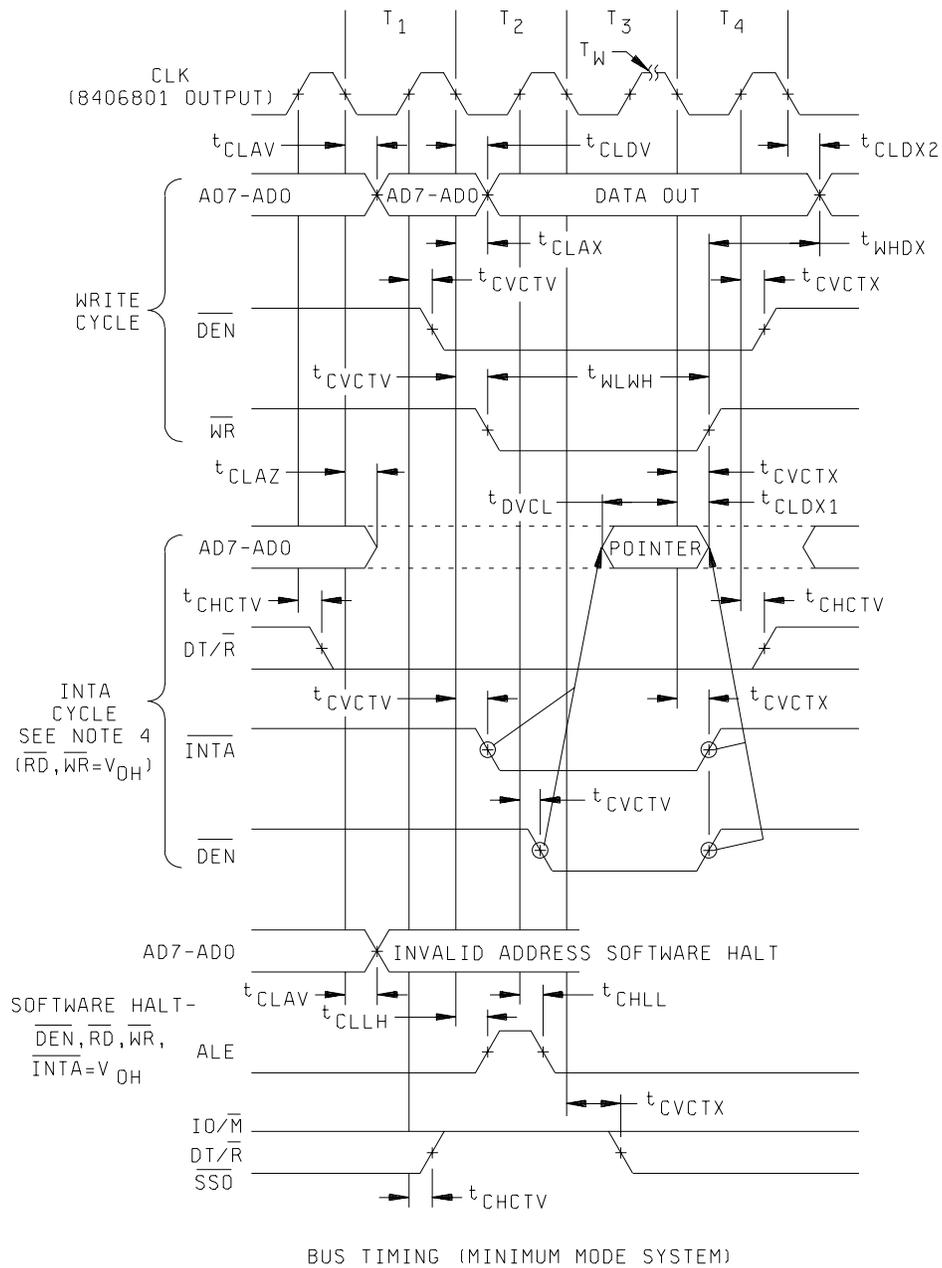


FIGURE 3. Switching waveforms and test circuits - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE <b>A</b>		<b>5962-86016</b>
		REVISION LEVEL <b>B</b>	SHEET <b>14</b>

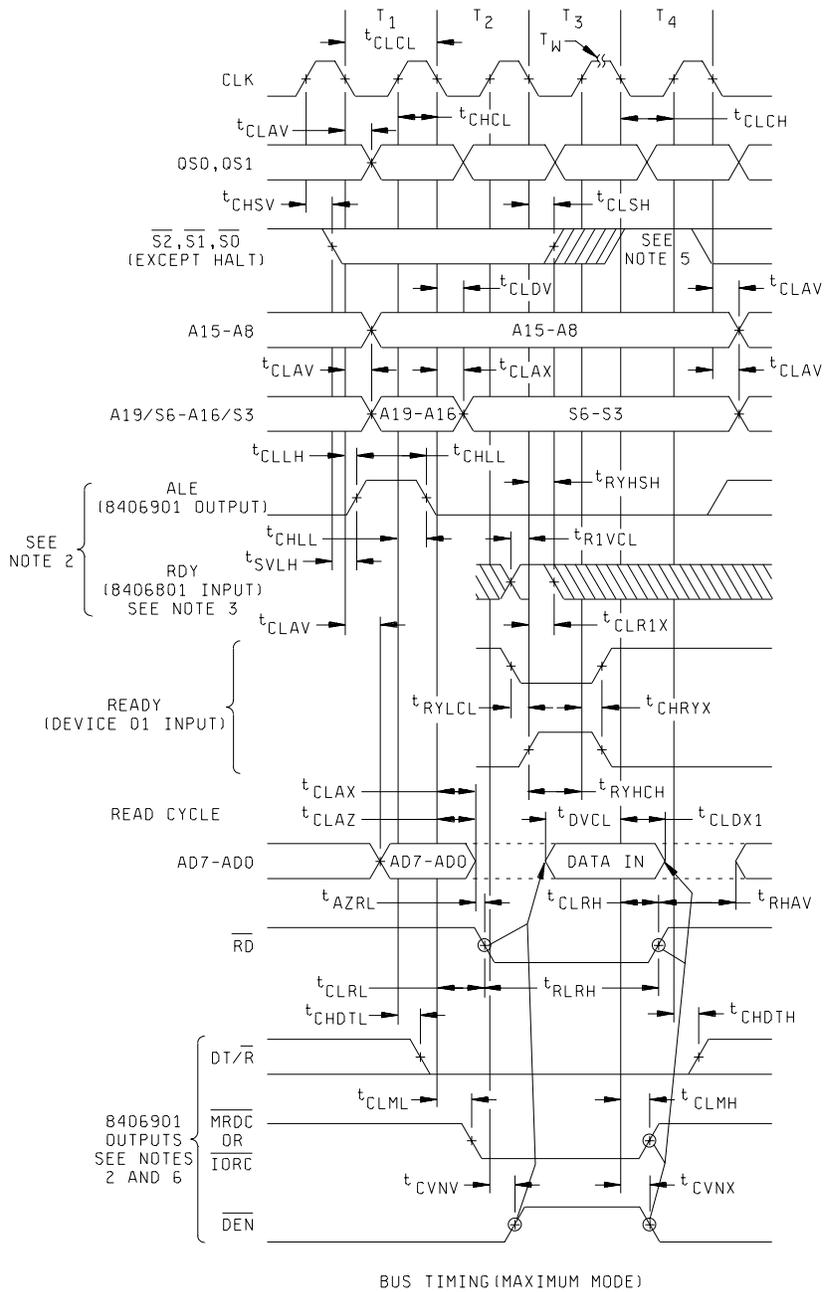


FIGURE 3. Switching waveforms and test circuits - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE <b>A</b>		<b>5962-86016</b>
		REVISION LEVEL <b>B</b>	SHEET <b>15</b>

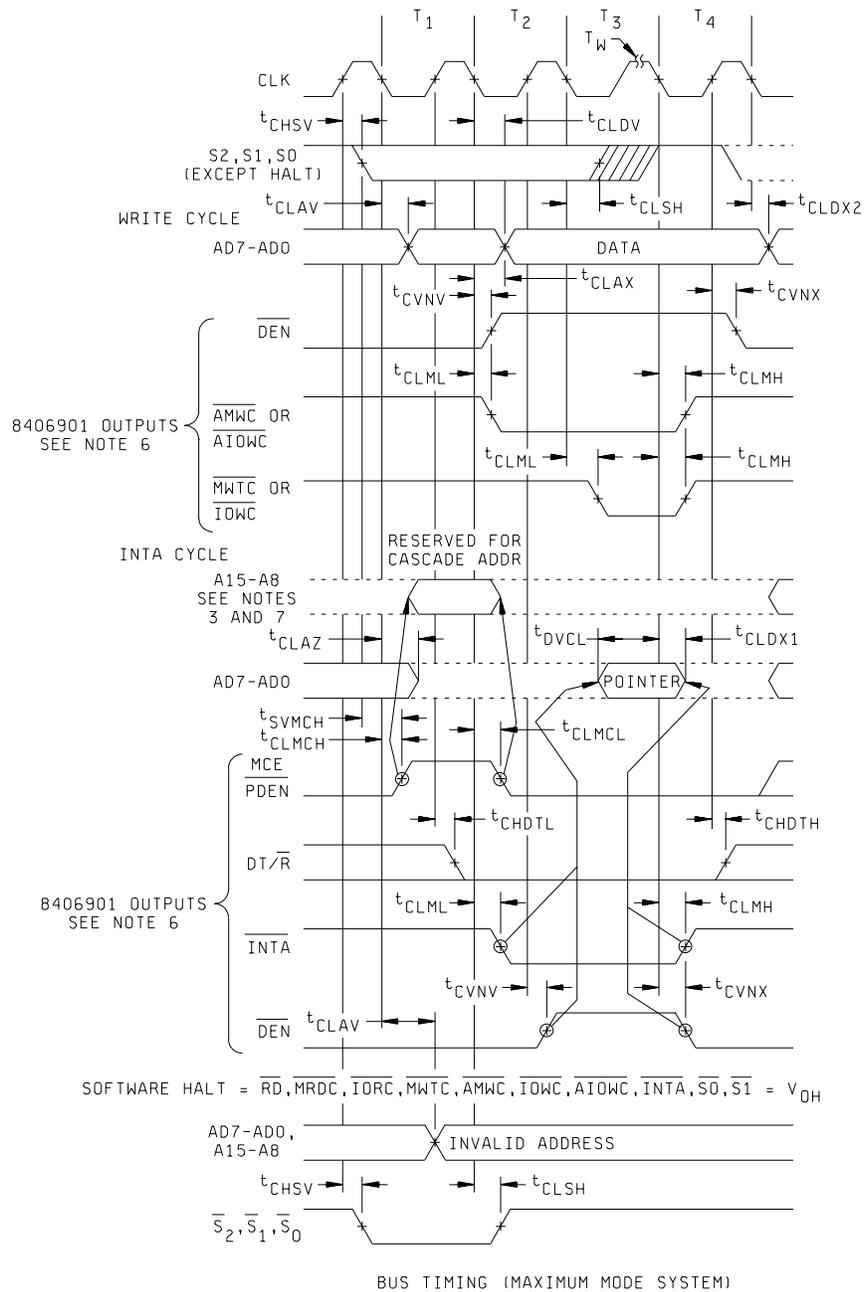


FIGURE 3. Switching waveforms and test circuits - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE <b>A</b>		<b>5962-86016</b>
		REVISION LEVEL <b>B</b>	SHEET <b>16</b>

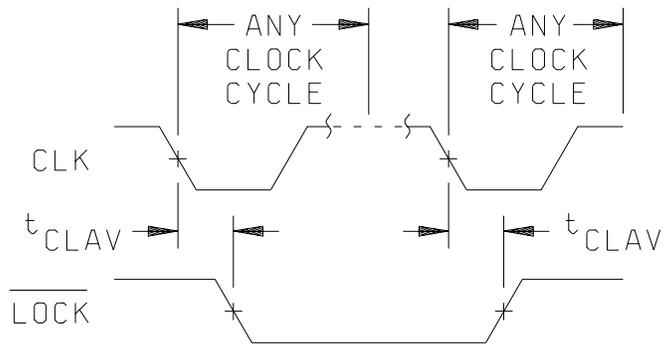
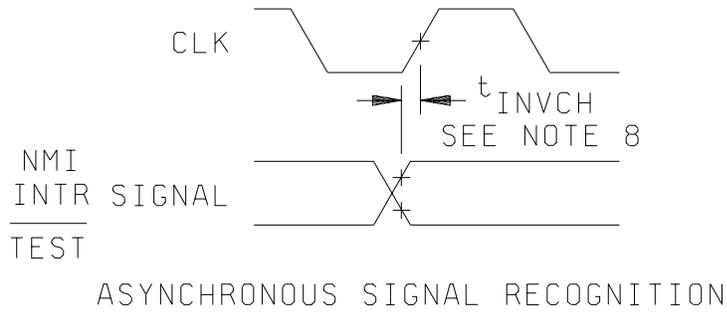
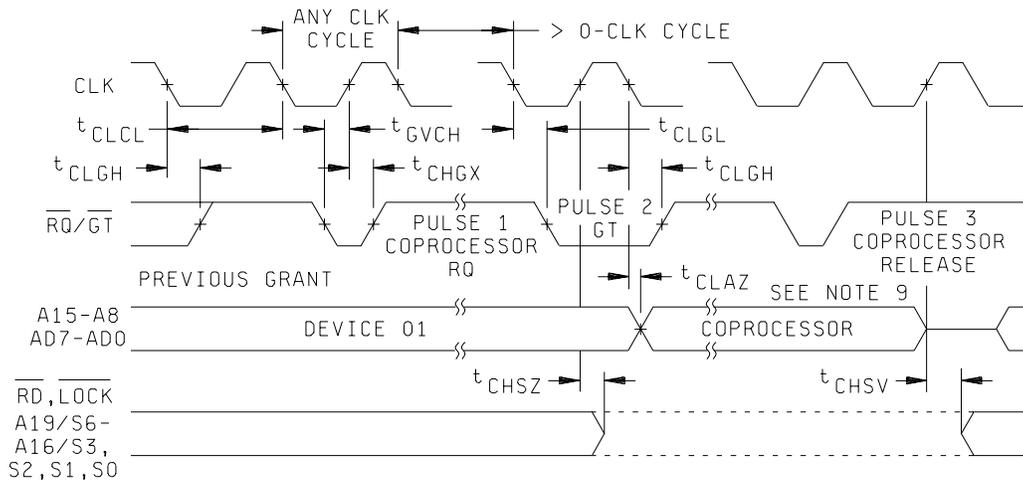
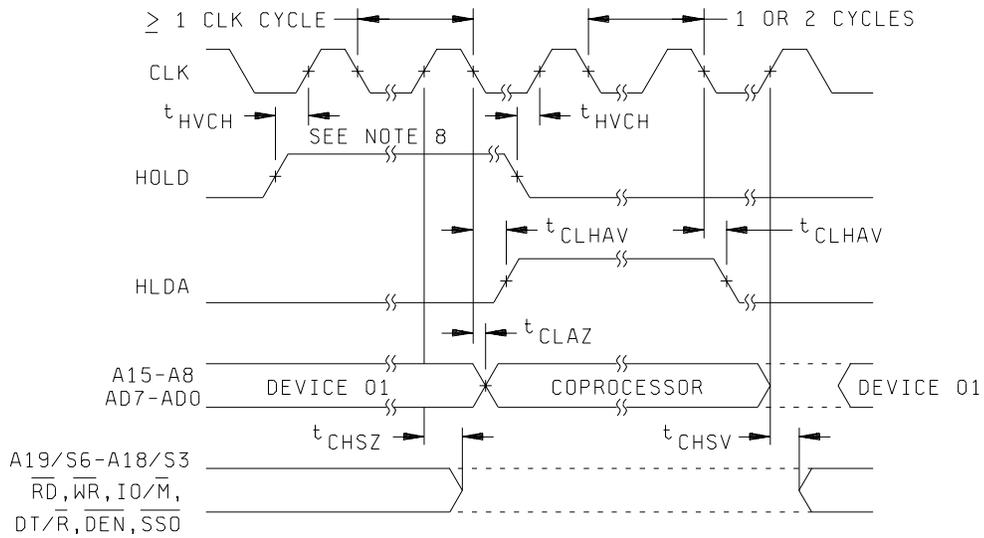


FIGURE 3. Switching waveforms and test circuits - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE <b>A</b>		<b>5962-86016</b>
		REVISION LEVEL <b>B</b>	SHEET <b>17</b>



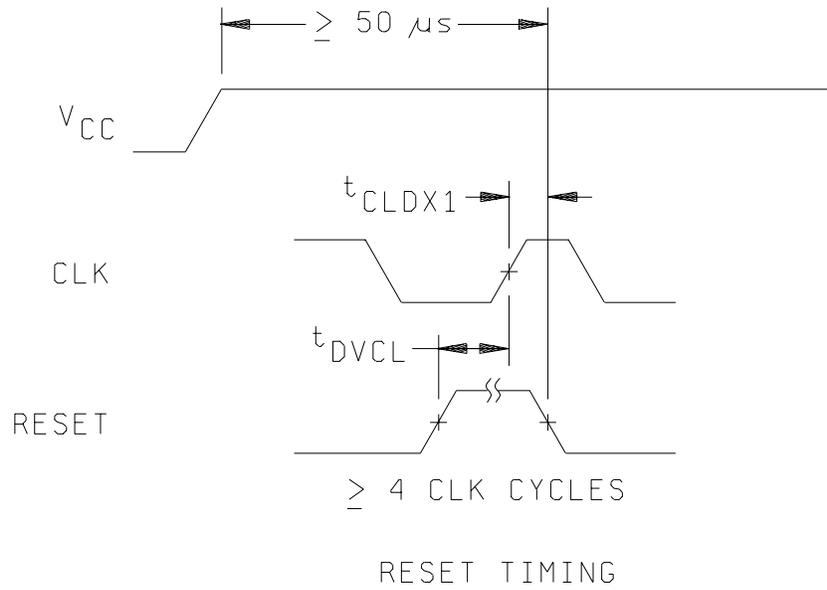
REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)

FIGURE 3. Switching waveforms and test circuits - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE <b>A</b>		<b>5962-86016</b>
		REVISION LEVEL <b>B</b>	SHEET <b>18</b>



**NOTES:**

1. All timing measurements are made at 1.5 V and all signals switch between  $V_{OH}$  and  $V_{OL}$ , unless otherwise specified.
2. Signals referencing military drawings 84068 and 84069 are shown only for informational purposes.
3. RDY is sampled near the end of T2, T3, and TW to determine if TW machine states are to be inserted.
4. Two INTA cycles run back-to-back. Device 01 local ADDR/DATA bus is floating during both INTA cycles. Control signals are shown for the INTA cycle.
5. Status inactive in state just prior to T4.
6. The issuance of drawing 84069 command and control signals ( $\overline{MDRC}$ ,  $\overline{MWTC}$ ,  $\overline{AMWC}$ ,  $\overline{IORC}$ ,  $\overline{IOWC}$ ,  $\overline{AIOWC}$ ,  $\overline{INTA}$ , and DEN) lags the active high 84069 CEN.
7. Cascade address is valid between first and second  $\overline{INTA}$  cycles.
8. Setup requirements for asynchronous signals only to guarantee recognition at next CLK.
9. The coprocessor may not drive the busses outside the region shown without risking contention.

FIGURE 3. Switching waveforms and test circuits - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE <b>A</b>		<b>5962-86016</b>
		REVISION LEVEL <b>B</b>	SHEET <b>19</b>

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
  - (1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 7, 9

\* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 ( $C_{IN}$ ,  $C_{OUT}$ , and  $C_{I/O}$  measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A sample size of fifteen devices with zero rejects shall be required, and all input and output terminals shall be tested.
- d. Subgroups 7 and 8 shall include verification of the programming set and functionality of the device. These tests form a part of the manufacturers test tape and shall be maintained and available from the approved source of supply.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Pin descriptions. Pin descriptions shall be as specified in table III herein.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE <b>A</b>		<b>5962-86016</b>
		REVISION LEVEL <b>B</b>	SHEET <b>21</b>

TABLE III. Pin descriptions.

<u>Minimum and maximum system mode</u>																	
<p>The following pin descriptions are for device 01 system in either minimum or maximum mode. The "local bus" in these descriptions is the direct multiplexed bus interface connection to device 01 (without regard to additional bus buffers).</p>																	
<u>Name</u>	<u>I/O</u>	<u>Description</u>															
AD7 – AD0	I/O	<u>Address data bus.</u> These data lines constitute the time multiplexed memory/I/O ADDRESS (T1) and data (T2, T3, TW, and T4) bus. These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".															
A15 – A8	O	<u>Address bus.</u> These lines provide address bits 8 through 15 for the entire bus cycle (T1-T4). These lines do not have to be latched by ALE to remain valid. A15 – A8 are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".															
A19/S6, A18/S5, A17/S4, A16/S3	O	<p><u>Address/status.</u> During T1, these are the four most significant address lines for memory operations. During I/O operations, these lines are LOW. During memory and I/O operations, status information is available on these lines during T2, T3, TW, and T4. S6 is always LOW. The status of the interrupt enable flat bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown.</p> <p>This information indicates which segment register is presently being used for data accessing.</p> <p>These lines float to 3-state OFF during local bus "hold acknowledge".</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>S4</th> <th>S3</th> <th>Characteristics</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td>Alternate data</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td>Stack</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td>Code or none</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td>Data</td> </tr> </tbody> </table>	S4	S3	Characteristics	0	0	Alternate data	0	1	Stack	1	0	Code or none	1	1	Data
S4	S3	Characteristics															
0	0	Alternate data															
0	1	Stack															
1	0	Code or none															
1	1	Data															
$\overline{RD}$	O	<u>Read.</u> Read strobe indicates that the processor is performing a memory or I/O read cycle depending on the state of the IO/M pin or S2. This signal is used to read devices which reside on device 01 local bus. $\overline{RD}$ is active LOW during T2, T3, and TW of any read cycle, and is guaranteed to remain HIGH in T2 until device 01 local bus has floated. This signal floats to 3-state OFF in "hold acknowledge".															
READY	I	<u>READY.</u> The acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory or I/O is synchronized by military drawing PIN 8406801 clock generator to form READY. This signal is active HIGH. Device 01 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.															
INTR	I	<u>Interrupt request.</u> A level-triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.															
$\overline{TEST}$	I	<u>TEST.</u> Input is examined by the "wait for test" instruction. If the $\overline{TEST}$ input is LOW, execution continues; otherwise, the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.															

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		REVISION LEVEL <b>B</b>	SHEET <b>22</b>

TABLE III. Pin descriptions - Continued.

<u>Minimum and maximum system mode</u> - Continued		
<u>Name</u>	<u>I/O</u>	<u>Description</u>
NMI	I	<u>Nonmaskable interrupt</u> . An edge-triggered input which causes a type 2 interrupt. A subroutine is vectored via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	I	<u>RESET</u> . Causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized.
CLK	I	<u>Clock</u> . Provides the basic timing for the processor and bus controller. It is asymmetric with a 33 percent duty cycle to provide optimized internal timing.
V <sub>CC</sub>		V <sub>CC</sub> . The +5.0 V ±10% power supply pin.
GND		<u>GND</u> . The ground pins.
MN/MX		<u>Minimum/maximum</u> . Indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

Minimum system mode

The following pin descriptions are for device 01 system in minimum mode (i.e., MN/MX = V<sub>CC</sub>). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described previously.

<u>Name</u>	<u>I/O</u>	<u>Description</u>
IO/M	O	<u>Status line</u> . An inverted maximum mode S <sub>2</sub> . It is used to distinguish a memory access from an I/O access. IO/M becomes valid in the T <sub>4</sub> preceding a bus cycle and remains valid until the final T <sub>4</sub> of the cycle (I/O = HIGH, M = LOW). IO/M floats to 3-state OFF in local bus "hold acknowledge".
WR	O	<u>Write</u> . Strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the IO/M signal. WR is active for T <sub>2</sub> , T <sub>3</sub> , and TW of any write cycle. It is active LOW and floats to 3-state OFF in local bus "hold acknowledge".
INTA	O	<u>INTA</u> . Used as a read strobe for interrupt acknowledge cycles. It is active LOW during T <sub>2</sub> , T <sub>3</sub> , and TW of each interrupt acknowledgement cycle.
ALE	O	<u>Address latch enable</u> . Provided by the processor to latch the address into military drawing PIN 8406701 or 8406702 address latch. It is a HIGH pulse active during clock low of T <sub>1</sub> of any bus cycle. Note that ALE is never floated.
DT/R	O	<u>Data transmit/receive</u> . Needed in a minimum system that desires to use military drawing PIN's 5962-8757701 or 5962-8757702 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/R is equivalent to S <sub>1</sub> in the maximum mode, and its timing is the same for IO/M (T-HIGH, R-LOW). This signal floats to 3-state OFF in local bus "hold acknowledge".
DEN	O	<u>Data enable</u> . Provided as an output enable for military drawing PIN's 5962-8757701 or 5962-8757702 in a minimum system that uses the transceiver. DEN is active LOW during each memory and I/O access and for INTA cycles. For a read or INTA cycle, it is active from the middle of T <sub>2</sub> until the middle of T <sub>4</sub> ; while for a write cycle, it is active from the beginning of T <sub>2</sub> until the middle of T <sub>4</sub> . DEN floats to 3-state OFF during local bus "hold acknowledge".

**STANDARD  
MICROCIRCUIT DRAWING**  
DEFENSE SUPPLY CENTER COLUMBUS  
COLUMBUS, OHIO 43216-5000

SIZE  
**A**

**5962-86016**

REVISION LEVEL  
**B**

SHEET  
**23**

TABLE III. Pin descriptions - Continued.

Minimum system mode - Continued																																						
Name	I/O	Description																																				
HOLD, HLDA	I O	<u>HOLD</u> . Indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement, in the middle of a T4 or T1 clock cycle. Simultaneous with the issuance of HLDA, the processor will float the local bus and control the lines. After HOLD is detected as being LOW, the processor lowers HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. Hold is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.																																				
$\overline{\text{SSO}}$	O	<u>Status line</u> . Logically equivalent to $\overline{\text{S0}}$ in the maximum mode. The combination of SSO, IO/M and DT/R allows the system to completely decode the current bus cycle status. SSO is held to high impedance logic one during local bus "hold acknowledge". <table border="1" data-bbox="570 709 1338 1031"> <thead> <tr> <th>IO/M</th> <th>DT/R</th> <th><math>\overline{\text{SSO}}</math></th> <th>Characteristics</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Interrupt acknowledge</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Read I/O port</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Write I/O port</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Halt</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Code access</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Read memory</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Write memory</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Passive</td> </tr> </tbody> </table>	IO/M	DT/R	$\overline{\text{SSO}}$	Characteristics	1	0	0	Interrupt acknowledge	1	0	1	Read I/O port	1	1	0	Write I/O port	1	1	1	Halt	0	0	0	Code access	0	0	1	Read memory	0	1	0	Write memory	0	1	1	Passive
IO/M	DT/R	$\overline{\text{SSO}}$	Characteristics																																			
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0	1	1	Passive																																			

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE <b>A</b>		<b>5962-86016</b>
		REVISION LEVEL <b>B</b>	SHEET <b>24</b>

TABLE III. Pin descriptions - Continued.

<u>Maximum system mode</u>																																						
<p>The following pin descriptions are for device 01 system in maximum mode (i.e., <math>\overline{MN/\overline{MX}} = \text{GND}</math>). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described previously.</p>																																						
<u>Name</u>	<u>I/O</u>	<u>Description</u>																																				
$\overline{S0}$ $\overline{S1}$ $\overline{S2}$	O O O	<p><u>Status.</u> Active during clock high of T4, T1, and T2, and is returned to the passive state (1, 1, 1) during T3 or during TW when READY is HIGH. This status is used by military drawing PIN 8406901 bus controller to generate all memory and I/O access control signals. Any change by S2, S1, or S0 during T4 is used to indicate the end of a bus cycle.</p> <p>These signals are held at a high impedance logic one state during "grant sequence".</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="text-align: center;"><math>\overline{S2}</math></th> <th style="text-align: center;"><math>\overline{S1}</math></th> <th style="text-align: center;"><math>\overline{S0}</math></th> <th style="text-align: center;">Characteristics</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td>Interrupt acknowledge</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td>Read I/O port</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td>Write I/O port</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td>Halt</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td>Code access</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td>Read memory</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td>Write memory</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td>Passive</td> </tr> </tbody> </table>	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics	0	0	0	Interrupt acknowledge	0	0	1	Read I/O port	0	1	0	Write I/O port	0	1	1	Halt	1	0	0	Code access	1	0	1	Read memory	1	1	0	Write memory	1	1	1	Passive
$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics																																			
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1	0	0	Code access																																			
1	0	1	Read memory																																			
1	1	0	Write memory																																			
1	1	1	Passive																																			
$\overline{RQ/GT0}$ , $\overline{RQ/GT1}$	I/O	<p><u>Request/grant.</u> Pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bi-directional with RQ/GT0 having higher priority than RQ/GT1. RQ/GT has internal bus-hold high circuitry and, if unused, may be left unconnected. The request/grant sequence is as follows (see RQ/GT timing sequence):</p> <ol style="list-style-type: none"> <li>1. A pulse of one CLK wide from another local bus master indicates a local bus request ("hold") to device 01 (pulse 1).</li> <li>2. During a T4 or T1 clock cycle, a pulse one clock wide from device 01 to the requesting master (pulse 2), indicates that device 01 has allowed the local bus to float and that it will enter the "grant sequence" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "grant sequence".</li> </ol>																																				

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE <b>A</b>		<b>5962-86016</b>
		REVISION LEVEL <b>B</b>	SHEET <b>25</b>

TABLE III. Pin descriptions - Continued.

<u>Maximum system mode</u> - Continued		
<u>Name</u>	<u>I/O</u>	<u>Description</u>
$\overline{RQ/GT0}$ , $\overline{RQ/GT1}$ (continued)		<p>3. A pulse of one CLK wide from the requesting master indicates to device 01 (pulse 3) that the "hold" request is about to end and that device 01 can reclaim the local bus at the next CLK. The CPU then enters T4 (or T1 if no bus cycles pending).</p> <p>Each master-master exchange of the local bus is a sequence of three pulses. There must be one idle CLK cycle after bus exchange. Pulses are active LOW.</p> <p>If the request is made while the CPU is performing a memory cycle, it will release the local bus during the T4 of the cycle when all the following conditions are met:</p> <ol style="list-style-type: none"> <li>1. Request occurs on or before T2.</li> <li>2. Current cycle is not the low bit of a word.</li> <li>3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence.</li> <li>4. A locked instruction is not currently executing.</li> </ol> <p>If the local bus is idle when the request is made, the two possible events will follow:</p> <ol style="list-style-type: none"> <li>1. Local bus will be released during the next clock.</li> <li>2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.</li> </ol>
$\overline{LOCK}$	O	<p><math>\overline{LOCK}</math>. Indicates that other system bus masters are not to gain control of the system bus while LOCK is active (LOW). The LOCK signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and is held at a high impedance logic one state during "grant sequence". In Max Mode, LOCK is automatically generated during T2 of the first INTA cycle and removed during T2 of the second INTA cycle.</p>

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE <b>A</b>		<b>5962-86016</b>
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TABLE III. Pin descriptions - Continued.

<u>Maximum system mode</u> - Continued																	
<u>Name</u>	<u>I/O</u>	<u>Description</u>															
QS1, QS0	O	<p><u>Queue status.</u> Provide status to allow external tracking of the internal device 01 instruction queue.</p> <p>The queue status is valid during the CLK cycle after which the queue operation is performed. Note that the queue status never goes to a high impedance state (floated).</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="text-align: center;">QS1</th> <th style="text-align: center;">QS0</th> <th style="text-align: center;">Characteristics</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td>No operation</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td>First byte of Opcode from queue</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td>Empty the queue</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td>Subsequent byte from queue</td> </tr> </tbody> </table>	QS1	QS0	Characteristics	0	0	No operation	0	1	First byte of Opcode from queue	1	0	Empty the queue	1	1	Subsequent byte from queue
QS1	QS0	Characteristics															
0	0	No operation															
0	1	First byte of Opcode from queue															
1	0	Empty the queue															
1	1	Subsequent byte from queue															
HIGH	O	Pin 34 is always a logic one in the maximum mode and is held at a high impedance logic one during a "grant sequence".															

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		REVISION LEVEL <b>B</b>	SHEET <b>27</b>

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 03-08-11

Approved sources of supply for SMD 5962-86016 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8601601QA	34371	MD80C88/883
5962-8601601XA	<u>3/</u>	MR80C88/883

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE  
number

34371

Vendor name  
and address

Intersil Corporation  
2401 Palm Bay Blvd  
P.O. Box 883  
Melbourne, FL 32902-0883

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.