REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add vendor CAGE 01295 to case outlines R and 2. Add vendor CAGE 27014 to case outline 2.	87-09-23	M. A. Frye
B	Change CAGE code to 67268. Add case outline S to drawing. Add vendor CAGE 01295 to case outline S. Remove vendor CAGE 04713 from drawing. Editorial changes to table I. Editorial changes throughout.	89-07-24	M. A. Frye
C	Update boilerplate to MIL-PRF-38535 requirements. - jak	01-12-04	Thomas M. Hess

The first page of this drawing has been changed.

Current CAGE CODE is 67268

REV																			
SHEET																			
REV																			
SHEET																			

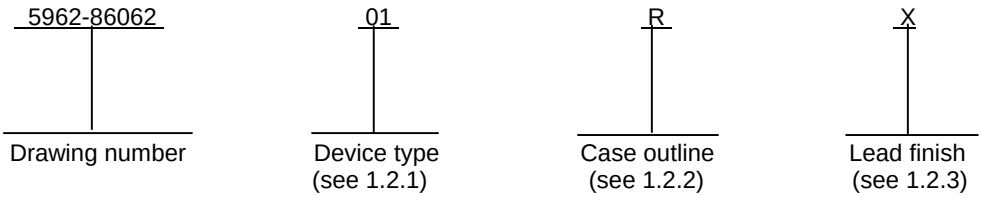
REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A	PREPARED BY Greg A. Pitz	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING	CHECKED BY D. A. DiCenzo	
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	APPROVED BY Nelson A. Hauck DRAWING APPROVAL DATE 86-07-17 REVISION LEVEL C	MICROCIRCUIT, DIGITAL, HIGH-SPEED CMOS, OCTAL INVERTING D-TYPE LATCH WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON SIZE **A** / CAGE CODE **14933** / **5962-86062** SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HC563	Octal inverting D-type latch with three-state outputs

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V dc to +7.0 V dc
DC input voltage range ..... -0.5 V dc to V_{CC} +0.5 V dc
DC output voltage range ..... -0.5 V dc to V_{CC} +0.5 V dc
DC input diode current ..... ± 20 mA
DC output diode current ..... ± 20 mA
DC output current (per pin) ..... ± 35 mA
DC V_{CC} or GND current (per pin) ..... ± 70 mA
Maximum power dissipation (P_D) ..... 500 mW 2/
Lead temperature (soldering, 10 seconds) ..... +260°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C

1/ Unless otherwise specified, all voltages are referenced to ground.
2/ For T_C = +100°C to +125°C, derate linearly at 12 mW/°C.

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})..... +2.0 V dc to +6.0 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C
Input rise or fall time:

V_{CC} = 2.0 V..... 0 to 1000 ns
V_{CC} = 4.5 V..... 0 to 500 ns
V_{CC} = 6.0 V..... 0 to 400 ns

Minimum setup time (t_S):

T_C = +25°C:
V_{CC} = 2.0 V..... 75 ns
V_{CC} = 4.5 V..... 15 ns
V_{CC} = 6.0 V..... 13 ns

T_C = -55°C/+125°C:
V_{CC} = 2.0 V..... 110 ns
V_{CC} = 4.5 V..... 22 ns
V_{CC} = 6.0 V..... 19 ns

Minimum hold time (t_h):

T_C = +25°C:
V_{CC} = 2.0 V..... 50 ns
V_{CC} = 4.5 V..... 10 ns
V_{CC} = 6.0 V..... 9 ns

T_C = -55°C/+125°C:
V_{CC} = 2.0 V..... 75 ns
V_{CC} = 4.5 V..... 15 ns
V_{CC} = 6.0 V..... 13 ns

Minimum pulse width (t_W):

T_C = +25°C:
V_{CC} = 2.0 V..... 80 ns
V_{CC} = 4.5 V..... 16 ns
V_{CC} = 6.0 V..... 14 ns

T_C = -55°C°+125°C:
V_{CC} = 2.0 V..... 120 ns
V_{CC} = 4.5 V..... 24 ns
V_{CC} = 6.0 V..... 20 ns

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 and QML-38535 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

Table I. Electrical performance characteristics.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 20$ µA	V_{CC} = 2.0 V	1, 2, 3	1.9		V
			V_{CC} = 4.5 V		4.4		
			V_{CC} = 6.0 V		5.9		
		$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 6.0$ mA	V_{CC} = 4.5 V		3.7		
		$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 7.8$ mA	V_{CC} = 6.0 V		5.2		
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 20$ µA	V_{CC} = 2.0 V	1, 2, 3		0.1	V
			V_{CC} = 4.5 V			0.1	
			V_{CC} = 6.0 V			0.1	
		$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 6.0$ mA	V_{CC} = 4.5 V			0.4	
		$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 7.8$ mA	V_{CC} = 6.0 V			0.4	
High-level input voltage	V_{IH} 2/		V_{CC} = 2.0 V	1, 2, 3	1.5		V
			V_{CC} = 4.5 V		3.15		
			V_{CC} = 6.0 V		4.2		
Low-level input voltage	V_{IL} 2/		V_{CC} = 2.0 V	1, 2, 3		0.3	V
			V_{CC} = 4.5 V			0.9	
			V_{CC} = 6.0 V			1.2	
Input capacitance	C_{IN}	V_{IN} = 0.0 V, T_C = +25°C See 4.3.1c		4		10	pF
Quiescent current	I_{CC}	$V_{IN} = V_{CC}$ or GND V_{CC} = 6.0 V		1, 2, 3		160	µA
Input leakage current	I_{IN}	$V_{IN} = V_{CC}$ or GND V_{CC} = 6.0 V		1, 2, 3		±1.0	µA
Three-state output leakage current	I_{OZ}	$V_{OUT} = V_{CC}$ or GND $V_{IN} = V_{IH}$ or V_{IL}		1, 2, 3		±10.0	µA
Input capacitance	C_{OUT}	V_{IN} = 0.0 V, T_C = +25°C See 4.3.1c		4		20	pF
Functional tests		See 4.3.1d		7			
Propagation delay, time, Dn to On	t_{PLH1}, t_{PHL1} 3/	C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		175	ns
				10, 11		265	
			V_{CC} = 4.5 V	9		35	
				10, 11		53	
			V_{CC} = 6.0 V	9		30	
				10, 11		45	

See footnotes at end of table.

Table I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay, time, LE to On	t_{PLH2}, t_{PHL2} 3/	C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		175	ns
				10, 11		265	
			V_{CC} = 4.5 V	9		35	
				10, 11		53	
			V_{CC} = 6.0 V	9		30	
				10, 11		45	
Propagation delay, time, output enable, OE to On	t_{PZH}, t_{PZL} 3/	C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		175	ns
				10, 11		265	
			V_{CC} = 4.5 V	9		35	
				10, 11		53	
			V_{CC} = 6.0 V	9		30	
				10, 11		45	
Propagation delay, time, output disable, OE to On	t_{PHZ}, t_{PLZ} 3/	C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		150	ns
				10, 11		225	
			V_{CC} = 4.5 V	9		30	
				10, 11		45	
			V_{CC} = 6.0 V	9		26	
				10, 11		38	
Transition time, output rise and fall	t_{THL}, t_{TLH} 4/	C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		60	ns
				10, 11		90	
			V_{CC} = 4.5 V	9		12	
				10, 11		18	
			V_{CC} = 6.0 V	9		10	
				10, 11		15	

1/ For a power supply of 5.0 V ±10% the worst case output voltage (V_{OH} and V_{OL}) occur for HC at 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst case V_{IN} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V, respectively. (The V_{IH} value at V_{CC} = 5.5 V is 3.85 V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage so the 6.0 V values should be used. Power dissipation capacitance (C_{PD}), typically 50 pF, determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}2 f+I_{CC} V_{CC}$; and the no load dynamic current consumption, $I_S = C_{PD}V_{CC}f+I_{CC}$.

2/ V_{IH} and V_{IL} tests not required if applied as forcing functions for V_{OH} or V_{OL}.

3/ AC testing at V_{CC} = 2.0 V and V_{CC} = 6.0 V shall be guaranteed, if not tested, to the limits specified in table I.

4/ Transition times (t_{TLH}, t_{THL}) shall be guaranteed, if not tested, to the limits specified in table I.

Device type	01
Case outlines	R,S and 2
Terminal number	Terminal symbol
1	$\overline{OE}$
2	D_0
3	D_1
4	D_2
5	D_3
6	D_4
7	D_5
8	D_6
9	D_7
10	GND
11	$\overline{LE}$
12	$\overline{O_7}$
13	$\overline{O_6}$
14	$\overline{O_5}$
15	$\overline{O_4}$
16	$\overline{O_3}$
17	$\overline{O_2}$
18	$\overline{O_1}$
19	$\overline{O_0}$
20	V_{CC}

Pin Description	
Symbol	Description
Dn (n = 0 to 7)	Data inputs
$\overline{On}$ (n = 0 to 7)	Data outputs
$\overline{LE}$	Latch enable control input (active low)
$\overline{OE}$	Output enable control input (active low)

FIGURE 1. Terminal connections.

Inputs			Outputs
$\overline{OE}$	$\overline{LE}$	Dn	$\overline{On}$
L	H	H	L
L	H	L	H
L	L	l	H
L	L	h	L
H	X	X	Z

H = High voltage level
L = Low voltage level
X = Irrelevant
Z = High impedance
l = Low voltage level one set-up time prior to the high to low latch enable transition
h = High voltage level one set-up time prior to the high to low latch enable transition

FIGURE 2. Truth table.

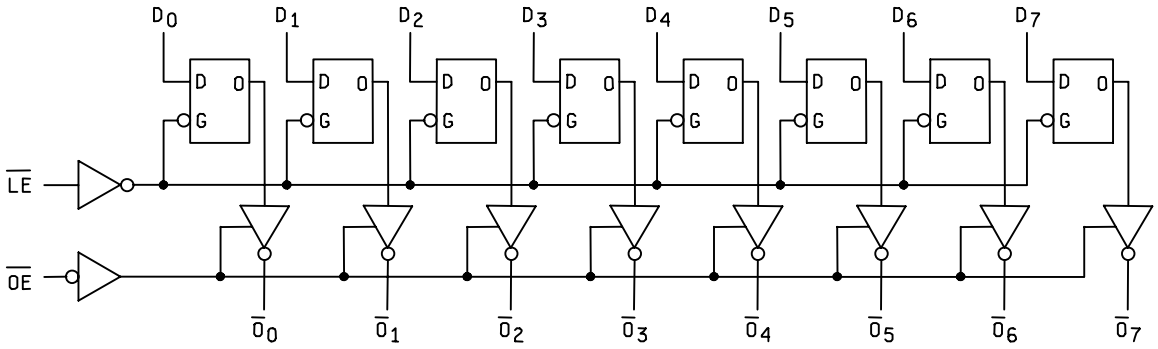


FIGURE 3. Logic diagram.

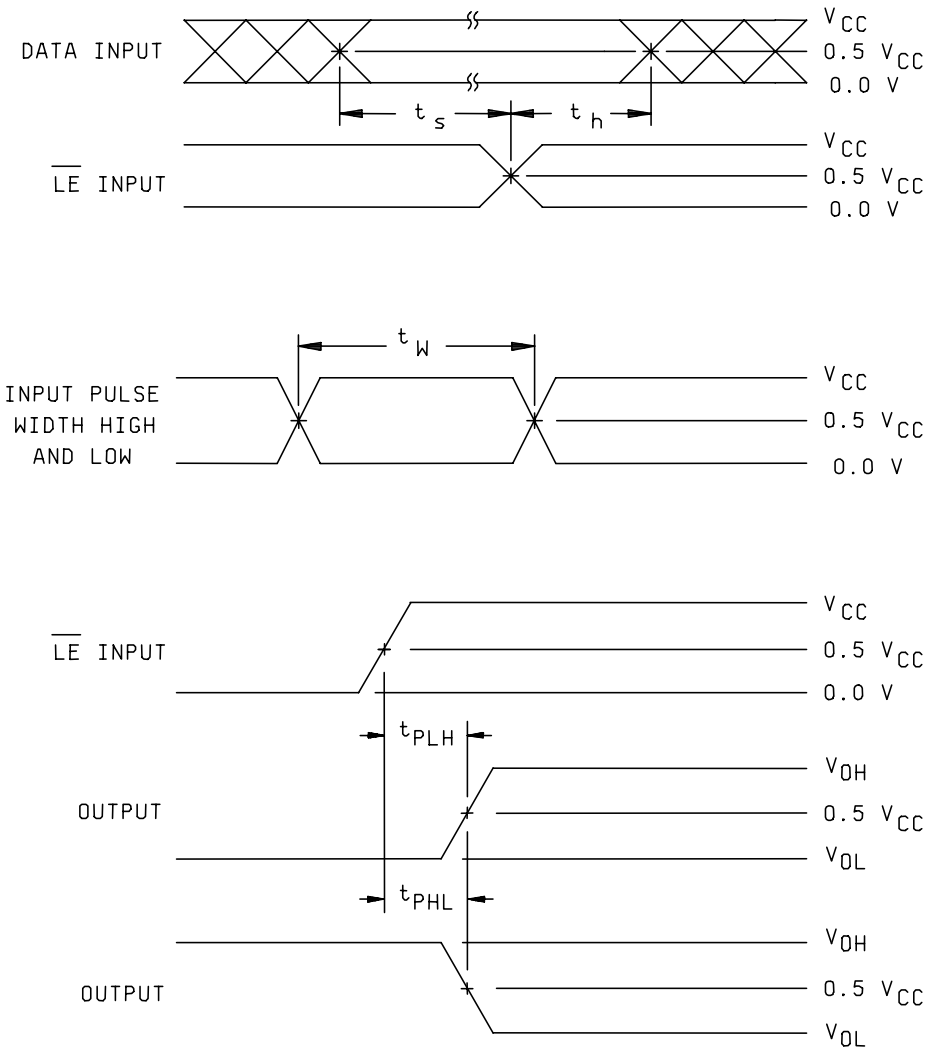
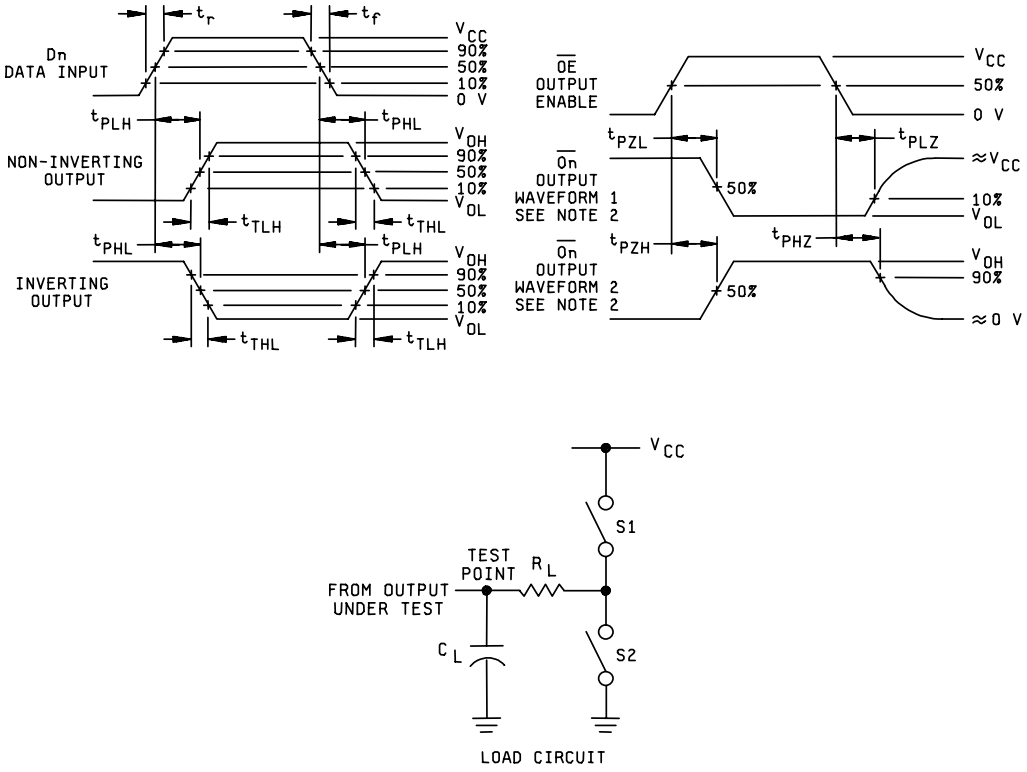


FIGURE 4. Switching waveforms and test circuit.



PARAMETER	R_L	C_L	S1	S2
t_{PZH}	1kΩ	50 pF	Open	Closed
t_{PZL}			Closed	Open
t_{PHZ}	1kΩ	50 pF	Open	Closed
t_{PLZ}			Closed	Open
t_{PLH},t_{PHL} or t_{THL},t_{TLH}	------	50 pF	Open	Open

NOTES:
1. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. R_L = 1 kΩ or equivalent.
4. Input signal from pulse generator: V_{IN} = 0.0 V to V_{CC}; PRR ≤ 1MHz; Z_O = 50Ω; t_r = 6.0 ns; t_f = 6.0 ns; t_r and t_f shall be measured from 0.1 V_{CC} to 0.9 V_{CC} and from 0.9 V_{CC} to 0.1 V_{CC}, respectively; duty cycle = 50 percent.
5. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
6. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit – Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroup 7 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, and D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1, 2, 9 1/
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 9, 10, 11 2/
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

1/ PDA applies to subgroup 1.
2/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 01-12-04

Approved sources of supply for SMD 5962-86062 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8606201RA	01295	CD54HC563F3A
5962-8606201SA	3/	SNJ54HC563W
5962-86062012A	3/	SNJ54HC563FK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: 6412 Highway 75 South Sherman, TX 75090-0084