

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add vendor CAGE 34333. Add vendor CAGE U4637. Editorial changes throughout.	87-04-16	M. A. Frye
B	Add device types 02, 03, and 04. Editorial changes throughout.	87-12-21	M. A. Frye
C	Change vendor CAGE 12969 to 48726. Change max duty cycle min limit. Add vendor CAGE U4637 for additional devices, also change name form Integrated Power to Seagate Microelectronics. Add vendor CAGE 34333 for additional devices. Add testing for delay to output, rise time, and fall time tests. Editorial changes throughout.	89-10-10	M. A. Frye
D	Add packages C, E, F, 2, H, and X. Changes unity gain bandwidth limit. Editorial changes throughout.	92-11-23	M. A. Frye
E	Add device types 05, 06, 07, and 08. Add vendor CAGE 48726 for device type 05, 06, 07, and 08. Changes to table I electricals. Delete vendor CAGE U4637 from drawing. Add vendor CAGE U3158. Editorial changes throughout.	93-09-10	M. A. Frye
F	Changes in accordance with NOR 5962-R146-94.	94-05-17	M. A. Frye
G	Changes in accordance with NOR 5962-R251-97.	97-03-19	M. A. Frye
H	Change vendor CAGE 48726 to 01295. Add class V for vendor CAGE 01295. . Editorial changes throughout. - lgt	00-11-08	R. Monnin
J	Correction to the V _{MIN} limit in table I for device types 03 and 06. Editorial changes throughout. - rrp	01-10-10	R. Monnin
K	Add case outline D. - ro	02-05-30	R. Monnin
L	For CAGE 01295 only, delete case outline 2 and substitute case outline X for device class V devices. - ro	03-12-19	R. Monnin

CURRENT CAGE CODE 67268

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

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REV STATUS	REV	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13						

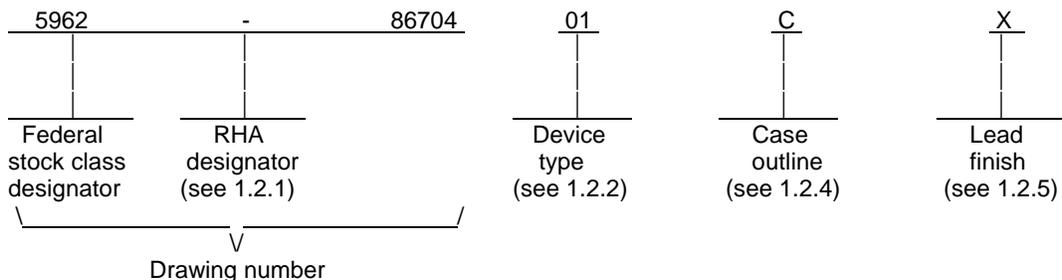
PMIC N/A	PREPARED BY DONALD R. OSBORNE	<p align="center">DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 http://www.dsc.dla.mil</p> <p align="center">MICROCIRCUIT, LINEAR, PROGRAMMABLE PRIMARY SIDE PULSE WIDTH MODULATOR, MONOLITHIC SILICON</p>																	
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY D. A. DICENZO																		
	APPROVED BY N. A. HAUCK																		
	DRAWING APPROVAL DATE 86-11-10																		
	REVISION LEVEL L	SIZE A	CAGE CODE 14933	5962-86704															
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1. SCOPE

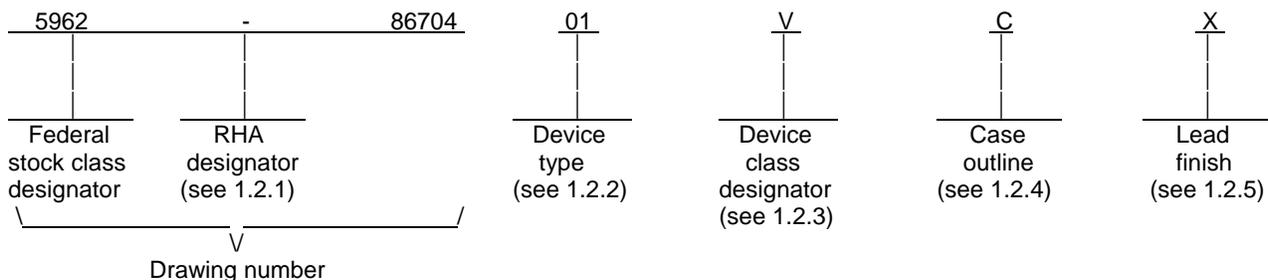
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	1842	Off-line current mode pulse width modulator controller
02	1843	Off-line current mode pulse width modulator controller
03	1844	Off-line current mode pulse width modulator controller
04	1845	Off-line current mode pulse width modulator controller
05	1842A	Off-line current mode pulse width modulator controller
06	1843A	Off-line current mode pulse width modulator controller
07	1844A	Off-line current mode pulse width modulator controller
08	1845A	Off-line current mode pulse width modulator controller

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1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
H	GDFP1-F10 or CDFP2-F10	10	Flat pack
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line
X	CQCC1-N20	20	Square leadless chip carrier (see figure 1)
2	CQCC1-N20	20	Square leadless chip carrier (see figure 1)

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage (V_{CC})	30 V
Output current	± 1.0 A
Output energy (capacitance load)	5.0 μ j
Analog input voltage (pins 2 and 3)	-0.3 V to +6.3 V
Error amplifier output sink current	10 mA
Power dissipation (P_D)($T_A = +25^\circ\text{C}$):	
Cases C, E, F, H, P, X, and 2	1.0 W 4/
Case D	700 mW 4/
Storage temperature range	-65°C to $+150^\circ\text{C}$
Lead temperature (soldering, 10 seconds)	$+300^\circ\text{C}$
Junction temperature (T_J)	$+150^\circ\text{C}$
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+15 V ± 5.0 percent
Ambient operating temperature range (T_A)	-55°C to $+125^\circ\text{C}$

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ All voltages are with respect to ground, and all currents are positive when flowing into the specified terminal.

3/ All references to pin numbers are for case outline P.

4/ Derate at 8.0 mW/ $^\circ\text{C}$ above $T_A = +25^\circ\text{C}$ for case P, 10 mW/ $^\circ\text{C}$ above $T_A = +50^\circ\text{C}$ for cases C and E, 5.5 mW/ $^\circ\text{C}$ above $T_A = +25^\circ\text{C}$ for case D, 8.7 mW/ $^\circ\text{C}$ above $T_A = +25^\circ\text{C}$ for case F, 9.0 mW/ $^\circ\text{C}$ above $T_A = +40^\circ\text{C}$ for cases 2 and X, and 6.9 mW/ $^\circ\text{C}$ above $T_A = +25^\circ\text{C}$ for case H.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

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3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 110 (see MIL-PRF-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
REFERENCE SECTION							
Reference output voltage	V _{REF}	I _O = 1.0 mA, T _J = +25°C	1	All	4.95	5.05	V
Line regulation	V _{RLINE}	12 V ≤ V _{IN} ≤ 25 V	1, 2, 3	All		20	mV
Load regulation	V _{RLOAD}	1.0 mA ≤ I _O ≤ 20 mA	1, 2, 3	All		25	mV
Total output variation		Line, load, and temperature <u>2/</u>	1, 2, 3	All	4.90	5.10	V
Long term stability <u>2/</u>		T _A = +125°C, 1000 hours, V _{REF}	2	All		25	mV
Output short-circuit current	I _{OS}		1, 2, 3	All	-30	-180	mA
OSCILLATOR SECTION							
Initial accuracy		T _J = +25°C <u>3/</u>	4	All	47	57	kHz
Voltage stability		12 V ≤ V _{CC} ≤ 25 V	4, 5, 6	All		1.0	%
Discharge current		V _{RT/CT} = 2 V Device types 05, 06, 07, and 08	1	All	7.8	8.8	mA
			2, 3		7.5	8.8	
ERROR AMP SECTION							
Input voltage	V _{IN}	V _{COMP} = 2.5 V	1, 2, 3	All	2.45	2.55	V
Input bias current	I _{IB}		1, 2, 3	All		-1.0	μA
Open loop voltage gain	A _{VOL}	2.0 V ≤ V _O ≤ 4.0 V	4, 5, 6	All	65		dB
Unity gain bandwidth	GBW	<u>2/</u>	4, 5, 6	All	0.55		MHz
Power supply rejection ratio	PSRR	12 V ≤ V _{CC} ≤ 25 V	4, 5, 6	All	60		dB
Output sink current	I _{SINK}	V _{VFB} = 2.7 V, V _{COMP} = 1.1 V	1, 2, 3	All	2.0		mA
Output source current	I _{SOURCE}	V _{VFB} = 2.3 V, V _{COMP} = 5.0 V	1, 2, 3	All	-0.5		mA
V _{OUT} high	V _{OH}	V _{VFB} = 2.3 V, R _L = 15 kΩ to ground	1, 2, 3	All	5.0		V
V _{OUT} low	V _{OL}	V _{VFB} = 2.7 V, R _L = 15 kΩ to V _{REF}	1, 2, 3	All		1.1	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CURRENT SENSE SECTION							
Gain	A	<u>4/</u> <u>5/</u>	4, 5, 6	All	2.85	3.15	V/V
Maximum input signal		V _{COMP} = 5.0 V <u>4/</u>	4, 5, 6	All	0.9	1.1	V
Input bias current	I _{IB}		1, 2, 3	All		-10	μA
Delay to output	T _D	V _{VFB} = 0 V, <u>2/</u> V _{ISENSE} = 2 V (step input)	9	All		300	ns
			10, 11			400	
OUTPUT SECTION							
Output low voltage	V _{OL}	I _{SINK} = 20 mA	1, 2, 3	All		0.4	V
					I _{SINK} = 200 mA		
Output high voltage	V _{OH}	I _{SOURCE} = 20 mA	1, 2, 3	All	13		V
					I _{SOURCE} = 200 mA	12	
Rise time	t _r	C _L = 1000 pF <u>2/</u>	9	All		150	ns
			10, 11			200	
Fall time	t _f	C _L = 1000 pF <u>2/</u>	9	All		150	ns
			10, 11			200	
UVLO saturation voltage	UVLOSAT	V _{CC} = 5 V, I _{SINK} = 10 mA, Device types 05, 06, 07, and 08.	1, 2, 3	All		1.2	V
UNDER-VOLTAGE LOCKOUT SECTION							
Start threshold	V _{TH}		1, 2, 3	01, 03 05, 07	15	17	V
				02, 04 06, 08	7.8	9.0	
Minimum operating voltage	V _{MIN}	After turn-on	1, 2, 3	01 05, 03	9.0	11	V
				06 07, 08	7.0	8.2	
				02, 04	7.0	8.3	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
PWM SECTION							
Maximum duty cycle	t _{ON} / t _{OSC} (max)		1, 2, 3	01, 02 05, 06	93	100	%
				03, 04 07, 08	46	50	
Minimum duty cycle	t _{ON} / t _{OSC} (min)		1, 2, 3	All		0	%
TOTAL STANDBY CURRENT							
Start-up current	I _{START}		1, 2, 3	All		1.0	mA
Operating supply current	I _{CC}	V _{VFB} = V _{ISENSE} = 0 V	1, 2, 3	All		17	mA

1/ T_A = T_J. Characteristics apply at V_{CC} = 15 V (adjust V_{CC} above the start threshold before setting at 15 V), R_T = 10 kΩ and C_T = 3.3 nF unless otherwise specified.

2/ These parameters are guaranteed if not tested.

3/ Output frequency equals oscillator frequency for device types 01, 02, 05, and 06. Output frequency is one half oscillator frequency for device types 03, 04, 07, and 08.

4/ Parameter measured at trip point of latch with V_{FB} = 0 V.

5/ Gain is defined as :

$$A = \frac{\Delta V_{COMP}}{\Delta V_{SENSE}} ; 0 V \leq V_{ISENSE} \leq 0.8 V$$

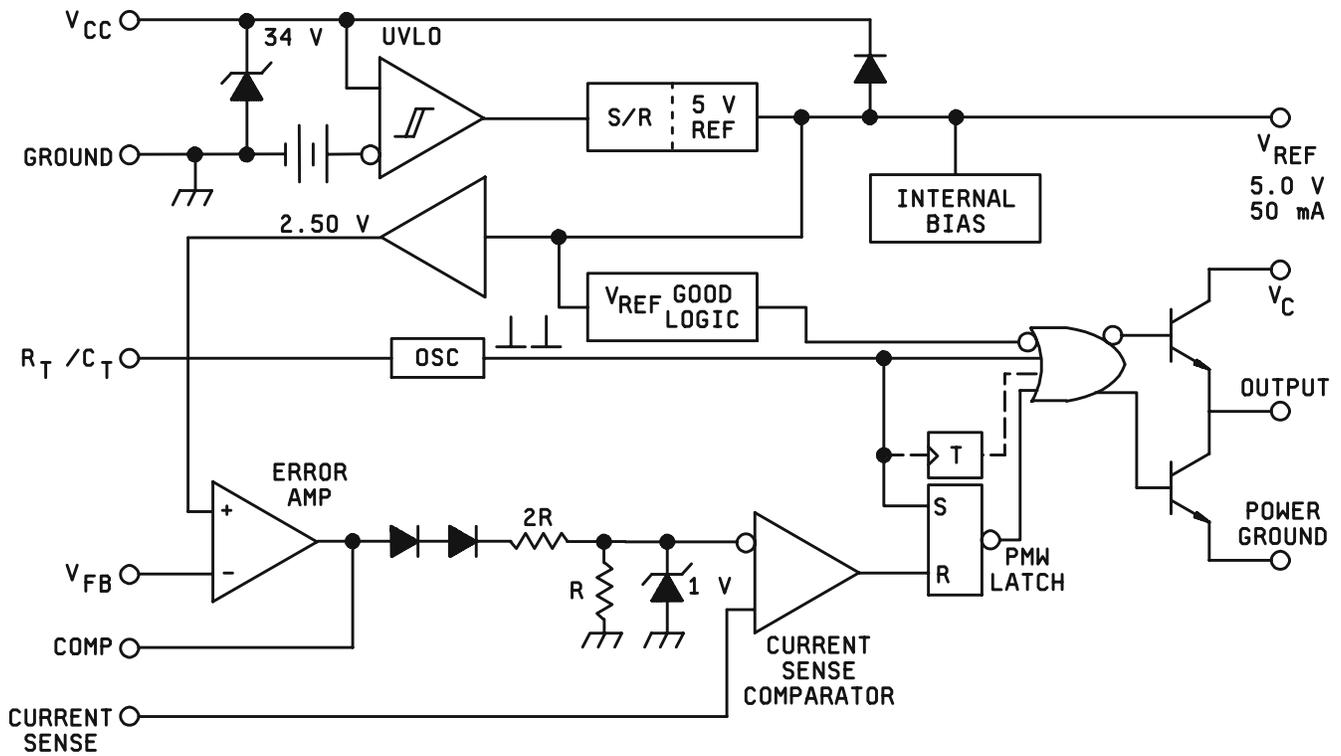
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Device types	All	All	All	01, 02	03, 04	All
Case outlines	C and D	H	P	2	2	X
Terminal number	Terminal symbol					
1	COMP	COMP	COMP	NC	NC	NC
2	NC	V _{FB}	V _{FB}	COMP	NC	COMP
3	V _{FB}	I _{SENSE}	I _{SENSE}	NC	COMP	NC
4	NC	R _T /C _T	R _T /C _T	NC	NC	NC
5	I _{SENSE}	POWER GND	GROUND	V _{FB}	V _{FB}	V _{FB}
6	NC	GROUND	OUTPUT	NC	NC	NC
7	R _T /C _T	OUTPUT	V _{CC}	I _{SENSE}	I _{SENSE}	I _{SENSE}
8	POWER GND	V _C	V _{REF}	NC	R _T /C _T	NC
9	GROUND	V _{CC}	---	NC	NC	NC
10	OUTPUT	V _{REF}	---	R _T /C _T	NC	R _T /C _T
11	V _C	---	---	NC	NC	NC
12	V _{CC}	---	---	GROUND	POWER GND	POWER GND
13	NC	---	---	NC	GROUND	GROUND
14	V _{REF}	---	---	NC	NC	NC
15	---	---	---	OUTPUT	OUTPUT	OUTPUT
16	---	---	---	NC	NC	NC
17	---	---	---	V _{CC}	V _C	V _C
18	---	---	---	NC	V _{CC}	V _{CC}
19	---	---	---	NC	NC	NC
20	---	---	---	V _{REF}	V _{REF}	V _{REF}

NOTE : Case outlines E and F are not available from an approved source.
NC = No connect.

FIGURE 1. Terminal connections.

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NOTE : Toggle flip flop used only in device types 03, 04, 07, and 08.

FIGURE 2. Logic diagram.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1, 2, 3, 4 <u>1/</u>	1, 2, 3, 4 <u>1/</u>	1, 2, 3, 4 <u>1/</u>
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 9, 10, 11 <u>2/</u>	1, 2, 3, 4, 5, 6, 9, 10, 11 <u>2/</u>	1, 2, 3, 4, 5, 6, 9, 10, 11 <u>2/</u>
Group C end-point electrical parameters (see 4.4)	1	1	1
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

2/ Subgroups 9, 10, and 11 are guaranteed if not tested to the limits specified in table I.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

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4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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Approved sources of supply for SMD 5962-86704 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-8670401CA	34333	SG1842J/883B
5962-8670401DA	01295	UC1842W/883B
5962-8670401EA	<u>3</u> /	SG1842J/883B
5962-8670401FA	<u>3</u> /	SG1842F/883B
5962-8670401HA	34333	SG1842F/883B
5962-8670401PA	01295	UC1842J/883B
	34333	SG1842Y/883B
	U3158	IP1842J/883B
5962-8670401XA	01295	UC1842L/883B
5962-86704012A	34333	SG1842L/883B
5962-8670401VPA	01295	UC1842JQMLV
5962-8670401VXA	01295	UC1842LQMLV
5962-8670401V2A	<u>3</u> /	UC1842LQMLV
5962-8670402CA	34333	SG1843J/883B
5962-8670402DA	01295	UC1843W/883B
5962-8670402EA	<u>3</u> /	SG1843J/883B
5962-8670402FA	<u>3</u> /	SG1843F/883B

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-8670402HA	34333	SG1843F/883B
5962-8670402PA	01295	UC1843J/883B
	34333	SG1843Y/883B
	U3158	IP1843J/883B
5962-8670402XA	01295	UC1843L/883B
5962-86704022A	34333	SG1843L/883B
5962-8670402VPA	01295	UC1843JQMLV
5962-8670402VXA	01295	UC1843LQMLV
5962-8670402V2A	<u>3</u> /	UC1843LQMLV
5962-8670403CA	34333	SG1844J/883B
5962-8670403DA	01295	UC1844W/883B
5962-8670403EA	<u>3</u> /	SG1844J/883B
5962-8670403FA	<u>3</u> /	SG1844F/883B
5962-8670403HA	34333	SG1844F/883B
5962-8670403PA	01295	UC1844J/883B
	34333	SG1844Y/883B
	U3158	IP1844J/883B
5962-8670403XA	01295	UC1844L/883B
5962-86704032A	34333	SG1844L/883B
5962-8670403VPA	01295	UC1844JQMLV
5962-8670403VXA	01295	UC1844LQMLV

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-8670403V2A	<u>3</u> /	UC1844LQMLV
5962-8670404CA	34333	SG1845J/883B
5962-8670404DA	01295	UC1845W/883B
5962-8670404EA	<u>3</u> /	SG1845J/883B
5962-8670404FA	<u>3</u> /	SG1845F/883B
5962-8670404HA	34333	SG1845F/883B
5962-8670404PA	01295	UC1845J/883B
	34333	SG1845Y/883B
	U3158	IP1845J/883B
5962-8670404XA	01295	UC1845L/883B
5962-86704042A	34333	SG1845L/883B
5962-8670404VPA	01295	UC1845JQMLV
5962-8670404VXA	01295	UC1845LQMLV
5962-8670404V2A	<u>3</u> /	UC1845LQMLV
5962-8670405PA	01295	UC1842AJ/883B
5962-8670405XA	01295	UC1842AL/883B
5962-8670405VPA	01295	UC1842AJQMLV
5962-8670405VXA	01295	UC1842ALQMLV
5962-8670405V2A	<u>3</u> /	UC1842ALQMLV

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8670406PA	01295	UC1843AJ/883B
5962-8670406XA	01295	UC1843AL/883B
5962-8670406VPA	01295	UC1843AJQMLV
5962-8670406VXA	01295	UC1843ALQMLV
5962-8670406V2A	<u>3/</u>	UC1843ALQMLV
5962-8670407PA	01295	UC1844AJ/883B
5962-8670407XA	01295	UC1844AL/883B
5962-8670407VPA	01295	UC1844AJQMLV
5962-8670407VXA	01295	UC1844ALQMLV
5962-8670407V2A	<u>3/</u>	UC1844ALQMLV
5962-8670408PA	01295	UC1845AJ/883B
5962-8670408XA	01295	UC1845AL/883B
5962-8670408VPA	01295	UC1845AJQMLV
5962-8670408VXA	01295	UC1845ALQMLV
5962-8670408V2A	<u>3/</u>	UC1845ALQMLV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

<u>Vendor CAGE number</u>	<u>Vendor name and address</u>
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-0084
34333	Microsemi Integrated Products 11861 Western Avenue Garden Grove, CA 92641-1816
U3158	Semelab PLC Coventry Road, Lutterworth, Leicestershire LE174JB United Kingdom

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