REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change vendor name of CAGE U4637. Make changes to 1.2.2, 3.3, 4.2, 4.3.1, 4.3.2. Editorial changes throughout. Make changes to table I.	89-06-15	M. A. FRYE
B	Changes in accordance with N.O.R. 5962-R145-95.	95-06-29	M. A. FRYE
C	Drawing updated to reflect current requirements. - ro	02-08-27	R. MONNIN

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
RICK OFFICER

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAY MONNIN

APPROVED BY
MICHAEL A. FRYE

DRAWING APPROVAL DATE
87-11-24

MICROCIRCUIT, LINEAR, REGULATING PULSE WIDTH MODULATOR, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
C	A	**67268**	**5962-87645**

SHEET 1 OF 12

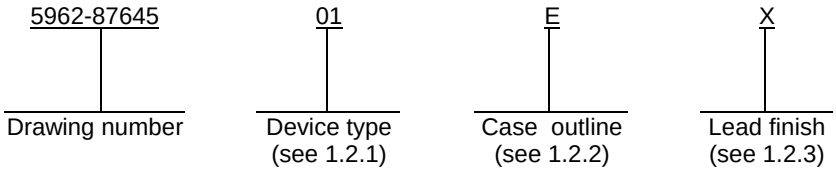
DSCC FORM 2233
APR 97

5962-E545-02

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	1524B	Regulating pulse width modulator
02	1524A	Regulating pulse width modulator

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Input voltage ($+V_{IN}$) ---------- +42 V dc
Collector voltage ---------- +60 V dc
Logic input range:
  Device type 01 ---------- -0.3 V dc to +5.5 V dc
  Device type 02 ---------- -0.3 V dc to +5.3 V dc
Current limit sense inputs ---------- -0.3 V dc to $+V_{IN}$
Output current (each transistor):
  Device type 01 ---------- 200 mA
  Device type 02 ---------- 250 mA
Reference load current ---------- 50 mA
Oscillator charging current ---------- 5 mA
Maximum power dissipation (P_D) ---------- 1,000 mW 1/
Lead temperature (soldering, 10 seconds) ---------- +300°C
Junction temperature (T_J) ---------- +150°C
Thermal resistance, junction-to-case (θ_{JC}) ---------- 60°C/W
Thermal resistance, junction-to-ambient (θ_{JA}) ---------- 100°C/W

1/ Must withstand the added P_D due to short-circuit test; e.g., I_{OS}.

1.4 Recommended operating conditions.

Input voltage range ($+V_{IN}$):
- Device type 01 ---------- +7 V dc to +40 V dc
- Device type 02 ---------- +8.5 V dc to +40 V dc

Collector voltage ---------- 0 V dc to +60 V dc

Error amp common mode range:
- Device type 01 ---------- +2.3 V dc to V_{REF}
- Device type 02 ---------- +1.5 V dc to +5.5 V dc

Current limit sense common mode range ---------- 0 V dc to V_{IN} -2.5 V dc

Output current range (each transistor):
- Device type 01 ---------- 0 mA to 100 mA
- Device type 02 ---------- 0 mA to 200 mA

Reference load current range ---------- 0 mA to 20 mA

Oscillator charging current range ---------- 25 μA to 1.8 mA

Oscillator frequency range:
- Device type 01 ---------- 100 Hz to 400 Hz
- Device type 02 ---------- 140 Hz to 480 kHz

Oscillator timing resistor range (R_T) ---------- 2 kΩ to 150 kΩ

Oscillator timing capacitor range (C_T):
- Device type 01 ---------- 1 nF to 0.1 μF
- Device type 02 ---------- 470 pF to 0.1 μF

Ambient operating temperature range (T_A) ---------- -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 -- Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 -- List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power consumption							
Standby current	I_{CC}	V_{IN} = 40 V, $V_{SHUTDOWN}$ = 2.0 V	1,2,3	01	3	12	mA
		V_{IN} = 8.5 V to 40 V, $V_{SHUTDOWN}$ = 2.0 V		02	3	10	
		V_{IN} = 6V				4	
Reference section							
Reference voltage out	V_{REF}		1	All	4.95	5.05	V
			2,3		4.90	5.10	
Line regulation	V_{RLINE}	V_{IN} = 7V to 40 V	1,2,3	01		20	mV
		V_{IN} = 8.5 V to 40 V		02		20	
Load regulation	V_{LOAD}	I_L = 0 mA to 20 mA	1,2,3	01		30	mV
				02		25	
Short-circuit current	I_{OS}	V_{REF} = 0 V	1,2,3	01	25	120	mA
				02		150	
Temperature stability	$\Delta V_{REF} / \Delta T$	I_L = 0 mA 3/	1,2,3	01		50	mV
Ripple rejection	$\Delta V_{IN} / \Delta V_{REF}$	f = 120 Hz	4	01	45		dB
				02	50		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Oscillator section							
Initial accuracy	F_{OSC}	OSCILLATOR OUTPUT pin is open	4	01	42	48	kHz
				02	41	45	
Temperature stability	Ftemp	OSCILLATOR OUTPUT pin is open	5,6	01	41.2	48.8	kHz
				02	40	46	
Voltage stability	Vstb	V_{IN} = 7 V to 40 V	4,5,6	01		1	%
		V_{IN} = 8.5 V to 40 V		02		1	
Clock pulse amplitude	V_{OSC}		4,5,6	All	3		V
Clock pulse width	t_{PW}		4,5,6	01	0.2	1.2	µs
				02	0.25	1.0	
Maximum oscillator frequency	Fmax	R_T = 2 kΩ, C_T = 470 pF, OSCILLATOR OUTPUT pin load at 2 kΩ and 10 pF	4,5,6	01	400		kHz
		R_T = 2 kΩ, C_T = 470 pF		02	480		
Minimum oscillator frequency	Fmin	R_T = 150 kΩ, C_T = 0.1 µF	1,2,3	02		140	Hz
Sawtooth peak voltage	Vsp	V_{IN} = 40 V	4,5,6	01	3.3	3.9	V
				02	3.3	3.9	
Sawtooth valley voltage	Vsv	V_{IN} = 40 V	4,5,6	01	0.6	1.2	V
				02	0.5	1.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Current limit comparator							
Sense voltage	V_{SENSE}	V_{CM} = 0 V	1,2,3	01	180	220	mV
			1	02	188	212	
			2,3		180	220	
Input bias current	I_{SENSE}		1,2,3	All		10	µA
Pulse width modulator comparator							
Minimum duty cycle outputs A, B	t_{on} / t_{OSC}	Vcomp = 0.5 V	4,5,6	All		0	%
Maximum duty cycle outputs A, B	t_{on} / t_{OSC}	Vcomp = 3.9 V	4,5,6	All	45		%
Error amplifier section							
Input offset voltage	V_{IO}	$R_S \le 2$ kΩ	1,2,3	All		5	mV
Input bias current	I_{IB}		1,2,3	All		5	µA
Input offset current	I_{IO}		1,2,3	All		1	µA
DC open loop gain	Avol	$R_L > 10$ MΩ	1,2,3	01	60		dB
		$R_L > 10$ MΩ, ΔV_{OUT} = 1 V to 4 V		02	68		
Output low level	V_{LO}	Isink = 100 µA, INV. INPUT – NONINV. INPUT > 150 mV	1,2,3	01		0.5	V
		Isink = 70 µA, INV. INPUT – NONINV. INPUT > 150 mV		02		0.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Error amplifier section							
Output high level	V_{HI}	Isource = 100 µA, INV. INPUT – NONINV. INPUT > 150 mV	1,2,3	01	3.8		V
		Isource = 70 µA, INV. INPUT – NONINV. INPUT > 150 mV		02	5.0		
Common mode rejection	CMRR	V_{CM} = 2.3 V to V_{REF}	1,2,3	01	70		dB
		V_{CM} = 1.5 V to 5.5 V		02	70		
Supply voltage rejection	PSRR	V_{IN} = 7 V to 40 V	1,2,3	01	76		dB
		V_{IN} = 8.5 V to 40 V		02	70		
Shutdown input							
High input voltage	V_{IH}		1,2,3	01	2		V
				02	1.2		
High input current	I_{IH}	$V_{SHUTDOWN}$ = +5.0 V	1,2,3	01		1	mA
		$V_{SHUTDOWN}$ = +2.5 V		02		3	
Low input voltage	V_{IL}		1,2,3	01		0.6	V
				02		0.4	
Under voltage lockout							
Threshold voltage	V_T	V_{IN} = V_{REF}	1,2,3	01	4.3	4.7	V
		Measured at V_{IN} at V_{CC} pin with V_{IN} rising and R_{REF} open		02	6.5	8.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output section							
Collector leakage current	I_{CEX}	V_{CE} = 60 V	1,2,3	All		50	µA
Collector saturation voltage	V_{CE} (sat)	I_C = 10 mA	1,2,3	01		0.4	V
		I_C = 100 mA				2.0	
		I_C = 20 mA		02		0.4	
		I_C = 200 mA				2.2	
Emitter output voltage	V_{EO}	I_E = 10 mA	1,2,3	All	17.5		V
		I_E = 100 mA			17		
Emitter voltage rise time	t_r	R_E = 2 kΩ	4,5,6	All		400	ns
Collector voltage fall time	t_f	R_C = 2 kΩ	4,5,6	All		200	ns

1/ For device 01: V_{IN} = 20 V, F_{OSC} = 45 kHz, R_T = 2700 Ω ±1 percent, C_T = 0.01 µF ±1 percent and over operation temperature, unless otherwise specified.

2/ For device 02: V_{IN} = 20 V, F_{OSC} = 43 kHz, R_T = 2700 Ω ±0.1 percent, C_T = 0.01 µF ±0.1 percent and over operation temperature, unless otherwise specified.

3/ Guaranteed, if not tested to the limits specified in table I herein.

Device type	01
Case outline	E
Terminal number	Terminal symbol
1	INVERTING INPUT
2	NONINVERTING INPUT
3	OSCILLATOR OUTPUT
4	+CL SENSE
5	-CL SENSE
6	R_T
7	C_T
8	GND
9	COMPENSATION
10	SHUTDOWN
11	EMITTER A
12	COLLECTOR A
13	COLLECTOR B
14	EMITTER B
15	V_{CC}
16	V_{REF}

FIGURE 1. Terminal connections.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,4
Group A test requirements (method 5005)	1,2,3,4,5,6
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-08-27

Approved sources of supply for SMD 5962-87645 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8764501EA	34333	SG1524BJ/883B
	U3158	IP1524BJ/883B
5962-8764502EA	01295	UC1524AJ/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493
34333	Microsemi Integrated Products 11861 Western Avenue Garden Grove, CA 92641-1816
U3158	Semelab PLC Coventry Road, Lutterworth Leicestershire LE174JB United Kingdom Point of contact: Martinez & Associates 234 Boston Post Road Wayland, MA 01778