

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical changes to table I. Editorial changes throughout.	1990 AUG 8	W. Heckman

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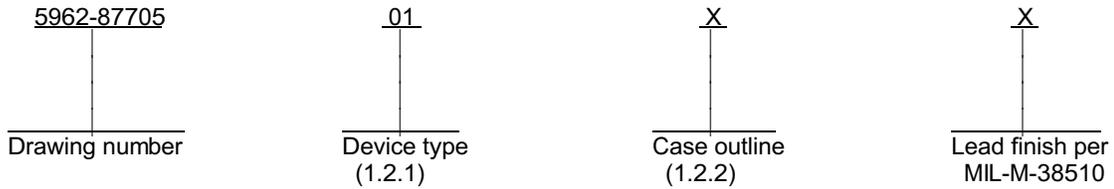
REV																			
SHEET																			
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29				
REV STATUS OF SHEETS				REV		A	A	A	A	A	A	A	A	A	A	A	A	A	A
				SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Jeffery Tunstall		DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444															
<p>STANDARDIZED MILITARY DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p>AMSC N/A</p>	CHECKED BY Tim H. Noh		MICROCIRCUIT, BIPOLAR, VMEbus CONTROLLER, MONOLITHIC SILICON															
	APPROVED BY William K. Heckman																	
	DRAWING APPROVAL DATE 26 AUGUST 1987		SIZE A	CAGE CODE 67268	5962-87705													
	REVISION LEVEL A		SHEET 1 OF 29															

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	68172	VMEbus controller (BUSCON)

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

<u>Outline letter</u>	<u>Case outline</u>
X	D-10 (28-lead 1.490" x .610" x .232") dual-in-line package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Storage temperature range	-65° C to +150° C
Maximum power dissipation (P_D) ^{1/}	1.4 W
Lead temperature (soldering, 5 seconds)	+300° C
Junction temperature (T_J)	+175° C
Thermal resistance, junction-to-case (θ_{JC})	20° C/W
Thermal resistance, junction-to-ambient (θ_{JA})	50° C/W

1.4 Recommended operating conditions.

Supply voltage:	
V_{CC}	4.75 V dc to 5.25 V dc
V_{SS}	0 V
High level input voltage (logic inputs) (V_{IH})	2.0 V to V_{CC}
Low level input voltage (logic inputs) (V_{IL})	GND to 0.8 V dc
Minimum high level output voltage	2.7 V dc
Maximum low level output voltage	0.5 V dc
Frequency of operation	25 MHz
Case operating temperature range (T_C)	-55° C to +125° C

^{1/} Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawing (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $\frac{1}{2}/\frac{3}{}$ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Group A subgroups	Limits		Unit
				Min	Max	
DSI, ONBD, SLVN, VMEN, LBRN, RELSE, RESETN Input low current Input high current Input low voltage Input high voltage	I_{IL} I_{IH} V_{IL} V_{IH}	$V_1 = 0.4\text{ V}$ $V_1 = 2.7\text{ V}$	1, 2, 3 1, 2, 3 1, 2, 3 1, 2, 3	2.0	-400 20 0.8	μA μA V V
ASN, MASN, BGINN, DTACKN, BERRN, LDTACKN, LBERRN Input low current Input high current Input low voltage Input high voltage	I_{IL} I_{IH} V_{IL} V_{IH}	$V_1 = 0.4\text{ V}$ $V_1 = 2.7\text{ V}$	1, 2, 3 1, 2, 3 1, 2, 3 1, 2, 3	2.0	-400 20 0.8	μA μA V V
R/WN, CLK Input low current Input high current Input low voltage Input high voltage	I_{IL} I_{IH} V_{IL} V_{IH}	$V_1 = 0.4\text{ V}$ $V_1 = 2.7\text{ V}$	1, 2, 3 1, 2, 3 1, 2, 3 1, 2, 3	2.0	-800 40 0.8	μA μA V V
BGOUTN, VMEENN, SLVSELN, DSENN, DENN, DDIR (low current totem pole) Output low voltage Output high voltage	V_{OL} V_{OH}	$I_{OL} = 8\text{ mA}, V_{CC} = 4.75\text{ V}$ $I_{OH} = -0.4\text{ mA}, V_{CC} = 4.75\text{ V}$	1, 2, 3 1, 2, 3	2.7	0.5	V V
MASTENN (high current totem pole) Output low voltage Output high voltage	V_{OL} V_{OH}	$I_{OL} = 24\text{ mA}, V_{CC} = 4.75\text{ V}$ $I_{OH} = -1.0\text{ mA}, V_{CC} = 4.75\text{ V}$	1, 2, 3 1, 2, 3	2.7	0.5	V V
MASN (low current three-state) Output low voltage Output high voltage	V_{OL} V_{OH}	$I_{OL} = 8\text{ mA}, V_{CC} = 4.75\text{ V}$ $I_{OH} = -0.4\text{ mA}, V_{CC} = 4.75\text{ V}$	1, 2, 3 1, 2, 3	2.7	0.5	V V
ASN (high current three-state) Output low voltage Output high voltage	V_{OL} V_{OH}	$I_{OL} = 48\text{ mA}, V_{CC} = 4.75\text{ V}$ $I_{OH} = -3.0\text{ mA}, V_{CC} = 4.75\text{ V}$	1, 2, 3 1, 2, 3	2.7	0.5	V V
LDTACKN, LBERRN, LBGN (low current open collector) Output low voltage Output leakage current	V_{OL} I_{OH}	$I_{OL} = 8\text{ mA}, V_{CC} = 4.75\text{ V}$ $V_{OUT} = 5.25\text{ V}$	1, 2, 3 1, 2, 3		0.6 100	V μA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C	Refer- ence no.	Group A subgroups	Limits		Unit
					Min	Max	
DTACKN, BERRN, BRN, BBSYN (high current open collector) Output low voltage	V _{OL}	I _{OL} = 48 mA V _{CC} = 4.75 V					V
Output leakage current	I _{OH}	V _{OUT} = 5.25 V					μA
V _{CC} supply current	I _{CC}	V _{CC} = 5.25 V					mA
Clock and general parameters							
CLK cycle time (clk)	t ₁	See figures 2 to 11, 13	1	9, 10, 11	40		ns
CLK low time (clk)	t ₂	See figures 2 to 11, 13	2	9, 10, 11	15		ns
CLK high time (clk)	t ₃	See figures 2 to 11, 13	3	9, 10, 11	15		ns
Asynchronous input setup time to clk high							
ASN, MASN low	t ₄	See figures 2 to 6, 11, 13 4/	4	9, 10, 11	30		ns
ASN, MASN high	t ₅	See figures 2 to 4, 6 4/	5	9, 10, 11	25		ns
SLVN, VMEN low	t ₆	See figures 2 to 6, 13 5/	6	9, 10, 11	20		ns
SLVN, VMEN high	t ₇	See figures 4, 10, 11 5/	7	9, 10, 11	33		ns
ONBD low	t ₈	See figures 2, 3, 6 5/	8	9, 10, 11	25		ns
ONBD high	t ₉	See figure 11 5/	9	9, 10, 11	20		ns
LBRN, RELSE, BGINN low	t ₁₀	See figures 6, 9, 13 4/	10	9, 10, 11	23		ns
LBRN, RELSE, BGINN high	t ₁₁	See figures 7, 8 4/	11	9, 10, 11	10		ns
DSI low (end of slave cycle)	t ₁₂	See figures 4, 5, 6 4/	12	9, 10, 11	30		ns
Asynchronous input hold time from clk high							
ASN, MASN, DSI	t ₁₃	6/		9, 10, 11	0		ns
ONBD, VMEN	t ₁₄	7/		9, 10, 11	0		ns
LBRN, RELSE, BGINN	t ₁₅	6/		9, 10, 11	2		ns
Propagation, clk high to:							
BGOUTN low	t ₁₆	See figure 9	16	9, 10, 11	20	55	ns
LBN low	t ₁₇	See figure 13	17	9, 10, 11	20	70	ns
LBN high	t ₁₈			9, 10, 11	11	46	ns
BBSYN, BRN low	t ₁₉	See figures 6, 9, 13	19	9, 10, 11	17	53	ns
BBSYN, BRN high	t ₂₀	See figures 6, 13	20	9, 10, 11	14	34	ns
ASN low	t ₂₁	See figures 2, 3, 6	21	9, 10, 11	12	41	ns
ASN high	t ₂₂	See figures 2, 3	22	9, 10, 11		40	ns
SLVSELN, VMEENN low	t ₂₃	See figures 4 to 6, 11, 13	23	9, 10, 11	14	60	ns
MASTENN low	t ₂₄	See figures 6, 11, 13	24	9, 10, 11	19	42	ns

See footnotes at end of table.

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		REVISION LEVEL A	SHEET 5

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $\frac{1}{2}/\frac{3}{-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}}$	Refer- ence no.	Group A subgroups	Limits		Unit
					Min	Max	
Miscellaneous RESETN width low	t_{25}	<u>8/</u>		9, 10, 11	6 clk		ns
BGINN high to BGOUTN high	t_{27}	See figure 9	27	9, 10, 11	5	17	ns
R/WN high to DSI high (start of read cycle)	t_{28}	See figures 2, 4 <u>9/</u>	28	9, 10, 11	10		ns
DSI low to RWN low (end of read cycle)	t_{29}	See figures 2, 5 <u>9/</u>	29	9, 10, 11	10		ns
Address decoding SLVN high after DTACKN low	t_{33}	See figure 10	33	9, 10, 11	22		ns
VMEN, ONBD valid after MASN high	t_{34}	See figures 2, 3 <u>9/</u>	34	9, 10, 11	10		ns
MASN high	t_{35}	See figures 2, 3 <u>10/</u>	35	9, 10, 11	15		ns
DSI low	t_{36}	See figures 2, 3, 4	36	9, 10, 11	20		ns
ASN high	t_{37}	See figure 4 <u>10/</u>	37	9, 10, 11	20		ns
VMEbus acquisition ASN low to BGINN low (early release by other master)	t_{38A}	See figures 6, 13 <u>9/</u>	38A	9, 10, 11	10		ns
BBSYN low to BRN high	t_{40}	See figures 6, 13	40	9, 10, 11		15	ns
ASN high to VMEENN low, DENN low (write)	t_{42}	See figure 6 <u>11/ 12/</u>	42	9, 10, 11	20	57	ns
BBSYN or BGOUTN low to BGINN high	t_{43A}	See figures 6, 9, 13 <u>9/</u>	43A	9, 10, 11	0		ns
VMEbus master cycles ASN low to DSEN low	t_{46}	See figures 2, 3 <u>13/ 14/</u>	46	9, 10, 11	-1	14	ns
R/WN low to DDIR high	t_{47}	See figures 3, 6	47	9, 10, 11		36	ns
DDIR high to DENN low (write)	t_{48}	See figures 3, 6 <u>15/</u>	48	9, 10, 11	2	11	ns
DTACKN and BERRN high to DENN low (write, 1st bus cycle or preceded by read)	t_{49}	See figure 3 <u>15/</u>	49	9, 10, 11	14	41	ns
DENN low to DSENN low (write)	t_{50}	See figure 3 <u>13/</u>	50	9, 10, 11	clk +13	2 clk +53	ns
R/WN high to DDIR low	t_{51}	See figures 2, 4, 6	51	9, 10, 11	13	40	ns
DDIR low to DENN low (read)	t_{52}	See figure 2 <u>16/</u>	52	9, 10, 11	7	26	ns
DSI high to DENN low (read)	t_{53}	See figure 2 <u>16/</u>	53	9, 10, 11	10	30	ns
DSI high to DSENN low (read)	t_{54}	See figure 2 <u>14/</u>	54	9, 10, 11	14	45	ns
DTACKN and BERRN high to DSENN low	t_{55}	See figures 2, 3 <u>13/ 14/</u>	55	9, 10, 11	15	51	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $\frac{1}{-55^{\circ}\text{C}} \leq T_C \leq \frac{3}{+125^{\circ}\text{C}}$	Refer- ence no.	Group A subgroups	Limits		Unit
					Min	Max	
VMEbus master cycles DTACKN or BERRN low to LDTACKN or LBERRN low	t ₅₆	See figures 2, 3	56	9, 10, 11		66	ns
LDTACKN or LBERRN low to DSI or MASN high	t ₅₇	See figures 2, 3 <u>9/</u>	57	9, 10, 11	0		ns
DSI low to DSENN high	t ₅₈	See figures 2, 3 <u>17/</u>	58	9, 10, 11		37	ns
MASN high to DSENN high	t ₅₉	See figures 2, 3 <u>17/</u>	59	9, 10, 11		50	ns
R/WN high to DSENN high (after a write)	t ₆₀	See figure 3 <u>18/</u>	60	9, 10, 11		32	ns
MASN high to DENN high (read)	t ₆₂	See figure 2 <u>19/</u>	62	9, 10, 11		50	ns
DSI low to DENN high (read)	t ₆₃	See figure 2 <u>19/</u>	63	9, 10, 11		39	ns
R/WN high to DENN high (write)	t ₆₄	See figure 3 <u>20/</u>	64	9, 10, 11		30	ns
DSENN high to LDTACKN and LBERRN high	t ₆₅	See figures 2, 3 <u>21/</u>	65	9, 10, 11		54	ns
DTACKN and BERRN high to LDTACKN and LBERRN high	t ₆₆	See figures 2, 3 <u>21/</u>	66	9, 10, 11		17	ns
VMEbus release BBSYN low	t ₆₇	See figure 7 <u>9/</u>	67	9, 10, 11	2 clk		ns
MASN high to VMEENN high or DENN high (early release, write DENN (write) and VMEENN high to ASN high (early release)	t ₇₁ t ₇₃	See figure 7	71	9, 10, 11	7	46	ns
ASN high to ASN released (early release)	t ₇₄	See figure 7	74	9, 10, 11	6	52	ns
DENN (write) and VMEENN high to BBSYN high (intercycle release)	t ₇₆	See figure 8	76	9, 10, 11	0	19	ns
BBSYN high to RELSE low	t ₇₇	See figures 7, 8 <u>9/</u>	77	9, 10, 11	0		ns
Master to slave switching Clock high to MSTEEN high (clock at which (external) ASN is detected low)	t ₇₈	See figures 4, 6, 13 <u>22/</u>	78	9, 10, 11	13	30	ns
SLVN low to MASTENN high	t ₇₉	See figures 4, 6, 13 <u>22/</u>	79	9, 10, 11		18	ns
SLVSELN high to MASTENN high	t ₈₀	See figure 4 <u>22/</u>	80	9, 10, 11	18	35	ns
VMEENN low to DDIR change	t _{81A}	See figures 4, 6	81A	9, 10, 11	-1	16	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C	Refer- ence no.	Group A subgroups	Limits		Unit
					Min	Max	
VMEbus slave cycles							
R/WN low to DDIR low	t ₈₅	See figures 5, 6	85	9, 10, 11	16	45	ns
DDIR low to DENN low (write)	t ₈₆	See figures 5, 6 <u>23/</u>	86	9, 10, 11	7	25	ns
LDTACKN and LBERRN high to DENN low (write)	t ₈₇	See figure 5 <u>23/</u>	87	9, 10, 11	10	35	ns
R/WN high to DDIR high	t ₈₈	See figures 5, 6	88	9, 10, 11		17	ns
DDIR high to DENN low (read)	t ₈₉	See figure 4 <u>24/</u>	89	9, 10, 11	4	12	ns
DSI high to DENN low (read)	t ₉₁	See figure 4 <u>24/</u>	91	9, 10, 11		29	ns
SLVSELN low and DSI high to LDTACKN or LBERRN low	t ₉₂	See figures 4, 5, 6, 11 <u>9/ 25/</u>	92	9, 10, 11	0		ns
LDTACKN or LBERRN low to DTACKN or BERRN low	t ₉₃	See figures 4, 5, 6, 11	93	9, 10, 11		48	ns
LDTACKN or LBERRN low to DENN high (write)	t ₉₄	See figures 5, 6,	94	9, 10, 11	10	27	ns
DTACKN or BERRN low to DSI low or ASN high	t _{94A}	See figures 4, 5, 6, 11 <u>9/</u>	94A	9, 10, 11	0		ns
DSI low to DENN high (read)	t ₉₅	See figure 4	95	9, 10, 11		22	ns
ASN high to SLVSELN high	t ₉₆	See figures 4, 5, 11, 13	96	9, 10, 11	14	35	ns
DSI low to DTACKN and BERRN high	t ₉₇	See figures 4, 5, 6	97	9, 10, 11	14	32	ns
DENN high to DTACKN and BERRN high	t _{97A}	See figure 4	97A	9, 10, 11	0	20	ns
DSI low to LDTACKN and LBERRN high	t ₉₈	See figures 4, 5, 6, 13 <u>9/ 26/ 27/</u>	98	9, 10, 11	0	35	ns
LDTACKN and LBERRN high to (next) DSI high	t ₉₉	See figures 4, 5 <u>9/ 26/</u>	99	9, 10, 11	0		ns
VMEbus slave cycles							
Clock high to VMEENN, DENN VMEbus slave write high (clock which MASN is detected low)	t ₁₀₀	See figure 11 <u>28/</u>	100	9, 10, 11		clk +40	ns
ONBD high to VMEENN, DENN (VMEbus slave write) high	t ₁₀₁	See figure 11 <u>28/</u>	101	9, 10, 11	10	40	ns
VMEN low to VMEENN, DENN (VMEbus slave write) high	t ₁₀₂	<u>28/</u>		9, 10, 11	9	26	ns
SLVSELN high to VMEENN, DENN (VMEbus slave write) high	t ₁₀₃	See figures 6, 11, 13 <u>28/</u>	103	9, 10, 11	0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C	Refer- ence no.	Group A subgroups	Limits		Unit
					Min	Max	
VMEbus slave cycles Clock high to VMEENN, DENN (VMEbus slave write) high (clock at which DSI (selected) is detected low	t ₁₀₄	See figures 6, 13 <u>28/</u>	104	9, 10, 11	10	40	ns
Onboard cycles MASN high to SLVSELN high	t ₁₁₁	See figure 11	111	9, 10, 11	10	40	ns
DMAC-type operation Clock high to MASN active (clock from which BBSYN is driven high)	t ₁₁₂	See figure 12 <u>29/</u>	112	9, 10, 11	22	60	ns
ASN high to MASN active	t ₁₁₃	See figure 12 <u>29/</u>	113	9, 10, 11		20	ns
ASN low to MASN low	t ₁₁₄	See figure 12	114	9, 10, 11	20	49	ns
ASN high to MASN high	t ₁₁₅	See figure 12	115	9, 10, 11	5	25	ns
ASN high to MASN released	t ₁₁₆	See figure 12 <u>30/</u>	116	9, 10, 11		48	ns
LBN low to MASN released	t ₁₁₇	See figure 12 <u>30/</u>	117	9, 10, 11		50	ns
LBN low to LBRN high	t ₁₂₂	See figure 13 <u>9/</u>	122	9, 10, 11	0		ns

The following parameters have been derived directly from ac electrical characteristics, and are guaranteed but not tested separately.

BGINN low to BGOUTN low	t ₂₆	See figure 9	26	9, 10, 11	clk +18	2 clk +78	ns
Address decoding ASN low to SLVN valid	t ₃₀	See figures 4, 5, 6, 13 <u>31/</u>	30	9, 10, 11		clk -30	ns
MASN low to VMEN valid	t ₃₁	See figures 2, 3, 6, 11 <u>31/</u>	31	9, 10, 11		clk -30	ns
MASN low to ONBD valid	t ₃₂	See figures 2, 3, 6, 11 <u>31/</u>	32	9, 10, 11		clk -22	ns
VMEbus acquisition MASN low to BRN low	t ₃₈	See figure 6 <u>32/</u>	38	9, 10, 11	clk +20	2 clk +83	ns
BGINN low to BBSYN low	t ₃₉	See figures 6, 13	39	9, 10, 11	clk +15	2 clk +76	ns
BGINN low to VMEENN low, DENN low (write)	t ₄₁	See figure 6 <u>11/</u>	41	9, 10, 11	clk +3	2 clk +38	ns
BGINN low to DENN low (read)	t _{41A}	See figure 6 <u>16/</u>	41A	9, 10, 11	clk +5	2 clk +60	ns
VMEENN low to ASN low	t ₄₃	See figure 6 <u>33/</u>	43	9, 10, 11	clk -11	2 clk	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C	Refer- ence no.	Group A subgroups	Limits		Unit
					Min	Max	
The following parameters have been derived directly from ac electrical characteristics, and are guaranteed but not tested separately.							
VMEbus master cycles ASN high (successive VMEbus master cycles)	t ₄₄	See figures 2, 3 <u>33/</u>	44	9, 10, 11	2 clk		ns
MASN low to ASN low (subsequent cycle retaining VMEbus control)	t ₄₅	See figures 2, 3 <u>33/</u>	45	9, 10, 11	clk +18	2 clk +70	ns
MASN low to DENN low (read)	t _{53A}	See figure 2 <u>16/</u>	53A	9, 10, 11	clk +5	2 clk +60	ns
MASN high to ASN high (unless early release)	t ₆₁	See figures 2, 3	61	9, 10, 11	clk +8	2 clk +75	ns
VMEbus release BGINN high to BBSYN high	t ₆₈	See figures 7, 8 <u>21/</u>	68	9, 10, 11	clk +12	2 clk +35	ns
RELSE high to BBSYN high	t ₆₉	See figures 7, 8 <u>34/</u>	69	9, 10, 11	clk +12	2 clk +42	ns
ASN low to BBSYN high (early release)	t ₇₀	See figure 7	70	9, 10, 11	clk -8		ns
ASN high to BBSYN high (intercycle release)	t ₇₅	See figure 8	75	9, 10, 11	clk -6		ns
Master to slave switching MASTENN high to VMENN low	t ₈₁	See figures 4, 13	81	9, 10, 11	8	clk +13	ns
VMEENN low to SLVSELN low	t ₈₂	See figures 4, 6, 13 <u>35/</u>	82	9, 10, 11	clk -20	clk	ns
VME slave cycles SLVSELN high (successive slave cycles)	t ₈₃	See figure 5 <u>35/</u>	83	9, 10, 11	3 clk +56		ns
ASN low to SLVSELN low (already in slave state)	t ₈₄	See figure 5 <u>35/</u>	84	9, 10, 11	clk +13	2 clk +74	ns
ASN low to DENN low (read)	t ₉₀	See figure 4 <u>24/</u>	90	9, 10, 11	clk +22	2 clk +80	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

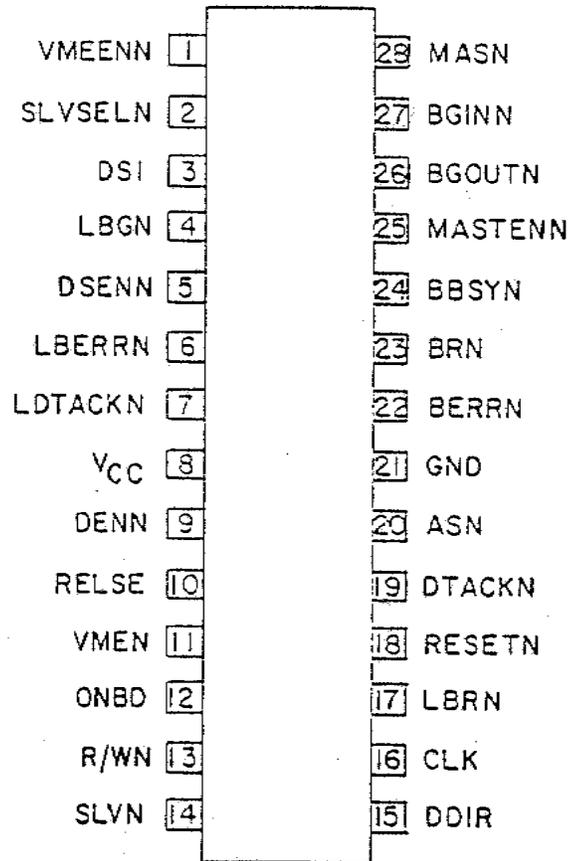
Test	Symbol	Conditions ^{1/ 2/ 3/} -55° C ≤ T _C ≤ +125° C	Refer- ence no.	Group A subgroups	Limits		Unit
					Min	Max	
The following parameters have been derived directly from ac electrical characteristics, and are guaranteed but not tested separately.							
Slave to master switching VMEENN high to MASTENN low	t ₁₀₅	See figures 6, 11, 13	105	9, 10, 11	-17		ns
MASTENN low to VMEENN low, DENN low (write, if next cycle on VMEbus)	t ₁₀₇	See figures 6, 13 ^{11/ 15/}	107	9, 10, 11	-24		ns
MASTENN low to DENN (read, next cycle on VMEbus)	t _{107A}	See figure 6 ^{16/}	107A	9, 10, 11	-5	20	ns
MASTENN low to SLVSELN low (if next cycle on board)	t ₁₀₈	See figure 11 ^{36/}	108	9, 10, 11	clk -28	clk +17	ns
Onboard cycles SLVSELN high (successive onboard cycles)	t ₁₀₉	See figure 11 ^{36/}	109	9, 10, 11	3 clk +22		ns
MASN low to SLVSELN low (MASTENN already low)	t ₁₁₀	See figure 11 ^{36/}	110	9, 10, 11	clk +11	2 clk +63	ns
DMAC-type operations LBRN low to BRN low (if BBSYN released)	t ₁₁₈	See figure 13	118	9, 10, 11	clk +15	2 clk +76	ns
LBRN low to LBGN low	t ₁₁₉	^{37/}		9, 10, 11	clk +18	2 clk +69	ns
BGINN low to LBGN low (ASN high) (ASN low)	t ₁₂₀	See figure 13	120	9, 10, 11	clk +18	2 clk +69	ns
MASN low (output) to LBGN low	t ₁₂₁	See figure 13	121	9, 10, 11	2 clk +18	3 clk +69	ns
LBRN high to LBGN high	t ₁₂₃	See figure 13 ^{38/}	123	9, 10, 11	clk +38	2 clk +69	ns
LBRN high to BBSYN high	t ₁₂₄	See figures 7, 8 ^{33/}	124	9, 10, 11	clk +10	2 clk +56	ns
ASN high to LBGN high (selected)	t ₁₂₅	See figures 13 ^{38/}	125	9, 10, 11	clk +12	2 clk +71	ns
DSI low to LBGN high (selected)	t ₁₂₆	See figures 13 ^{38/}	126	9, 10, 11	2 clk +15	3 clk +76	ns

- 1/ For operating at elevated temperatures, the device must be derated based on +175° C maximum junction temperature.
2/ Parameters are valid over specified temperature range.
3/ All voltage measurements are referenced to ground (V_{SS}). For testing, all signals swing between 0.4 V and 2.4 V with a transition time of 10 ns maximum. All time measurements are referenced at input voltages of 1.5 V.
4/ These setup times guarantee recognition at a rising edge of CLK, but the device will operate correctly if they are not met. If the asynchronous input is changed between the setup and hold times, the new state of the input may be recognized at this clock or the following clock.

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- 5/ These setup times are required on the rising edge of CLK following the one on which ASN or MASN is first recognized low. If parameters 30, 31, and 32 are met, these parameters are automatically guaranteed.
- 6/ These hold times guarantee (continued) recognition of the signal state at a rising edge of CLK, but the device will operate correctly if they are not met.
- 7/ These hold times are required on the rising edge of CLK preceding the one on which MASN is first recognized high. Parameter 34 provides a more straightforward requirement which guarantees these times.
- 8/ This parameter applies after V_{CC} and the clock signal are both within the specified limits.
- 9/ Guaranteed if not tested.
- 10/ These minimum times are to guarantee recognition.
- 11/ VMEENN is driven low only when 41, 42, and 107 have been met.
- 12/ Applies to ASN of VMEbus cycle which does not select this board as a slave.
- 13/ In a write operation, DSENN goes low when 46, 50, and 55 are met. Fifty-five is significant only for subsequent cycles in a series of writes with R/WN held low throughout.
- 14/ In a read operation, DSENN goes low when 46, 54, and 55 are met.
- 15/ In a write operation, DENN goes low when 41, 42, 48, 49, and 107 are met. Forty-nine does not apply for subsequent cycles in a series of writes if R/WN is held low throughout.
- 16/ In a read operation, DENN goes low when 52 and 53 are met.
- 17/ DSENN goes high when either 58 or 59 is met.
- 18/ Applies only if R/WN remains low after a write cycle, so that DSENN goes low again.
- 19/ In a read operation, DENN goes high when either 63 or 64 is met.
- 20/ In a write operation, DENN goes high when either 64 or 71 is met.
- 21/ LDTACKN and LBERRN go high when either 65 or 66 is met.
- 22/ MASTENN goes high when 78, 79, and 80 are all met.
- 23/ In a write operation, DENN goes low when 86 and 87 are met.
- 24/ In a read operation, DENN goes low when 89, 90, and 91 are met.
- 25/ The onboard slave(s) should wait for both SLVSELN and DSI before driving a response.
- 26/ Since BUSCON itself terminates DTACKN and BERRN when DSI goes low, the onboard slaves must meet this requirement to assure that a "lingering" LDTACKN or LBERRN is not presented as DTACKN or BERRN when the next DSI occurs. Ninety-nine is the real requirement. Ninety-eight maximum is derived from it, plus the 40 ns minimum high time of VMEbus data strobes and an allowance for receiver skew.
- 27/ The onboard slave(s) must meet this requirement so that the local response is not inadvertently presented to the onboard master.
- 28/ VMEENN goes high only when 100, (101 or 102), 103, and 104 are met. One hundred and four applies only if VMEbus slave cycle (with this board) is ending.
- 29/ MASN is driven out of Hi-Z state only when 112 and 113 are met.
- 30/ MASN is released to Hi-Z state only when 116 and 117 are met.
- 31/ These parameters guarantee parameters 6 through 10, but are not absolute requirements. If these parameters are not met, parameters 6 through 10, and 14 must be met for each clock edge from the one following the edge on which MASN or ASN is recognized low, until MASN or ASN goes high.
- 32/ BRN is driven low, and this acquisition sequence applies, only if BBSYN is high.
- 33/ ASN goes low when 43, 44, and 45 are met, 44 is not applicable on the first cycle after acquiring the VMEbus.
- 34/ BBSYN is always released in response to BGINN, RELSE, and LBRN all high. However, if this condition is detected during a clock period in which the decision to change ASN is made, the release of BBSYN is delayed one clock period so that 70 or 75 is met.
- 35/ SLVSELN goes low when 82, 83, and 84 (as applicable) are met.
- 36/ SLVSELN goes low when 108, 109, and 110 (as applicable) are met.
- 37/ The max figure applies only if BUSCON has kept VMEbus control (i.e., if BBSYN is low).
- 38/ LBGN goes high only when 123, 125, and 126 are met, but 125 and 126 apply only if a VMEbus slave cycle (with this board) is in progress.

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TOP VIEW

FIGURE 1. Terminal connections.

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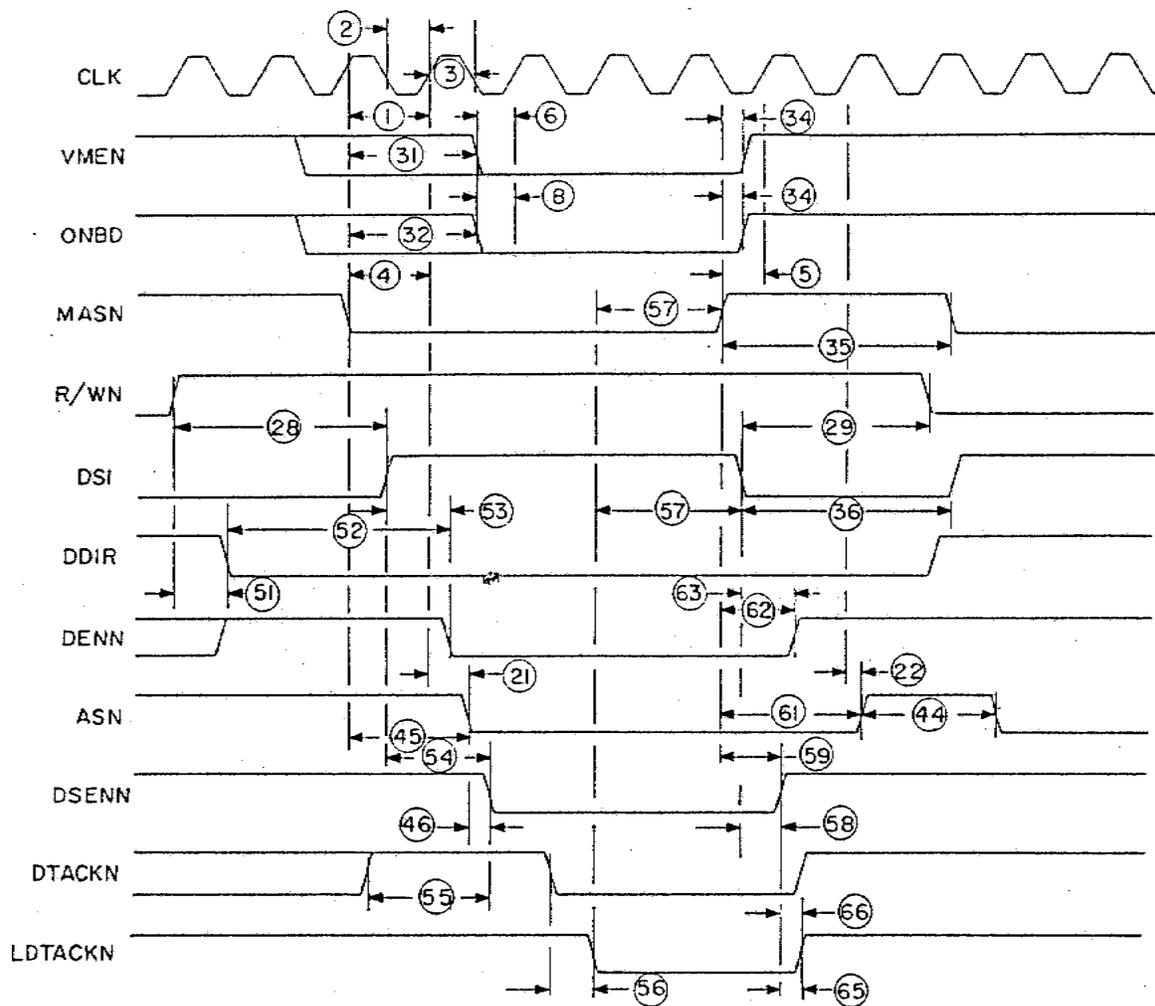


FIGURE 2. Switching waveform (read cycle from on board master to VMEbus slave-already in control of VMEbus).

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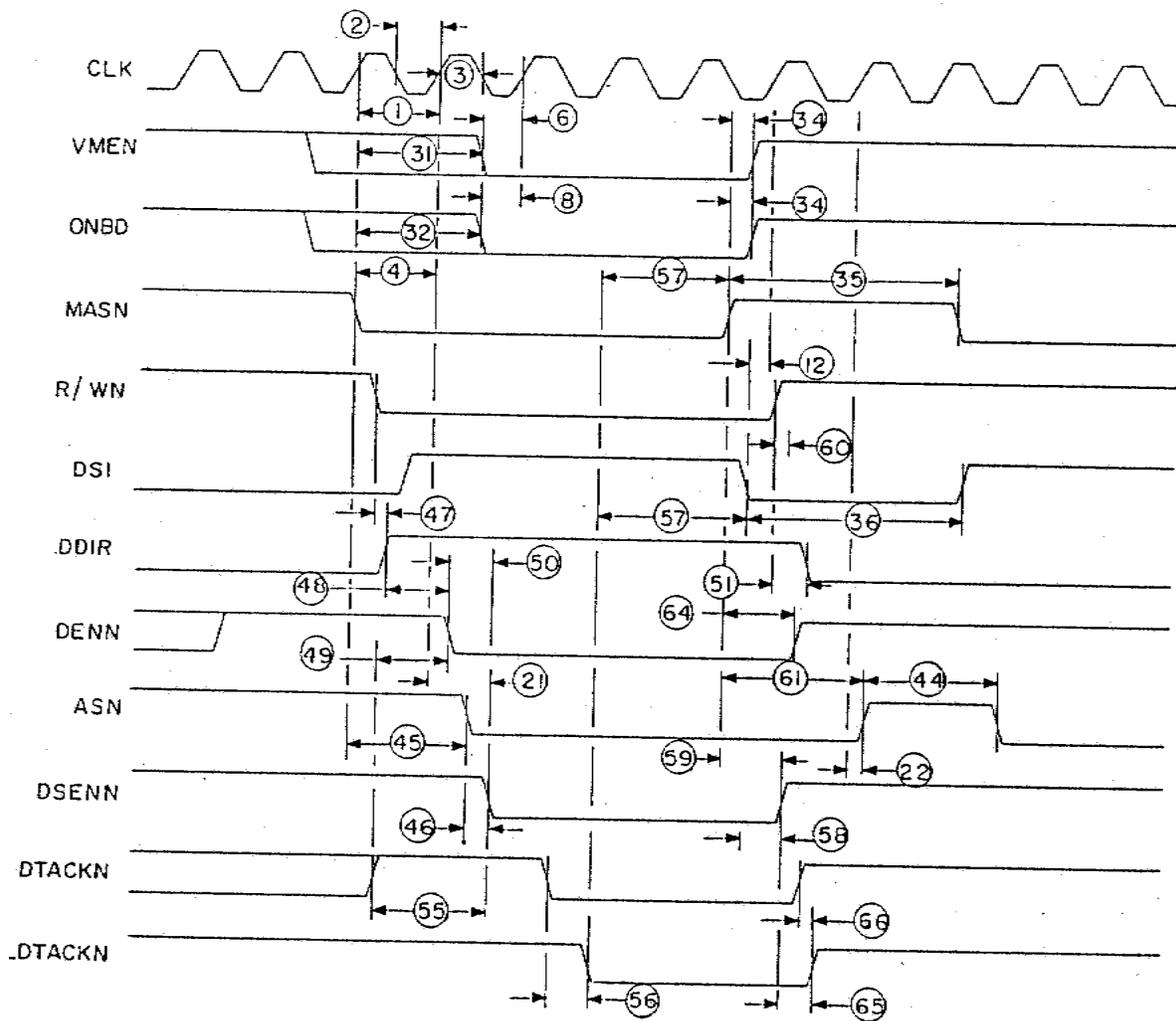


FIGURE 3. Switching waveform (write cycle from on board master to VMEbus slave-already in control of VMEbus).

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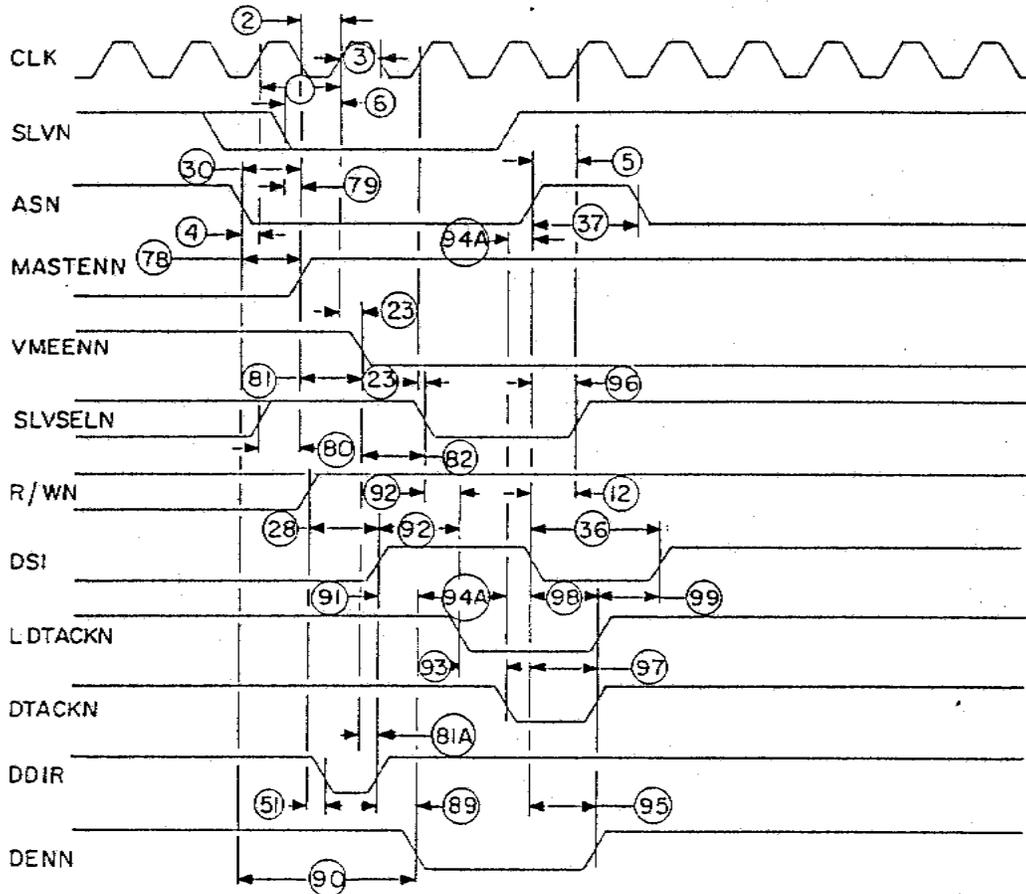


FIGURE 4. Switching waveforms (slave read cycle-starting in master mode).

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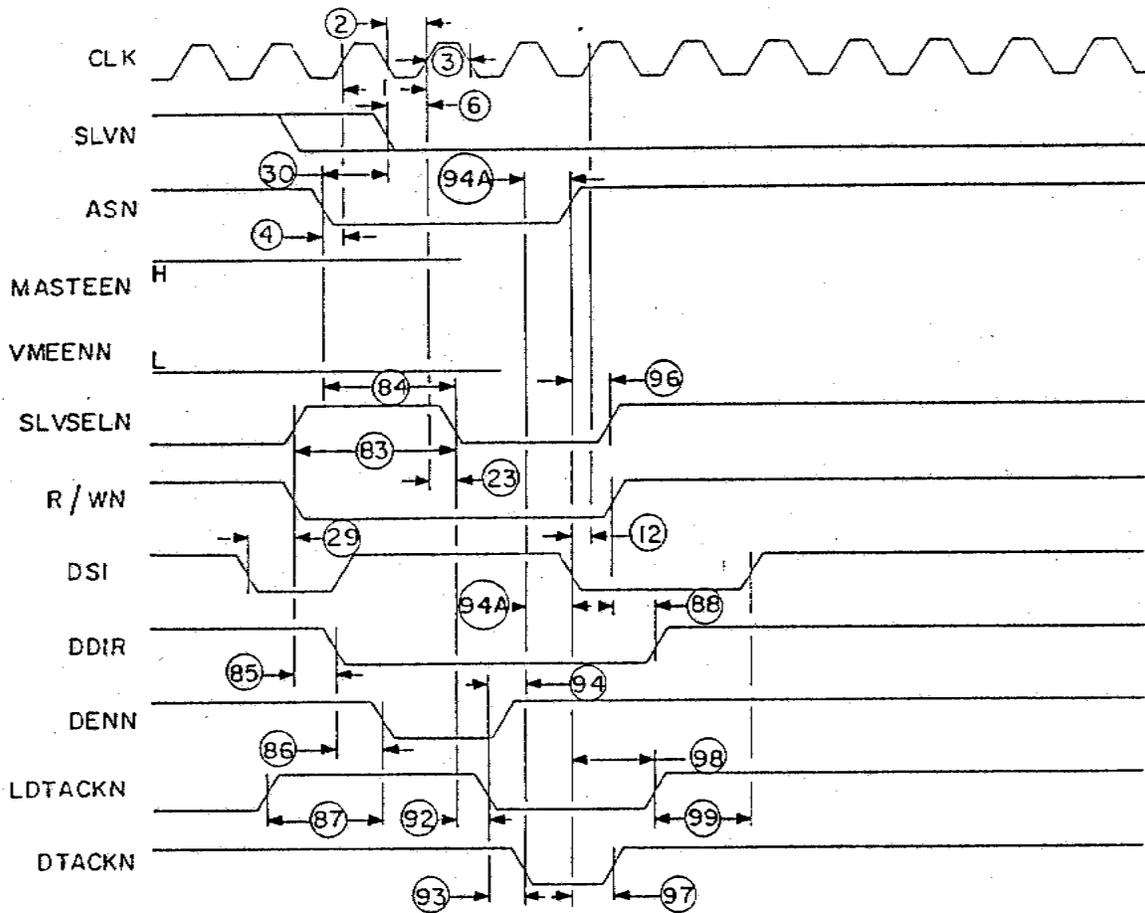


FIGURE 5. Switching waveforms (slave write cycle-starting in slave mode).

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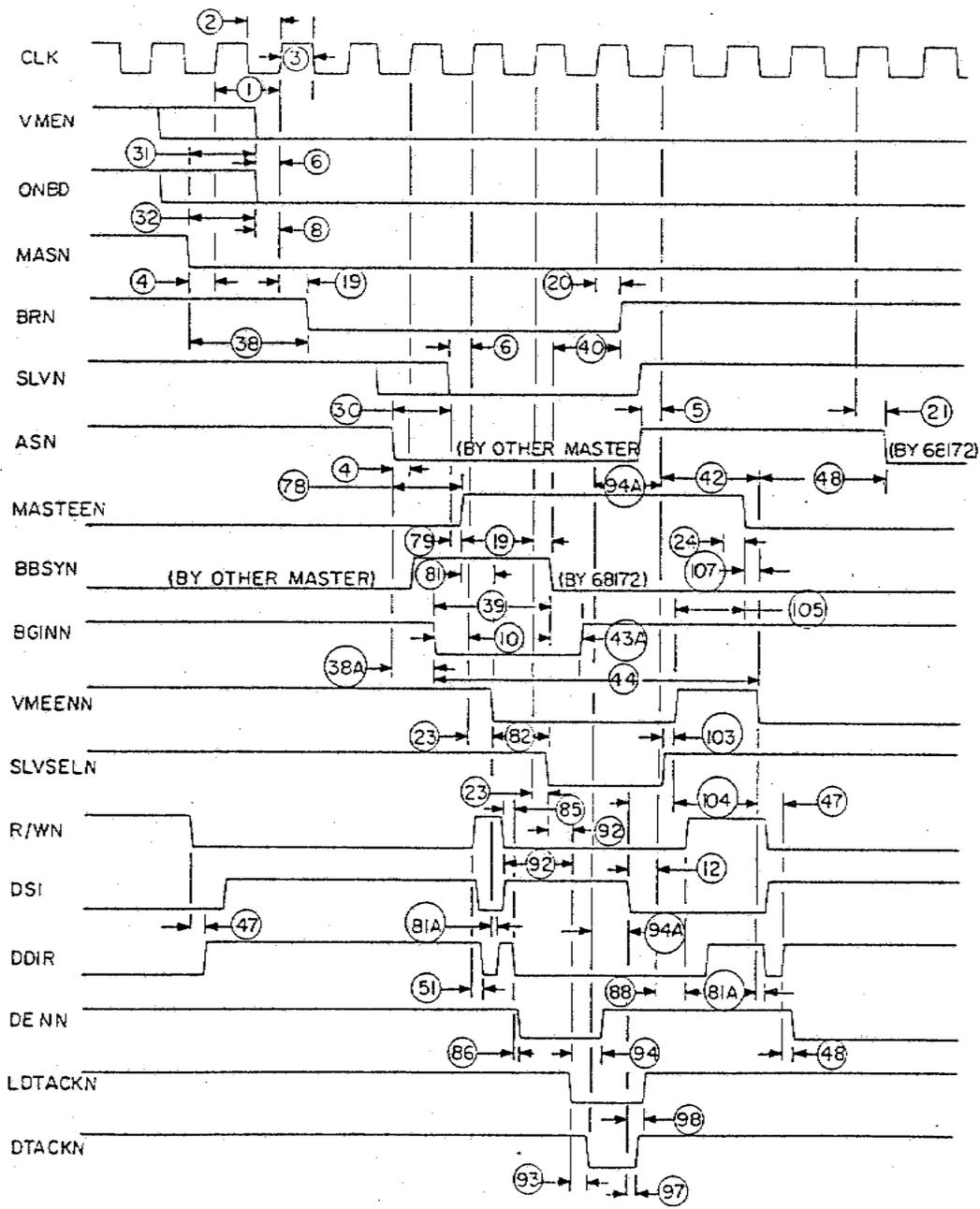


FIGURE 6. Switching waveforms (VMEbus acquisition, including slavewrite cycle).

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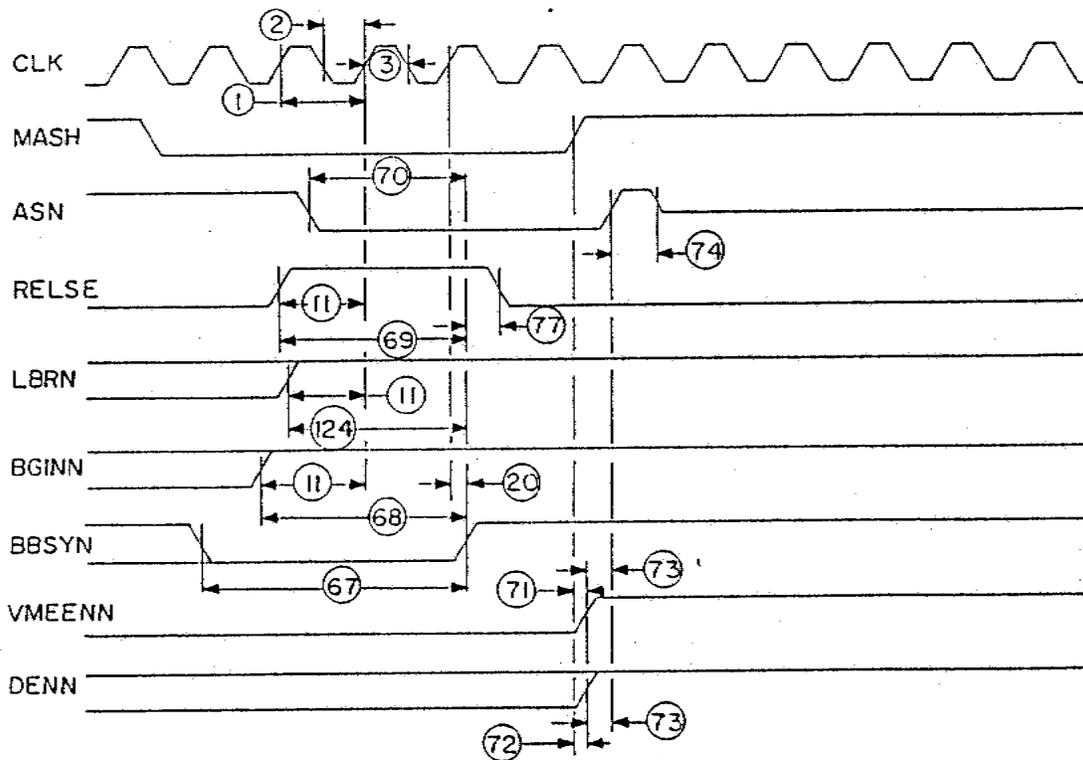


FIGURE 7. Switching waveforms ("early" VMEbus release).

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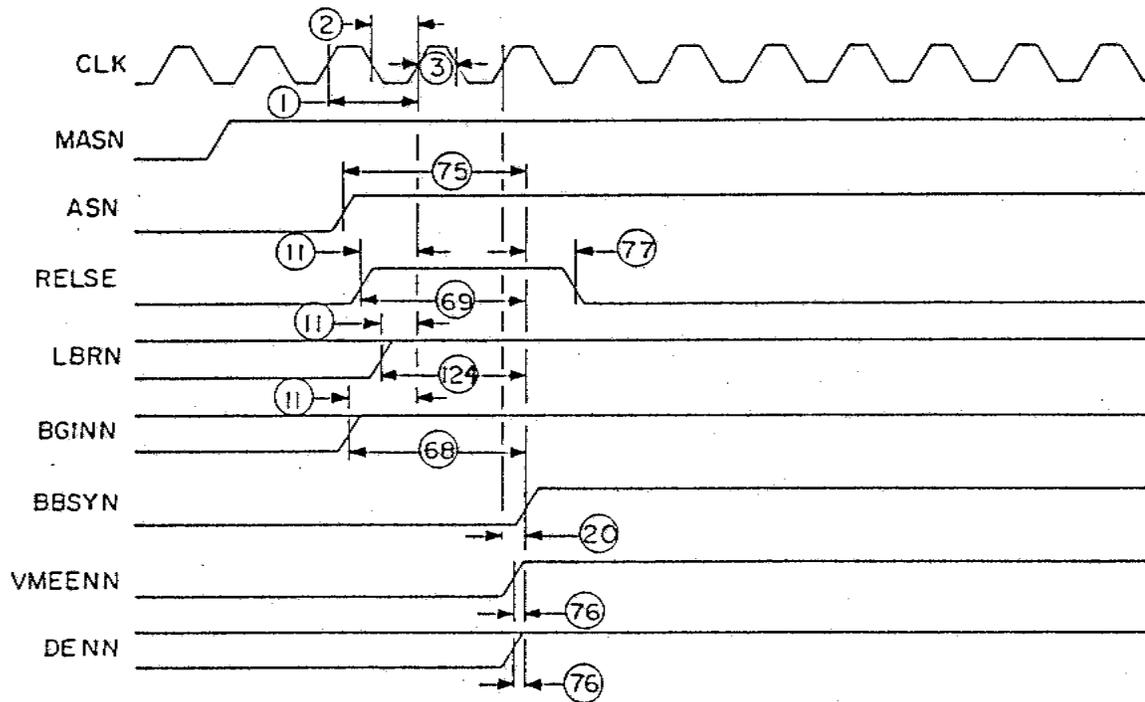


FIGURE 8. Switching waveforms (intercycle VMEbus release).

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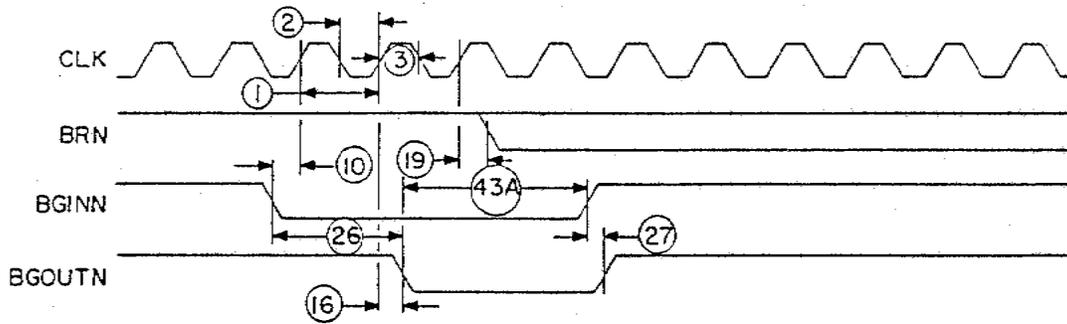


FIGURE 9. Switching waveform (passing a bus grant including earliest possible bus request thereafter).

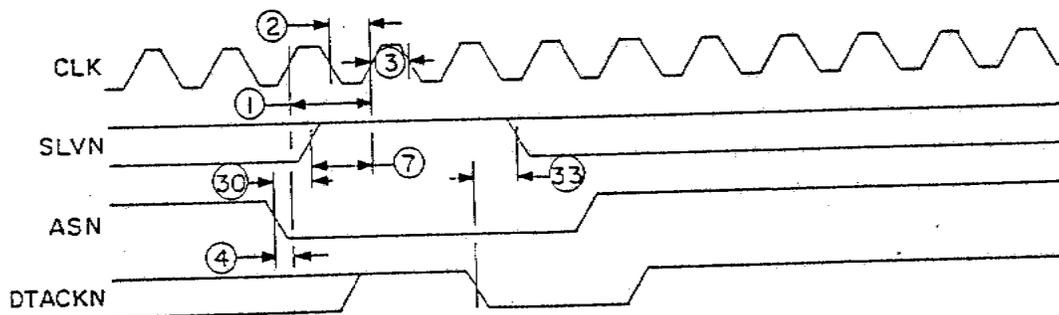


FIGURE 10. Switching waveform (nonselecting cycle on VMEbus)

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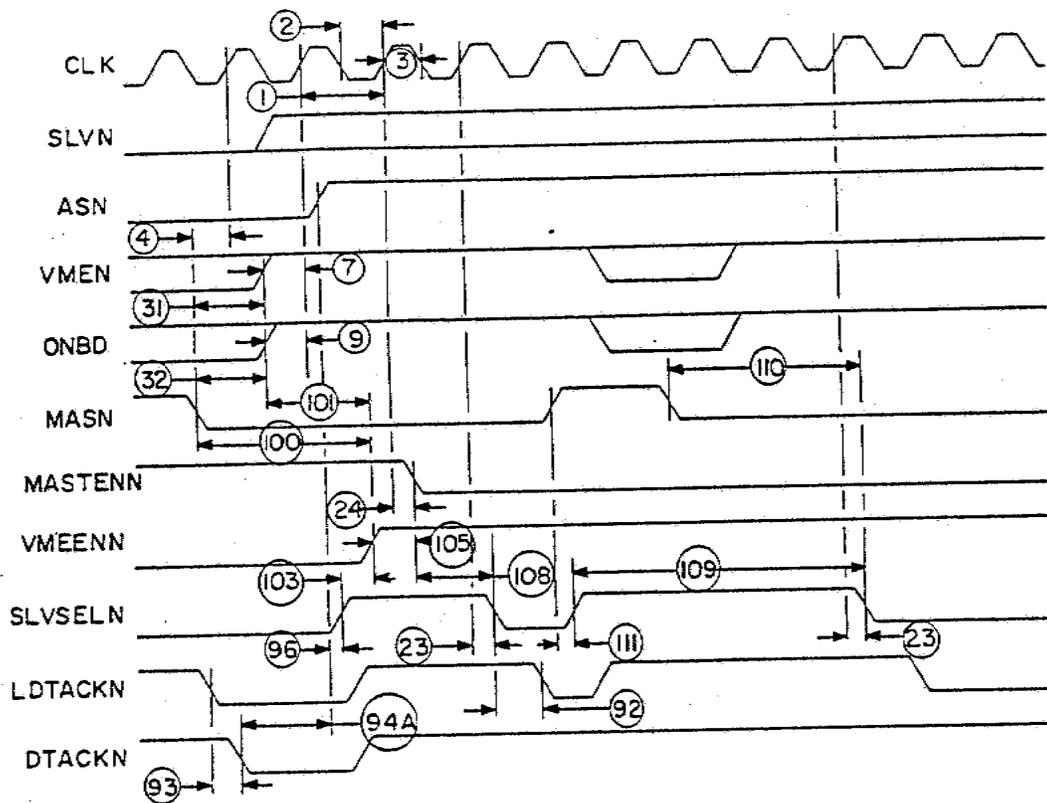


FIGURE 11. Switching waveforms (two on-board cycles following a slave cycle).

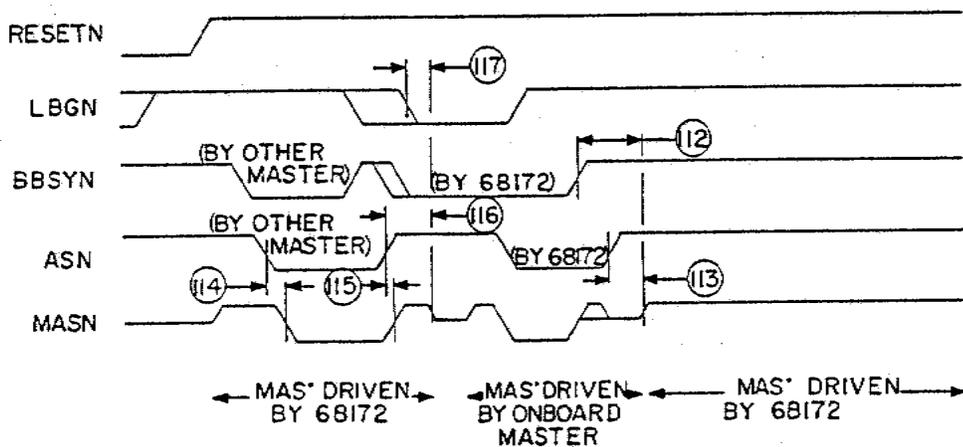


FIGURE 12. Switching waveforms (AS to MAS drive DMA type operation).

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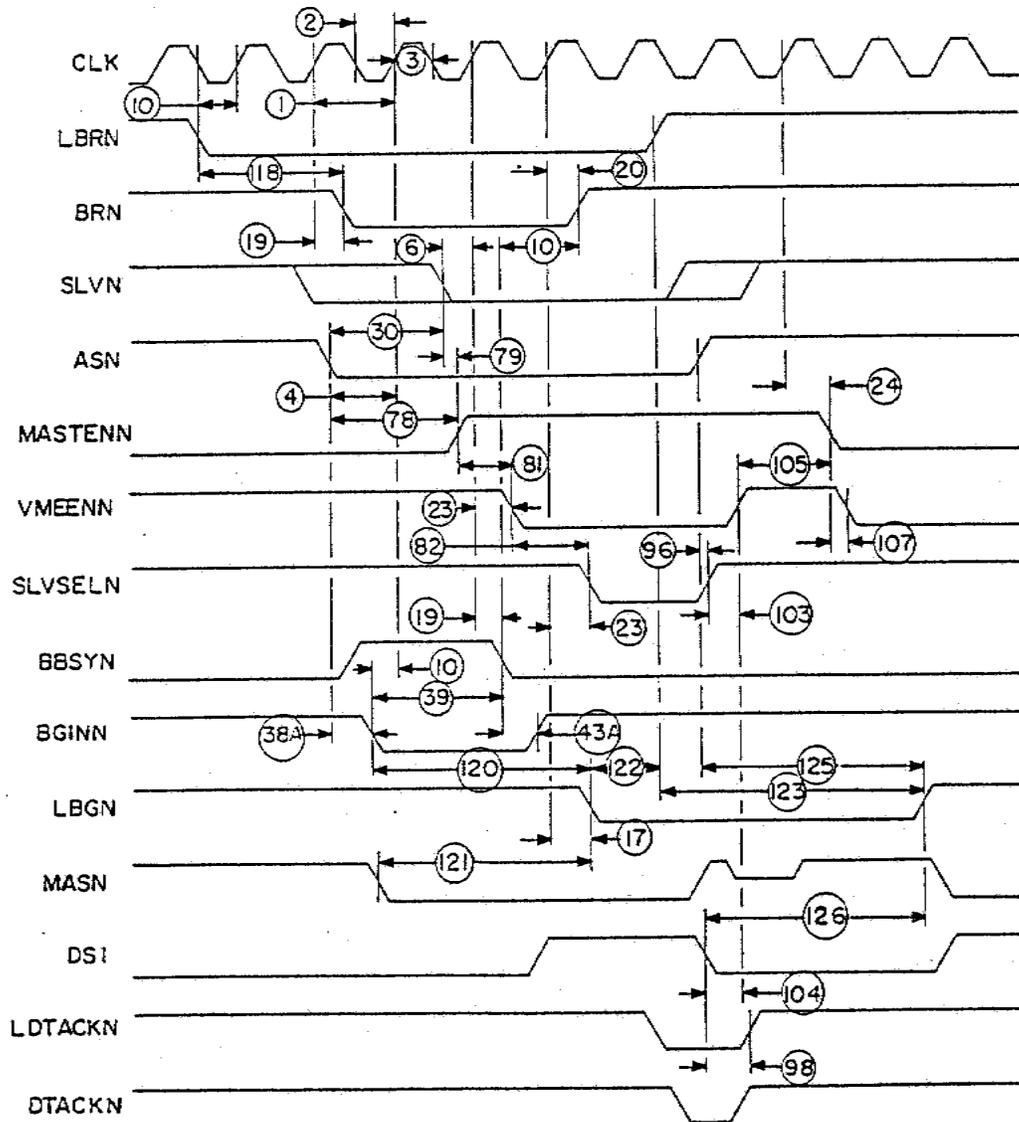


FIGURE 13. Switching waveforms (DMA type VMEbus acquisition with slave cycle from another VMEbus master).

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3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A using the circuit submitted with the certificate of compliance (see 3.6 herein).
 - (2) $T_A = +125^\circ\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroups 7 and 8 shall consist of verifying the pin functions described in 6.6.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A using the circuit submitted with the certificate of compliance (see 3.6 herein).
 - (2) $T_A = +125^\circ\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I) 1/
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,7,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

*PDA applies to subgroup 1.

1/ Any subgroup at the same temperature may be combined using a multifunction tester.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-8528.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8528.

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6.6 Pin descriptions.

Mnemonic	Pin no.	Type	Name and function
CLK	16	I	Clock: User-supplied clock signal.
SLVN	14	I	Slave: Active-low decode of the VMEbus address and address modifier lines indicating that the current cycle is for this board. SLVN should not be qualified with ASN nor VMEENN. It is first sampled on the rising clock edge after the rising edge on which ASN is first detected. It must remain valid until after the next low-going edge on DTACK or or BERRN. In a master-only application, SLVN should be pulled to V _{CC} .
ASN	20	I/O	Address strobe: Direct connect to VMEbus ASN.
VMEN	11	I	VME decode: Active-low decode of the master's address lines, indicating that the master's current cycle is for a slave on the VMEbus. VMEN should not be qualified with MASN nor MASTENN. It is first sampled on the rising clock edge after the one on which MASN is first detected. Thereafter, it must remain valid until MASN goes false (high). In a slave-only configuration, VMEN should be pulled up to V _{CC} .
LBRN	17	I	Local bus request: Connected to the low-active bus request output of a DMA controller. Typically tied to a high logic level in processor-type interfaces.
ONBD	12	I	Onboard: Active-high decode of the master's address lines, indicating that the master's current cycle is for an onboard slave that is dual-ported with the VMEbus. ONBD should not be qualified with MASN or MASTENN. It is first sampled on the rising clock edge after the one on which MASN is first detected. Thereafter, it must remain valid until after MASN goes false (high). In a master-only or slave-only application, ONBD should be grounded. If a master/slave configuration does not contain "local slaves" as shown on figure 3, VMEN and ONBD should both be connected to an active-low "VME decode". A cycle between the onboard master and a local slave (VMEN high, ONBD low) is ignored by BUSCON, and can proceed concurrently with a cycle between another VMEbus master and an onboard dual-ported slave.
MASN	28	I I/O	Master's address strobe: RMW and sequential VMEbus master cycles are accomplished by holding MASN low across several data strobes. If LBGN is high at the end of the RESETN low time, the state of ASN is driven onto MASN whenever BUSCON does not have control of the VMEbus. In a slave-only application, MASN should be pulled up to V _{CC} .

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Mnemonic	Pin no.	Type	Name and function
MASTENN	25	O	Master enable: In a master/slave application, the low state of this signal enables the master onto the shared bus and enables shared-bus responses back to the master. MASTENN also provides the direction control for the VMEbus address transceivers.
VMEENN	1	O	VME enable: Active-low enable for the VMEbus address drivers (master-only) or transceivers (master/slave).
SLVSELN	2	O	Slave select: Active-low select for the onboard slave resources (the shared/dual ported slaves in a master/slave application). Derived from MASN and ONBD, or from ASN and SLVN. If necessary, MASTENN and VMEENN are cycled to provide address setup time before SLVSELN is asserted.
BRN	23	O	Bus request: Active-low, open collector VMEbus request. Direct connect to the selected level among VMEbus BR0 to BR3.
BGINN	27	I	Bus grant in: Direct connect to the selected level among VMEbus BGOIN to BG3IN.
BGOUTN	26	O	Bus grant out: Direct connect to the selected level among VMEbus BG0OUT to BG3OUT.
BBSYN	24	O	Bus busy: Active-low, open collector direct connect to VMEbus BBSY.
LBN	4	I/O	Local bus grant: Active-low, open collector. Can be connected to the bus grant input of a DMA controller. Asserted when LBRN is low and the BUSCON has control of the VMEbus. Grounded, or driven low during RESET, to prevent the ASN state being driven onto MASN when the BUSCON is not in control of the VMEbus.
RELSE	10	I	Release: Active-high signal indicating that the onboard logic wants to release control of the VMEbus. In DMA controller applications, the BGACKN output of the DMAC should be connected to (or positive-logic ANDed into) this signal.
DTACKN	19	I/O O	Data transfer acknowledge: Active-low, open collector. Direct connect to VMEbus DTACK.
BERRN	22	I/O O	Bus error: Active-low, open collector. Direct connect to VMEbus BERR.

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Mnemonic	Pin no.	Type	Name and function
LDTACKN	7	O, I/O I	Local DTACK: Active-low, open collector. Output to onboard master and/or input from onboard slave.
LBERRN	6	O, I/O I	Local bus error: Onboard active-low, open collector. Output to onboard master and/or input from onboard slave.
DSI	3	I	Data strobe: The high-active or of the onboard data strobes, which may be from the onboard master or VMEbus master.
DSENN	5	O	Data strobe enable: Low-active, used to enable the onboard data strobes onto the VMEbus.
R/WN	13	I	Read/write: Onboard R/W signal from the onboard master or VMEbus master.
DDIR	15	O	Data direction control: Direction control for VMEbus data transceivers. A high level indicates the "onboard-to-VMEbus" direction.
DENN	9	O	Data enable: Low-active enable for VMEbus data transceivers.
RESETN	18	I	RESET: Low-active reset. Clears BUSCON logic.
V _{CC}	8	I	Power supply: +5 volts.
GND	21	I	Ground: 0 V reference.

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6.7 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC. The approved source listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>
5962-8770501XX	18324	68172/BXA

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

18324

Vendor name
and address

Signetics Corporation
1275 South 800 East Street
Orem, UT 84058
Point of contact: 811 E. Arques
Sunnyvale, CA 94088-3409

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87705
		REVISION LEVEL A	SHEET 29