

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with N.O.R. 5962-R343-97.	97-06-23	R. MONNIN
B	Add CAGE U3158 and update to reflect current requirements. - ro	02-09-25	R. MONNIN

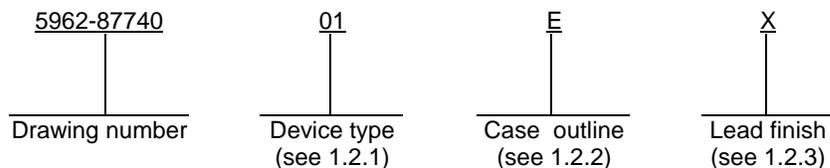
THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

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SHEET																				
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SHEET																				
REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B						
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11								
PMIC N/A	PREPARED BY MARCIA B. KELLEHER				DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 http://www.dsccl.dla.mil															
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY D. A. DICENZO																			
	APPROVED BY MICHAEL A. FRYE				MICROCIRCUIT, LINEAR, POWER SUPPLY SUPERVISORY CIRCUIT, MONOLITHIC SILICON															
	DRAWING APPROVAL DATE 88-05-09																			
	REVISION LEVEL B																			
				SHEET 1 OF 11																

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	1543	Power supply output supervisory circuit
02	1544	Power supply output supervisory circuit

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
V	GDIP1-T18 or CDIP2-T18	18	Dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Input supply voltage (V_{IN})	40 V dc
Sense inputs	V_{IN}
SCR trigger current	-600 mA ^{1/}
Indicator output voltage	40 V dc
Indicator output sink current	50 mA
Power dissipation (P_D)	1000 mW ^{2/ 3/}
Junction temperature (T_J)	+150°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases E and V	See MIL-STD-1835

1.4 Recommended operating conditions.

Ambient operating temperature range (T_A)	-55°C to +125°C
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^{1/} At higher input voltages, a dissipation limiting resistor (R_G) is required: $R_G > (V_{IN} - 5 V) / 0.2 A$.

^{2/} Derate linearly above $T_A = +25^\circ C$ at 8.0 mW/°C.

^{3/} Must withstand the added P_D due to short circuit test; e.g., I_{OS} .

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 -- Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 -- List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional diagrams. The functional diagrams shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C V _{IN} = 10 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Total device							
Input voltage range	V _{INR}		1,2	All	4.5	40	V
			3		4.7	40	
Supply current	I _S	V _{IN} = 40 V	1	All		10	mA
			2,3			15	
Reference section (V _{REF} and V _{IN} pins)							
Output voltage	V _O		1	All	2.48	2.52	V
			2,3		2.45	2.55	
Line regulation	V _{LINE}	V _{IN} = 5.0 V to 30 V	1,2,3	All		5.0	mV
Load regulation	V _{LOAD}	I _{REF} = 0 mA to -10 mA	1,2,3	All		10	mV
Short circuit current	I _{OS}	V _{REF} = 0 V	1,2,3	All	-10	-40	mA
SCR TRIGGER section (SCR TRIGGER, REMOTE ACTIVATE, and RESET pins)							
Peak output current	I _{O(pk)}	V _{IN} = 5.0 V, R _G = 0 Ω, V _O = 0 V	1,2,3	All	-100	-600	mA
Peak output voltage	V _{O(pk)}	V _{IN} = 15 V, I _O = 100 mA	1,2,3	All	12		V
Output off voltage	V _{O(off)}	V _{IN} = 40 V	1,2,3	All		0.1	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C V _{IN} = 10 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	

SCR TRIGGER section (SCR TRIGGER, REMOTE ACTIVATE, and RESET pins) – continued.

REMOTE ACTIVATE current	I _{ACT}	REMOTE ACTIVATE pin = GND	1,2,3	All		-0.8	mA
REMOTE ACTIVATE voltage	V _{ACT}	REMOTE ACTIVATE pin open	1,2,3	All		6.0	V
RESET current	I _{RESET}	REMOTE ACTIVATE and RESET pins = GND	1,2,3	All		-0.8	mA
RESET voltage	V _{RESET}	RESET pin = open, REMOTE ACTIVATE pin = GND	1,2,3	All		6.0	V

Comparator sections (OV INDICATE, OV DELAY, OV INPUT, UV INPUT, UV DELAY, and UV INDICATE pins).

For device 02, OV and UV INPUTS are tested inverted and noninverted respectively.

Input threshold voltage ^{1/}	V _{IN(th)}		1	All	2.45	2.55	V
			2,3		2.40	2.60	
Input bias current	I _{IB}	Sense input = 0 V	1,2,3	All		-1.0	μA
Delay saturation voltage	V _{D(sat)}		1,2,3	All		0.5	V
Delay high level voltage	V _{DH}		1,2,3	All		8.0	V
Delay charging current	I _D	V _D = 0 V	1,2,3	All	-200	-300	μA
Indicate saturation	V _{IND(SAT)}	I _L = +10 mA	1,2,3	All		0.5	V
Indicate leakage current	I _{L(IND)}	V _{IND} = 40 V	1,2,3	All		1.0	μA

Current limit section (CL INV INPUT, CL NI INPUT, OFFSET/COMP, CL OUTPUT, GROUND pins)

Input voltage range	V _{INR}		1,2,3	All	0	V _{IN} – 3.0 V	V
Input bias current	I _{IB}	OFFSET/COMP pin = open, V _{CM} = 0 V	1,2,3	All		-1.0	μA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C V _{IN} = 10 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Current limit section – continued (CL INV INPUT, CL NI INPUT, OFFSET/COMP, CL OUTPUT, GROUND pins)							
Input offset voltage	V _{OS}	OFFSET/COMP pin = open, V _{CM} = 0 V	1,2,3	All		10	mV
		10 kΩ ±0.1% from OFFSET/COMP pin to GROUND. 2 kΩ from C _L OUTPUT to V _{REF}			80	120	
Common mode rejection	CMRR	0 V ≤ V _{CM} ≤ 12 V, V _{IN} = 15 V	4,5,6	All	60		dB
Open loop voltage gain	A _{VOL}	OFFSET/COMP pin = open, V _{CM} = 0 V	4,5,6	All	72		dB
Output saturation	V _{O(SAT)}	I _L = -10 mA	1,2,3	All		0.5	V
Output leakage	I _{L(IND)}	V _{IND} = 40 V	1,2,3	All		1.0	μA

1/ Input voltage rising on pin 0 V input and falling on pin UV input.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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Device types	01	02
Case outlines	E	V
Terminal number	Terminal symbol	
1	SCR TRIGGER	SCR TRIGGER
2	REMOTE ACTIVATE	REMOTE ACTIVATE
3	RESET	RESET
4	OV INDICATE	OV INDICATE
5	OV DELAY	OV DELAY
6	OV NI INPUT	OV NI INPUT
7	UV NI INPUT	OV INV INPUT
8	UV DELAY	UV NI INPUT
9	UV INDICATE	UV INV INPUT
10	CL INV INPUT	UV DELAY
11	CL NI INPUT	UV INDICATE
12	OFFSET/COMP	CL INV INPUT
13	CL OUTPUT	CL NI INPUT
14	GROUND	OFFSET/COMP
15	V _{REF}	CL OUTPUT
16	V _{IN}	GROUND
17	---	V _{REF}
18	---	V _{IN}

FIGURE 1. Terminal connections.

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Device type 01

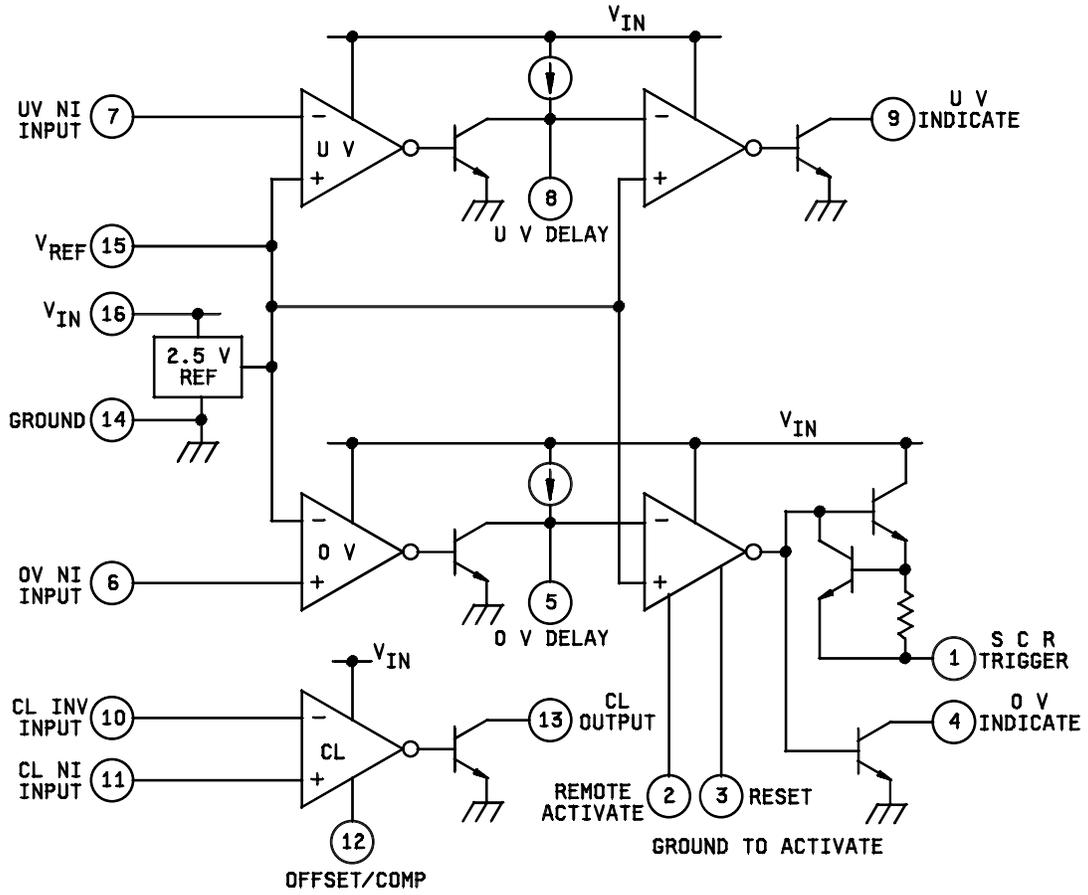


FIGURE 2. Fuctional diagram.

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Device type 02

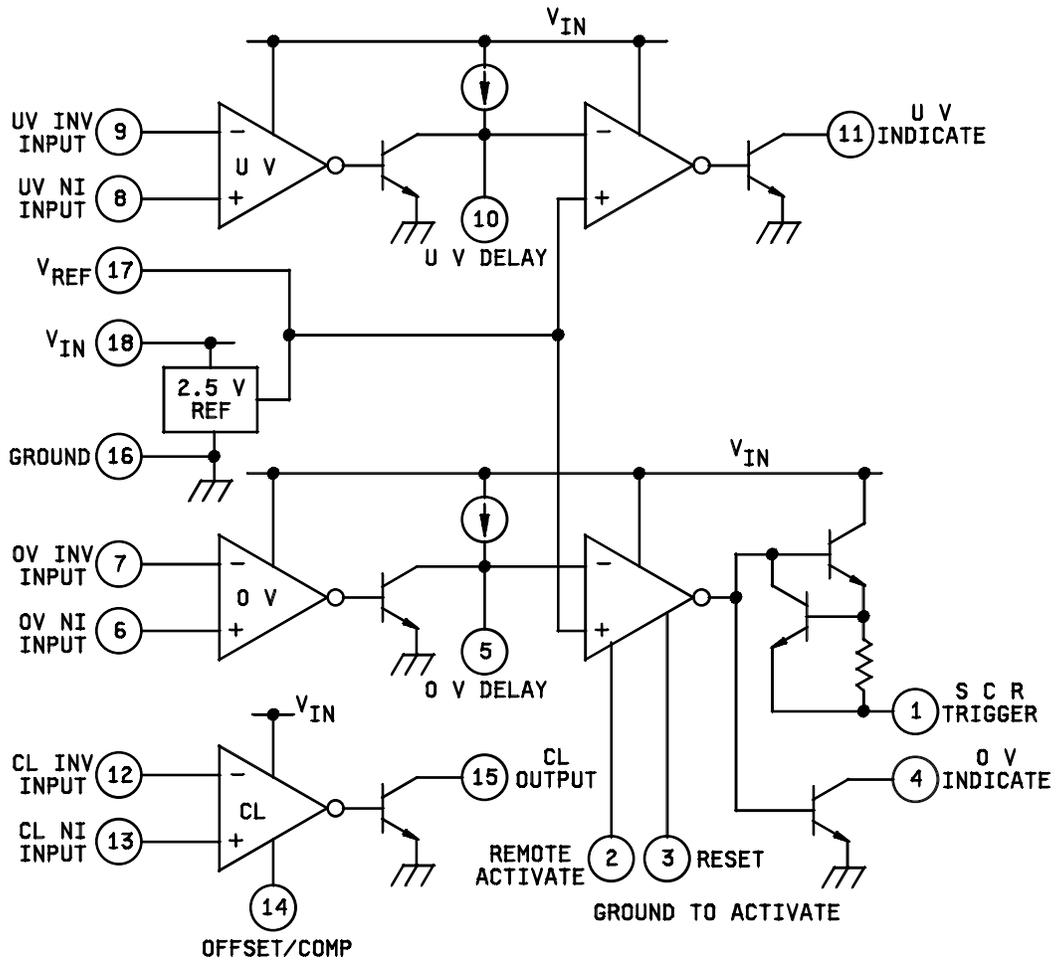


FIGURE 2. Functional diagram – Continued.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,4
Group A test requirements (method 5005)	1,2,3,4,5,6
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-09-25

Approved sources of supply for SMD 5962-87740 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8774001EA	01295	UC1543J/883B
	34333	SG1543J/883B
	U3158	IP1543J-DESC
5962-8774002VA	34333	SG1544J/883B
	U3158	IP1544J-DESC
	<u>3/</u>	UC1544J/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number

Vendor name and address

01295

Texas Instruments, Incorporated
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243
Point of contact: U.S. Highway 75 South
P.O. Box 84, M/S 853
Sherman, TX 75090-9493

34333

Microsemi Integrated Products
11861 Western Avenue
Garden Grove, CA 92641-1816

U3158

Semelab PLC
Coventry Road, Lutterworth
Leicestershire LE174JB
United Kingdom
Point of contact: Martinez & Associates
234 Boston Post Road
Wayland, MA 01778

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