REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R232-93	93-09-21	Michael A. Frye
B	Drawing updated to reflect current requirements. Removed programming logic from truth table B. Editorial changes throughout. - gap	00-11-02	Raymond Monnin

THE FRONT PAGE OF THIS DRAWING HAS BEEN REPLACED

REV																			
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REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
Steve Duncan

DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
89-04-26

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 2K X 8 BIT, ONE TIME PROGRAMMABLE PROM, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
B	A	**67268**	**5962-88734**

SHEET 1 OF 12

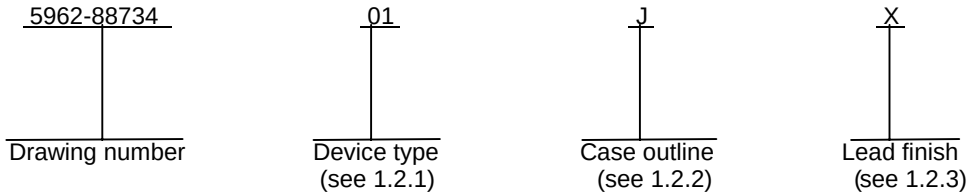
DSCC FORM 2233
APR 97

5962-E555-00

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	7C291	2K X 8-bit PROM	55 ns
02	7C291	2K X 8-bit PROM	45 ns
03	7C291	2K X 8-bit PROM	35 ns
04	7C291	2K X 8-bit PROM	25 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line package
K	GDFP2-F24 or CDFP3-F24	24	Flat package
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line package
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Voltage on any pin with respect to ground	-0.6 V dc to +7.0 V dc
V_{PP} with respect to ground	-0.6 V dc to +13.0 V dc
Power dissipation (P_D)	550 mW 1/
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short-circuit test; e.g., I_{OS}.

APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2 as applicable. When required in groups A, B, or C inspection (see 4.3), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern or equivalent (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.2.2 Programmed devices. The truth tables for programmed devices shall be as specified by an attached altered item drawing.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of PROM configurations, two processing options are provided for selection in the contract using an altered item drawing.

3.6.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 4.3.1. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.6.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing shall be satisfied by the manufacturer prior to delivery.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.10 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V\ dc \le V_{CC} = \le 5.5\ V\ dc$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}	V_{CC} = 4.5 V and 5.5 V	1, 2, 3	All	-0.5 1/	0.8	V
Input high voltage	V_{IH}	V_{CC} = 4.5 V and 5.5 V	1, 2, 3	All	2.0	V_{CC} +0.5 1/	V
Output low voltage 2/	V_{OL}	I_{OL} = 16 mA, V_{CC} = 4.5 V V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	All		0.45	V
Output high voltage 2/	V_{OH}	I_{OH} = -4 mA, V_{CC} = 4.5 V V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	All	2.4		V
Output short circuit Current 1/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = GND	1, 2, 3	All		-200	mA
Input load current 3/	I_{LI}	V_{IN} = 5.5 V and GND	1, 2, 3	All		±10	µA
Output leakage	I_{LO}	V_{OUT} = 5.5 V and GND	1, 2, 3	All		±10	µA
Operating active current 4/	I_{CC}	$\overline{CS}_1 = V_{IL}$, V_{CC} = 5.5 V 0_0 to 0_7 = 0 mA $CS_2 = CS_3 = V_{IH}$ $f = 1/t_{ACC}$	1, 2, 3	All		120	mA
Input capacitance	C_{IN}	V_{IN} = 0 V, f = 1 MHz, T_C = +25°C, see 4.3.1c	4	All		6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V, f = 1 MHz, T_C = +25°C, see 4.3.1c	4	All		12	pF
Address to output delay 5/	t_{ACC}	$\overline{CS}_1 = V_{IL}$ $CS_2 = CS_3 = V_{IH}$	9, 10, 11	01		55	ns
				02		45	
				03		35	
				04		25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} = \le$ 5.5 V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
All chip selects to output delay 4/, 5/	t_{CS}	Either $\overline{CS}_1$, CS_2, or CS_3 6/	9, 10, 11	01		30	ns
				02, 03		25	
				04		20	
All chip selects high to output float 1/, 5/	t_{DF}	Either $\overline{CS}_1$, CS_2, or CS_3 6/	9, 10, 11	01, 02, 03		25	ns
				04		20	
Address to output hold 1/, 5/	t_{OH}	$\overline{CS}_1 = V_{IL}$ $CS_2 = CS_3 = V_{IH}$	9, 10, 11	All	0		ns

1/ May not be tested, but shall be guaranteed to the limits specified in table I.

2/ These are absolute voltages with respect to device ground pin and include all over shoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

3/ Output shall be loaded in accordance with figure 4.

4/ The addresses, ($A_0 – A_{10}$ pins), are toggling between V_{IL} and V_{IH}.

5/ See figures 3 and 4.

6/ Worst case of output control signal lines $\overline{CS}_1$, CS_2, or CS_3.

Device types	01 through 04	
Case outlines	J, K, L	3
Terminal number	Terminal symbol	
1	A_7	NC
2	A_6	A_7
3	A_5	A_6
4	A_4	A_5
5	A_3	A_4
6	A_2	A_3
7	A_1	A_2
8	A_0	A_1
9	O_0	A_0
10	O_1	NC
11	O_2	O_0
12	GND	O_1
13	O_3	O_2
14	O_4	GND
15	O_5	NC
16	O_6	O_3
17	O_7	O_4
18	CS_3	O_5
19	CS_2	O_6
20	$\overline{CS}_1 / V_{PP}$	O_7
21	A_{10}	NC
22	A_9	CS_3
23	A_8	CS_2
24	V_{CC}	$\overline{CS}_1 / V_{PP}$
25	---	A_{10}
26	---	A_9
27	---	A_8
28	---	V_{CC}

FIGURE 1. Terminal connections.

Truth table A

	$\overline{CS}_1/V_{PP}$	CS_2	CS_3	I/0 pins
Programs	V_{PP}	C	C	Data in
Read	V_{IL}	V_{IH}	V_{IH}	Data out
Deselect	V_{IH}	X	X	High - Z
Deselect	X	V_{IL}	X	High - Z
Deselect	X	X	V_{IL}	High - Z

Truth table B

Pin functions				
Mode	CS_3	CS_2	$\overline{CS}_1$	Outputs
Read	V_{IH}	V_{IH}	V_{IL}	Data out
Output disable 1/	X	X	V_{IH}	High - Z
Output disable 1/	X	V_{IL}	X	High - Z
Output disable 1/	V_{IL}	X	X	High - Z

NOTES:
1. X = Don't care but not to exceed V_{CC} plus 5%.

FIGURE 2. Truth tables.

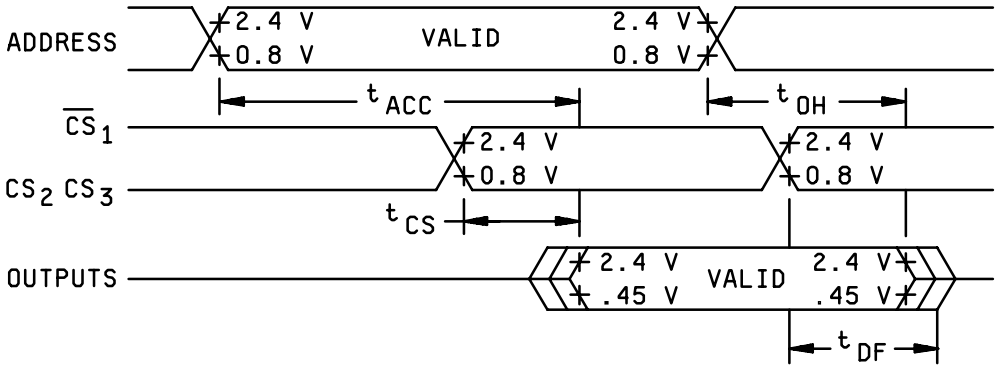
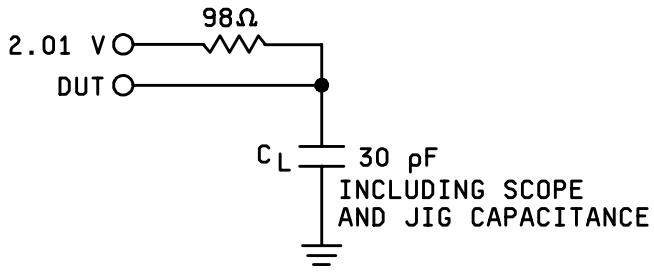


FIGURE 3. AC read timing diagram.

High impedance test systems only.



t_{DF} is tested with C_L = 5 pF.

FIGURE 4. Output load.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements. 1/

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8

* PDA applies to subgroup 1 and 7.
** See 4.3.1c.
1/ Any subgroups at the same temperature may be combined when using a multifunction tester.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input or output capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 4.4). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than four total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than four total device failures allowable.

e. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.7 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 00-11-02

Approved sources of supply for SMD 5962-88734 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8873401JA	3/	WS57C191B-55YMB
5962-8873401KA	3/	WS57C191B-55HMB
5962-8873401LA	3/	WS57C191B-55KMB
5962-88734013A	3/	WS57C191B-55ZMB
5962-8873402JA	3/	CY7C292A-45DMB
	3/	WS57C191B-45YMB
5962-8873402KA	3/	CY7C291A-45KMB
	3/	WS57C191B-45HMB
5962-8873402LA	65786	CY7C291A-45DMB
	3/	WS57C191B-45KMB
5962-88734023A	65786	CY7C291A-45LMB
	3/	WS57C191B-45ZMB
5962-8873403JA	3/	CY7C292A-35DMB
5962-8873403KA	3/	CY7C291A-35KMB
5962-8873403LA	65786	CY7C291A-35DMB
5962-88734033A	65786	CY7C291A-35LMB
5962-8873404JA	3/	CY7C292A-25DMB
5962-8873404KA	3/	CY7C291A-25KMB
5962-8873404LA	65786	CY7C291A-25DMB
5962-88734043A	65786	CY7C291A-25LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address	Truth table
65786	Cypress Semiconductor Inc 3901 North First Street San Jose, CA 94134-1506	B