

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Make changes to table I, figure 1, and editorial changes throughout.	90-06-29	William J. Johnson
B	Changes in accordance with NOR 5962-R079-94.	94-03-24	Michael A. Frye
C	Drawing updated to reflect current requirements. - lgt	01-08-23	Raymond Monnin

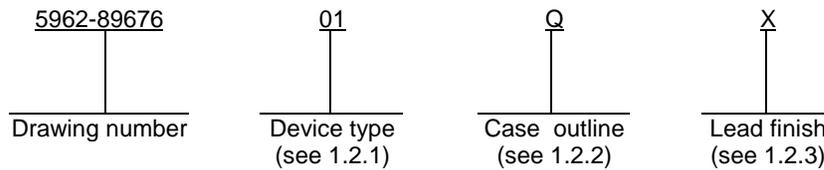
THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

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REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13						
PMIC N/A	PREPARED BY Rick C. Officer				DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 http://www.dsccl.dla.mil															
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Charles E. Besore																			
	APPROVED BY William J. Johnson																			
	DRAWING APPROVAL DATE 15 August 1989																			
	REVISION LEVEL C																			
				SIZE A	CAGE CODE 67268	5962-89676														
				SHEET 1 OF 13																

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>INL test</u>
01	CS5016-S	16-bit CMOS analog-to-digital converter, 16.25 μs	±5.0 LSB
02	CS5016-T	16-bit CMOS analog-to-digital converter, 16.25 μs	±1.0 LSB

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line
X	CQCC1-N44	44	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Positive digital supply (+V _D) voltage range.....	-0.3 V dc to +6.0 V dc	2/
Negative digital supply (-V _D) voltage range.....	+0.3 V dc to -6.0 V dc	
Positive analog supply (+V _A) voltage range.....	-0.3 V dc to +6.0 V dc	
Negative analog supply (-V _A) voltage range.....	+0.3 V dc to -6.0 V dc	
Analog ground (AGND) to digital ground (DGND).....	±0.5 V dc	
Input current, any pin except supplies.....	±10 mA	3/
Analog input voltage (A _{IN} and V _{REF} pins).....	-V _A -0.3 V dc to +V _A +0.3 V dc	
Digital input voltage.....	-0.3 V dc to +V _D +0.3 V dc	
Storage temperature range.....	-65°C to +150°C	
Lead temperature (soldering, 10 seconds).....	+260°C	
Junction temperature (T _J).....	+195°C	
Power dissipation		
Case Q.....	1500 mW	
Case X.....	1100 mW	
Thermal resistance, junction to case (θ _{JC}).....	See MIL-STD-1835	
Thermal resistance, junction to ambient (θ _{JA})		
Case Q.....	45°C/W	
Case X.....	60°C/W	

1/ All voltages referenced to AGND and DGND tied together.
 2/ In addition +V_D must not be greater than +V_A + 0.3 V dc.
 3/ Transient currents of up to 100 mA will not cause latch-up.

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1.4 Recommended operating conditions. 1/

Ambient operating temperature range (T _A)	-55°C to +125°C
Positive digital supply voltage (+V _D).....	+4.5 V dc to +V _A 2/
Negative digital supply voltage (-V _D).....	-4.5 V dc to -5.5 V dc
Positive analog supply voltage (+V _A)	+4.5 V dc to +5.5 V dc
Negative analog supply voltage (-V _A).....	-4.5 V dc to -5.5 V dc
Digital ground (DGND)	0 V dc
Analog ground (AGND)	0 V dc
Digital input low voltage (V _{IL}).....	-0.3 V dc to +0.8 V dc
Digital input high voltage (V _{IH}).....	+2.0 V dc to +V _D
Analog reference input voltage (V _{REF}) range.....	+4.5 V dc
Analog input voltage range:	
Unipolar mode	AGND to +V _{REF}
Bipolar mode.....	-V _{REF} to +V _{REF}

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 -- Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 -- List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ All voltages referenced to AGND and DGND tied together.
2/ In addition +V_D must not be greater than +V_A + 0.3 V dc.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution for which no missing codes is guaranteed	RES	1/	1, 2, 3	All	16		Bits
Integral linearity error	INL	1/ 2/	1, 2, 3	01		±5.0	LSB
				02		±1.0	
Full-scale error	FSE	1/ 2/	1, 2, 3	01		±4.0	LSB
				02		±3.0	
Full-scale error drift	dFSE/d _t	1/ 2/ 3/ 4/	2, 3	All		±4.0	LSB
Unipolar offset error	VOFF	1/ 2/	1, 2, 3	01		±4.0	LSB
				02		±3.0	
Unipolar offset error drift	dVOFF/d _t	1/ 2/ 3/ 4/	2, 3	All		±2.0	LSB
Bipolar offset error	BOFF	1/ 2/	1, 2, 3	01		±4.0	LSB
				02		±2.0	
Bipolar offset error drift	dBOFF/d _t	1/ 2/ 3/ 4/	2, 3	All		±3.0	LSB
Bipolar negative full- scale error	BNFSE	1/ 2/	1, 2, 3	01		±5.0	LSB
				02		±3.0	
Bipolar negative full- scale error drift	dBNFSE/d _t	1/ 2/ 3/ 4/	2, 3	All		±3.0	LSB
Peak harmonic or spurious noise	S/PN	1 kHz input, full scale amplitude, bipolar mode 1/ 2/ 12 kHz input, full scale amplitude, bipolar mode 1/ 2/	4, 5, 6	01	92		dB
				02	100		
				01	82		
				02	85		
Signal to noise ratio	S/(N+D)	1 kHz input, full scale amplitude, bipolar mode 1/ 2/	4, 5, 6	01	84		dB
				02	90		
Analog input capacitance in fine charge mode	C _{IN}	Unipolar mode, T _A = +25°C 1/ 3/	4	All		375	pF
		Bipolar mode, T _A = +25°C 1/ 3/				220	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital input voltage ($\overline{\text{HOLD}}$, CLKIN, CAL, $\overline{\text{INTRLV}}$, BW, RST, BP/ $\overline{\text{UP}}$, $\overline{\text{AO}}$, RD, $\overline{\text{CS}}$)	V _{IH}	<u>5/ 6/</u>	1, 2, 3	All	2.0		V
	V _{IL}					0.8	
Digital input current	I _{IN}	<u>5/ 6/</u>	1, 2, 3	All		±10	μA
Digital output voltage (D ₀ – D ₁₅ , SDATA, SCLK, $\overline{\text{EOC}}$, $\overline{\text{EOT}}$)	V _{OL}	Logic "0", <u>5/ 6/</u> I _{SINK} = -1.6 mA	1, 2, 3	All		0.4	V
	V _{OH}	Logic "1", <u>5/ 6/</u> I _{SOURCE} = 100 μA			+V _D -1.0		
High impedance state output current	I _{OZ}	Pins D ₀ to D ₁₅ only <u>5/ 6/</u>	1, 2, 3	All		±10	μA
Conversion time	t _C	<u>1/ 6/ 7/</u>	9, 10, 11	All		16.25	μs
Acquisition time	t _{ACQ}	T _A = +25°C <u>1/ 2/ 3/ 8/</u>	9	All		3.75	μs
Throughput	t _{PUT}	<u>1/ 2/ 6/</u>	9, 10, 11	All	50		kHz
Positive analog supply current	I _{A+}	+V _A , +V _D = 5.5 V <u>6/ 9/</u> -V _A , -V _D = -5.5 V	1, 2, 3	All		19.0	mA
Negative analog supply current	I _{A-}	+V _A , +V _D = 5.5 V <u>6/ 9/</u> -V _A , -V _D = -5.5 V	1, 2, 3	All		19.0	mA
Positive digital supply current	I _{D+}	+V _A , +V _D = 5.5 V <u>6/ 9/</u> -V _A , -V _D = -5.5 V	1, 2, 3	All		6.0	mA
Negative digital supply current	I _{D-}	+V _A , +V _D = 5.5 V <u>6/ 9/</u> -V _A , -V _D = -5.5 V	1, 2, 3	All		6.0	mA
Master clock <u>10/</u> frequency	f _{CLK}	T _A = -55°C Internally generated CLKIN = 0 V dc +V _D , +V _A = 4.5 V -V _D , -V _A = -4.5 V	11	All	1.75		MHz
$\overline{\text{HOLD}}$ pulse width	t _{HPW}	(see figure 4) <u>5/ 6/ 11/</u>	9, 10, 11	All	1/f _{CLK} +50	t _C	ns
Data delay time	t _{DD}	(see figure 4) <u>5/ 6/ 11/</u>	9, 10, 11	All		100	ns
$\overline{\text{EOC}}$ pulse width	t _{EPW}	(see figure 4) <u>5/ 6/ 11/</u>	9, 10, 11	All	4/f _{CLK} -20		ns
CAL, $\overline{\text{INTRLV}}$ to $\overline{\text{CS}}$ low setup time	t _{CS}	(see figure 5) <u>5/ 6/ 11/</u>	9, 10, 11	All	20		ns
A0 to $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low setup time	t _{AS}	(see figure 5) <u>5/ 6/ 11/</u>	9, 10, 11	All	20		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{\text{CS}}$ or $\overline{\text{RD}}$ High to A0 invalid hold time	t _{AH}	(see figure 5) <u>5/ 6/ 11/</u>	9, 10, 11	All	50		ns
$\overline{\text{CS}}$ High to CAL, $\overline{\text{INTRLV}}$ invalid hold time	t _{CH}	(see figure 5) <u>5/ 6/ 11/</u>	9, 10, 11	All	50		ns
$\overline{\text{CS}}$ low to data valid access time	t _{CA}	$\overline{\text{RD}}$ = logic "0" (see figure 5) <u>5/ 6/ 11/</u>	9, 10, 11	All		150	ns
$\overline{\text{RD}}$ low to data valid access time	t _{RA}	$\overline{\text{CS}}$ = logic "0" (see figure 5) <u>5/ 6/ 11/</u>	9, 10, 11	All		150	ns
Output float delay	t _{FD}	(see figure 5) <u>5/ 6/ 11/</u>	9, 10, 11	All		140	ns
SDATA to SCLK rising setup time	t _{SS}	(see figure 6) <u>5/ 6/ 11/</u>	9, 10, 11	All	2/f _{CLK} -50		ns
SCLK rising to SDATA hold time	t _{SH}	(see figure 6) <u>5/ 6/ 11/</u>	9, 10, 11	All	2/f _{CLK} -100		ns

- 1/ +V_A, +V_D = +5.0 V; -V_A, -V_D = - 5.0 V; V_{REF} = +4.5 V dc; f_{CLK} = 4 MHz; Analog source impedance = 200 Ω; Error tests are done after calibration at the temperature of interest.
- 2/ Synchronous sampling mode ($\overline{\text{EOT}}$ connected to $\overline{\text{HOLD}}$), interleave disabled.
- 3/ This parameter shall be measured only for initial characterization and after process or design changes which may affect this parameter.
- 4/ Total drift over -55°C to +125°C since calibration at power-up at +25°C.
- 5/ +V_A, +V_D = +5.0 V dc ±10%; -V_A, -V_D = -5.0 V dc ±10%.
- 6/ This parameter is guaranteed, if not tested, at T_A = +25°C. This parameter is tested at T_A = -55°C and +125°C.
- 7/ Measured from falling transition on $\overline{\text{HOLD}}$ to falling transition on $\overline{\text{EOC}}$.
- 8/ Acquisition time is the time allowed by the converter for acquisition of the input voltage prior to conversion.
- 9/ All outputs unloaded; All inputs swinging between +V_D and 0 V dc.
- 10/ Externally supplied maximum clock frequency is 4 MHz. Analog parametric measurements are done with the maximum external clock (see footnote 1/).
- 11/ Inputs: logic "0" = 0 V, logic "1" = +V_D; C_L = 50 pF.

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Device types	01 and 02	
Case outlines	Q	X
Terminal number	Terminal symbol	
1	$\overline{\text{HOLD}}$	$\overline{\text{HOLD}}$
2	D ₀	D ₀
3	D ₁	D ₁
4	D ₂	D ₂
5	D ₃	D ₃
6	D ₄	D ₄
7	D ₅	D ₅
8	D ₆	D ₆
9	D ₇	NC
10	DGND	D ₇
11	+V _D	DGND
12	D ₈	+V _D
13	D ₉	NC
14	D ₁₀	D ₈
15	D ₁₁	NC
16	D ₁₂	D ₉
17	D ₁₃	D ₁₀
18	D ₁₄	D ₁₁
19	D ₁₅	D ₁₂
20	CLKIN	D ₁₃
21	$\overline{\text{CS}}$	D ₁₄
22	$\overline{\text{RD}}$	D ₁₅
23	A0	CLKIN
24	BP/ $\overline{\text{UP}}$	$\overline{\text{CS}}$
25	+V _A	$\overline{\text{RD}}$
26	AIN	A0
27	AGND	BP/ $\overline{\text{UP}}$
28	V _{REF}	+V _A
29	REFBUF	AIN
30	-V _A	AGND
31	TST	V _{REF}
32	RST	REFBUF
33	BW	NC
34	$\overline{\text{INTRLV}}$	-V _A
35	CAL	TST
36	-V _D	RST
37	$\overline{\text{EOT}}$	BW
38	$\overline{\text{EOC}}$	$\overline{\text{INTRLV}}$
39	SCLK	CAL
40	SDATA	-V _D
41	----	$\overline{\text{EOT}}$
42	----	$\overline{\text{EOC}}$
43	----	SCLK
44	----	SDATA

NC = Not connected

FIGURE 1. Terminal connections.

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Function	HOLD	CS	CAL	INTRLV	RD	A0	RST
Hold and start convert		X	X	X	X	*	0
Initiate burst calibration	X	0	1	X	X	*	0
Stop burst cal and begin track	1	0	0	X	X	*	0
Initiate interleave calibration	X	0	X	0	X	*	0
Terminate interleave cal	X	0	X	1	X	*	0
Read output data	X	0	X	X	0	1	0
Read status register	1	0	X	X	0	0	0
High impedance data bus	X	1	X	X	X	*	X
High impedance data bus	X	X	X	X	1	*	X
Reset	X	X	X	X	X	X	1
Reset	0	0	X	X	X	0	X

* The status of A0 is not critical to the operation specified. However A0 should not be low with CS AND HOLD low, or a software reset will result.

FIGURE 2. Truth table.

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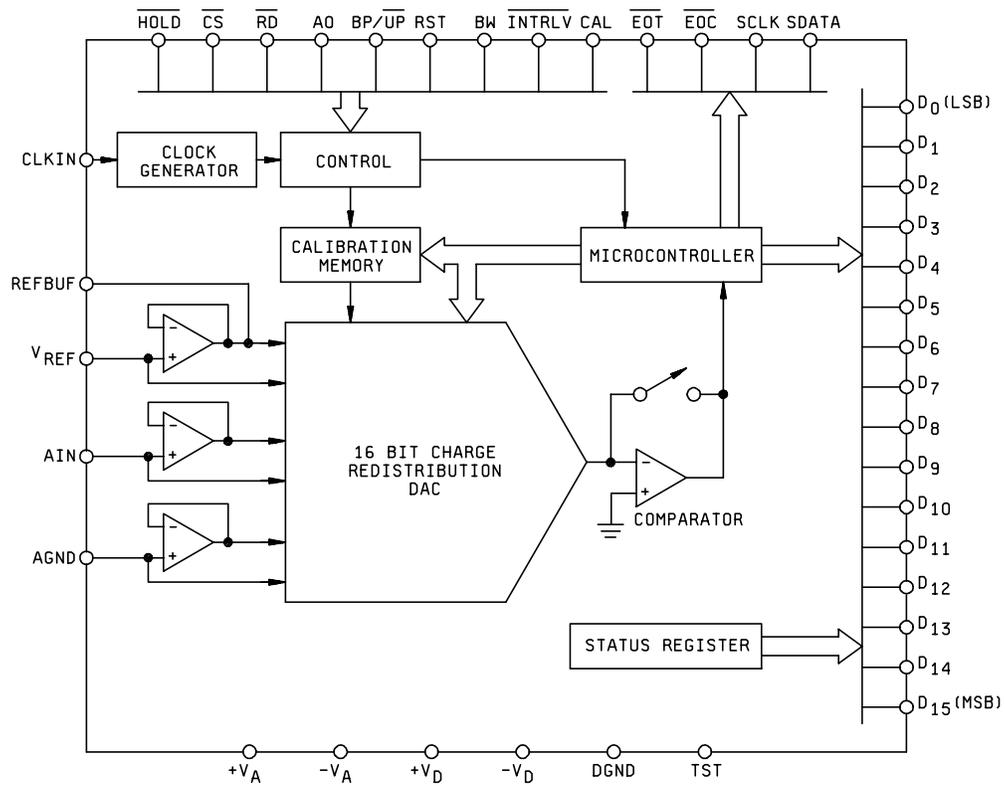


FIGURE 3. Block diagram.

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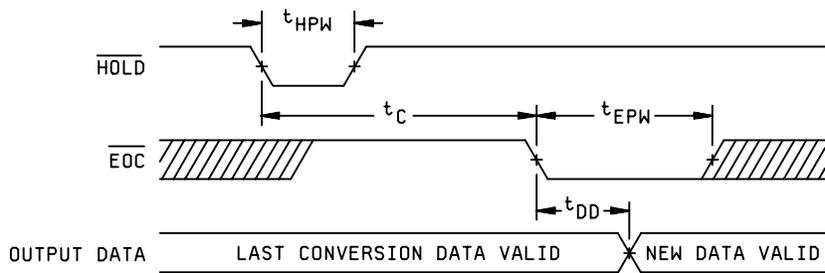


FIGURE 4. Conversion timing.

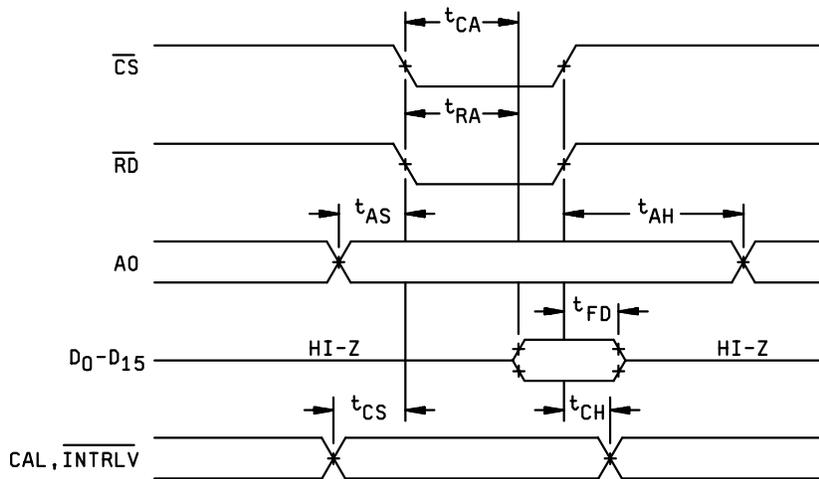


FIGURE 5. Read and calibration control timing.

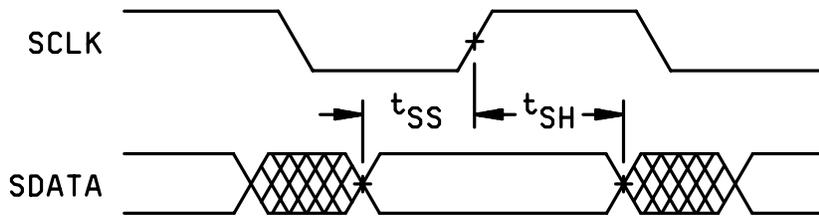


FIGURE 6. Serial output timing.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 7 and 8, in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1, 4
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 5, 6, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6, 9**, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3

* PDA applies to subgroup 1.

** Subgroup 9, if not tested shall be guaranteed to the limits specified in table I herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89676
		REVISION LEVEL C	SHEET 13

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-08-23

Approved sources of supply for SMD 5962-89676 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8967601QA	68911	SEI5016-SD16B
5962-8967601XA	68911	SEI5016-SE16B
5962-8967602QA	68911	SEI5016-TD16B
5962-8967602XA	68911	SEI5016-TE16B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

68911

Vendor name
and address

Space Electronics, Inc.
4031 Sorrento Valley Blvd.
San Diego, CA 92121-1404

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.