REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. - ro	01-11-15	R. MONNIN

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																			
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REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
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APPROVED BY
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DRAWING APPROVAL DATE
91-12-02

MICROCIRCUIT, LINEAR, RESOLVER-TO-DIGITAL CONVERTER, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
A	A	**67268**	**5962-90962**

SHEET 1 OF 14

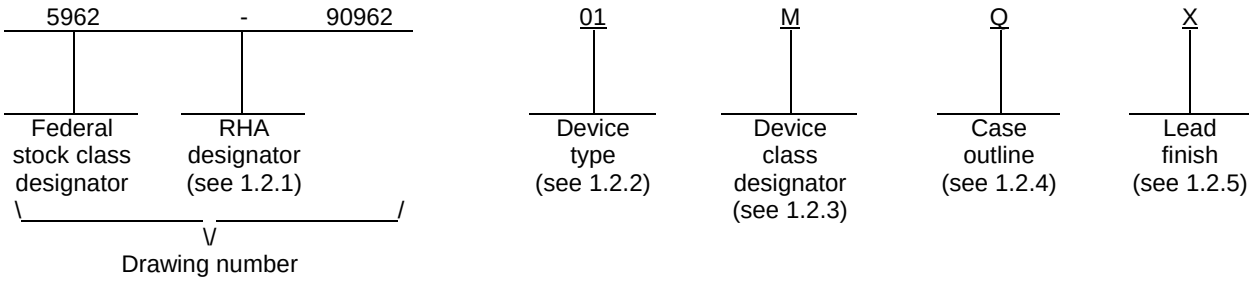
DSCC FORM 2233
APR 97

5962-E048-02

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD2S80A	Resolver-to-digital converter, 4 arc minute accuracy and 10 to 16 bits resolution

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line
X	CQCC1-N44	44	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Positive power supply ($+V_S$) to GND ..... +14.0 V dc 2/ 3/
Negative power supply ($-V_S$) to GND ..... -14.0 V dc 2/ 3/
Logic power supply (V_L) ..... $+V_S$ 2/
Digital input voltage to GND ..... -0.4 V to V_L
Voltage controlled oscillator (VCO) input ..... +14.0 V to $-V_S$ 2/ 3/
Demodulator (DEMOD) INPUT ..... +14.0 V to $-V_S$
INTEGRATOR INPUT ..... +14.0 V to $-V_S$
V_{REF} to GND ..... +14.0 V to $-V_S$ 4/
Analog input voltage (SIN, COS) to GND ..... +14.0 V to $-V_S$ 4/
Power dissipation (P_D) ..... 860 mW
Storage temperature range ..... -65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Thermal resistance, junction-to-case (θ_{JC}) :
Case Q ..... 11°C/W
Case X ..... 10°C/W

1.4 Recommended operating conditions.

Power supply voltage ($+V_S$ to $-V_S$) ..... ±12 V dc ±10 %
Power supply voltage (V_L) ..... +5 V ±10 %
ANALOG GND = DIGITAL GND ..... 0 V 5/
Analog input voltage (SIN, COS) ..... 2 V_{RMS} ±10 %
Analog input voltage (REF) ..... 1 V to 8 V peak
Ambient operating temperature range (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ GND refers to ANALOG GND.
3/ SIGNAL GND is internally connected to ANALOG GND.
4/ SIN, COS, REF input voltage may be present without $+V_S$, $-V_S$, V_L.
5/ ANALOG GND must be externally connected to DIGITAL GND.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and post irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Angular accuracy 3/		$+V_S$ = +10.8 V dc, $-V_S$ = -10.8 V dc, V_L = 5.0 V dc, SC1 = SC2 = high, 16 bit resolution	1,2,3	01		±4	arc mins
		$+V_S$ = +13.2 V dc, $-V_S$ = -13.2 V dc, V_L = 5.0 V dc, SC1 = SC2 = high, 16 bit resolution				±4	
Missing codes 3/		$+V_S$ = +10.8 V dc, $-V_S$ = -10.8 V dc, V_L = 5.0 V dc, SC1 = SC2 = high, 16 bit resolution	1,2,3	01		4	codes
		$+V_S$ = +13.2 V dc, $-V_S$ = -13.2 V dc, V_L = 5.0 V dc, SC1 = SC2 = high, 16 bit resolution				4	
Total effective angular offset		Output data nulled by application of offset current to integrator input	1,2,3	01		±800	nA
DEMOD OUTPUT 3/ scaling			1,2,3	01	90	110	nA/bit
VCO total effective offset		Measured with 68 kΩ input resistance	1,2	01		380	nA
			3			400	
INTEGRATOR OUTPUT range		$\pm V_S$ = ±12 V dc, V_L = 5.0 V dc, 1 mA load	1,2,3	01	±8		V
		$\pm V_S$ = ±10.8 V dc, V_L = 5.0 V dc, 1 mA load			±7		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Digital inputs high voltage	V_{IH}	DB1 – DB16, $\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$, BYTE SELECT, $\pm V_S = \pm 10.8$ V dc, $V_L = 5.0$ V dc	1,2,3	01	2.0		V
Digital inputs low voltage	V_{IL}	DB1 – DB16, $\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$, BYTE SELECT, $\pm V_S = \pm 13.2$ V dc, $V_L = 5.0$ V dc	1,2,3	01		0.8	V
Digital inputs high current	I_{IH}	DB1 – DB16, $\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$, BYTE SELECT, $\pm V_S = \pm 13.2$ V dc, $V_L = 5.5$ V dc, $V_{IH} = 5.5$ V dc	1,2,3	01		±100	µA
Digital inputs low current	I_{IL}	DB1 – DB16, $\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$, BYTE SELECT, $\pm V_S = \pm 13.2$ V dc, $V_L = 5.5$ V dc, $V_{IL} = 0.0$ V dc	1,2,3	01		±100	µA
Digital inputs low voltage 4/	V_{IL}	SC1, SC2, DATA LOAD, $\pm V_S = \pm 12.0$ V dc, $V_L = 5.0$ V dc, $\overline{\text{ENABLE}}$ = high	1,2,3	01		1.0	V
Digital inputs low current 4/	I_{IL}	SC1, SC2, DATA LOAD, $\pm V_S = \pm 12.0$ V dc, $V_L = 5.0$ V dc, $\overline{\text{ENABLE}}$ = high	1,2,3	01		-400	µA
Digital outputs high voltage	V_{OH}	DB1 – DB16, RIPPLE CLOCK, DIRECTION, $\pm V_S = \pm 12.0$ V dc, $V_L = 4.5$ V dc, $I_{OH} = 100$ µA	1,2,3	01	2.4		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Digital outputs low voltage	V_{OL}	DB1 – DB16, RIPPLE CLOCK, DIRECTION, $\pm V_S = \pm 12.0$ V dc, $V_L = 5.5$ V dc, $I_{OL} = 1.2$ mA	1,2,3	01		0.4	V
Floating state leakage current	I_{LKG}	DB1 – DB16 only, $\pm V_S = \pm 12.0$ V dc, $V_L = 5.5$ V dc, $V_{OL} = 0.0$ V	1,2,3	01		±100	µA
		DB1 – DB16 only, $\pm V_S = \pm 12.0$ V dc, $V_L = 5.5$ V dc, $V_{OH} = 5.0$ V				±100	
Power supply current from $+V_S$	$+I_S$	$+V_S = +13.2$ V dc	1,2,3	01		30	mA
Power supply current from $-V_S$	$-I_S$	$-V_S = -13.2$ V dc	1,2,3	01		-30	mA
Power supply current from $+V_L$	$+I_L$	$V_L = 5.5$ V dc	1,2,3	01		1.5	mA
VCO maximum rate			4,5,6	01		1.1	MHz
VCO gain scaling		Measured with VCO input current of ±10 µA	4,5,6	01	7110	8690	Hz/µA
VCO linearity 5/		VCO measured at 10 points over the frequency range 0.0 MHz to 1.0 MHz	4,5,6	01		±3	percent
Busy pulse width 3/	t_{BUSY}		9,10,11	01	200	600	ns

1/ $+V_S = +12.0$ V dc, $-V_S = -12.0$ V dc, $V_L = +5.0$ V dc.
2/ The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.
3/ V_{SIN}, $V_{COS} = 2\ V_{RMS}$ maximum at 5 kHz. $V_{REF} = 2\ V_{RMS}$ at 5 kHz.
4/ Digital inputs SC1, SC2, DATA LOAD are internally pulled up to $+V_S$.
5/ VCO linearity is expressed as percentage of reading.

Device type	01	
Case outlines	Q	X
Terminal number	Terminal symbol	
1	REF INPUT	REF INPUT
2	DEMOD INPUT	DEMOD INPUT
3	AC ERROR OUTPUT	AC ERROR OUTPUT
4	COS	COS
5	ANALOG GND	ANALOG GND
6	SIGNAL GND	SIGNAL GND
7	SIN	SIN
8	$+V_S$	$+V_S$
9	DB1 (MSB)	NC
10	DB2	DB1 (MSB)
11	DB3	DB2
12	DB4	DB3
13	DB5	DB4
14	DB6	DB5
15	DB7	DB6
16	DB8	DB7
17	DB9	DB8
18	DB10	DB9
19	DB11	DB10
20	DB12	DB11
21	DB13	DB12
22	DB14	DB13
23	DB15	DB14
24	DB16 (LSB)	DB15
25	V_L	DB16 (LSB)
26	$\overline{\text{ENABLE}}$	V_L
27	BYTE SELECT	$\overline{\text{ENABLE}}$
28	$\overline{\text{INHIBIT}}$	BYTE SELECT
29	DIGITAL GND	NC
30	SC1	$\overline{\text{INHIBIT}}$
31	SC2	DIGITAL GND
32	DATA LOAD	SC1
33	BUSY	SC2
34	DIRECTION	NC
35	RIPPLE CLOCK	DATA LOAD
36	$-V_S$	BUSY
37	VCO INPUT	DIRECTION
38	INTEGRATOR INPUT	RIPPLE CLOCK
39	INTEGRATOR OUTPUT	$-V_S$
40	DEMOD OUTPUT	VCO INPUT
41	---	NC
42	---	INTEGRATOR INPUT
43	---	INTEGRATOR OUTPUT
44	---	DEMOD OUTPUT

NC = No connection

FIGURE 1. Terminal connections.

Terminal symbol	Description
REFERENCE INPUT	Input pin for the reference signal.
DEMOD INPUT	Demodulator input pin.
AC ERROR OUTPUT	Output of ratio multiplier.
COS	Input pin for cosine signal from resolver.
ANALOG GROUND	Power ground.
SIGNAL GROUND	Ground pin for signals from resolvers.
SIN	Input pin for sine signal from resolver.
$+V_S$	Positive power supply.
DB1 – DB16	Parallel output data bits.
V_L	Logic power supply.
ENABLE	Logic high sets the output data bits to high impedence state, a logic low presents the data in the latches to the latches to the output pins.
BYTE SELECT	Selects the data output bits presented on data bits 1 to 8. Logic high will present the 8 most significant bits; a logic low will present the least significant byte.
INHIBIT	Logic low inhibits the data transfer from the counter to the output latches.
DIGITAL GROUND	Ground pin for digital circuitry.
SC1, SC2	Logic inputs used for selecting the resolution of the converter.
DATA LOAD	Logic low allows data to be loaded into the counters.
BUSY	Converter BUSY. A logic high indicates that the output latches are being updated and data should not be transferred.
DIRECTION	Logic output indicating the direction of rotation of the input signals.
RIPPLE CLOCK	A negative going pulse whenever the output of the converter changes from all 1's to all 0's or the converse.
$-V_S$	Negative power supply.
VCO INPUT	Input pin to the voltage controlled oscillator (VCO).
INTEGRATOR INPUT	Input pin of integrator.
INTEGRATOR OUTPUT	Output pin of integrator.
DEMOD OUTPUT	Output pin of demodulator.

FIGURE 1. Terminal connections – continued.

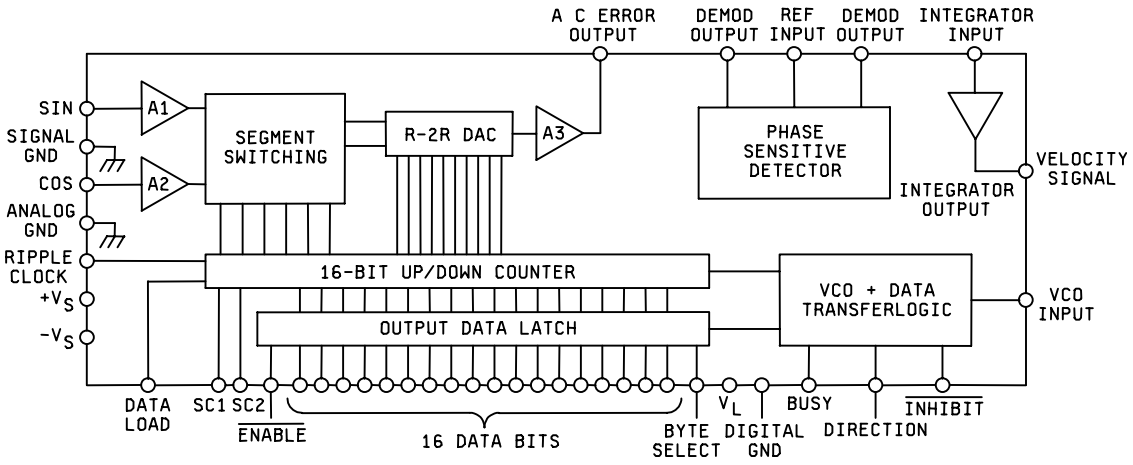


FIGURE 2. Block diagram.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,4,9	1,4,9	1,4,9
Final electrical parameters (see 4.2)	1,2,3,4,5,6, 1/ 9,10,11	1,2,3,4,5, 1/ 6,9,10,11	1,2,3,4,5, 1/ 6,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1,4,9	1,4,9	1,4,9
Group D end-point electrical parameters (see 4.4)	1,4,9	1,4,9	1,4,9
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions.

BINARY BITS (N)	RESOLUTION (2^N)	DEGREES / BIT	MINUTES / BIT	SECONDS / BIT
0	1	360.0	21600.0	1296000.0
1	2	180.0	10800.0	648000.0
2	4	90.0	5400.0	324000.0
3	8	45.0	2700.0	162000.0
4	16	22.5	1350.0	81000.0
5	32	11.25	675.0	40500.0
6	64	5.625	337.5	20250.0
7	128	2.8125	168.75	10125.0
8	256	1.40625	84.375	5062.5
9	512	0.703125	42.1875	2531.25
10	1024	0.3515625	21.09375	1265.625
11	2048	0.1757813	10.546875	632.8125
12	4096	0.0878906	5.273438	316.40625
13	8192	0.0439453	2.636719	158.20313
14	16384	0.0219727	1.318359	79.10156
15	32768	0.0109836	0.659180	39.55078
16	65536	0.0054932	0.329590	19.77539
17	131072	0.0027466	0.164795	9.88770
18	262144	0.0013733	0.082397	4.94385

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-11-15

Approved sources of supply for SMD 5962-90962 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9096201MQA	24355	AD2S80ATD/883B
5962-9096201MXA	24355	AD2S80ATE/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 7910 Traid Center Drive Greensboro, NC 27409-9605