

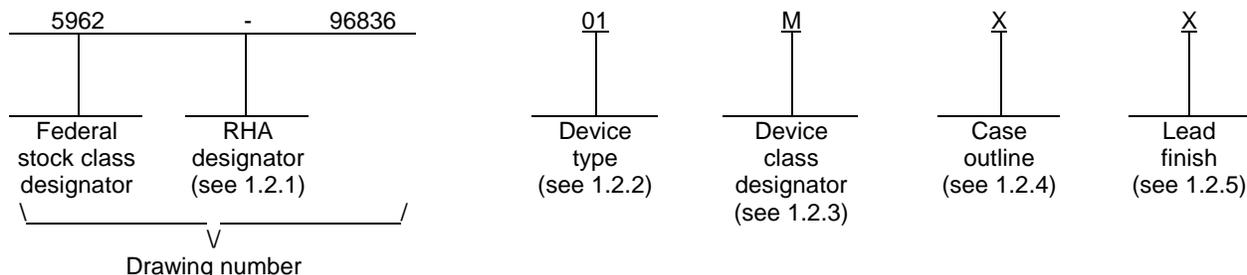
| REVISIONS | | | |
|-----------|---|-----------------|----------------|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Update drawing to current requirements. Editorial changes throughout. - gap | 02-05-08 | Raymond Monnin |

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| REV | | | | | | | | | | | | | | | | | | | | |
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| REV | | | | | | | | | | | | | | | | | | | | |
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| REV STATUS | REV | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | | | | | |
| PMIC N/A | PREPARED BY Kenneth Rice | <p align="center">DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 http://www.dscc.dla.mil</p> <p>MICROCIRCUIT, MEMORY, DIGITAL, CMOS, FIELD PROGRAMMABLE GATE ARRAY 2000 GATES, MONOLITHIC SILICON</p> | | | | | | | | | | | | | | | | | | |
| <p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p> | CHECKED BY Jeff Bowling | | | | | | | | | | | | | | | | | | | |
| | APPROVED BY Raymond Monnin | | | | | | | | | | | | | | | | | | | |
| | DRAWING APPROVAL DATE 98-03-31 | | | | | | | | | | | | | | | | | | | |
| REVISION LEVEL A | SIZE A | CAGE CODE 67268 | 5962-96836 | | | | | | | | | | | | | | | | | |
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1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function | Delay Factor (K) | |
|-------------|----------------|---------------------|------------------|------|
| | | | Min | Max |
| 01 | QL12X16B-0 | 2000 Gate CMOS FPGA | 0.39 | 1.82 |
| 02 | QL12X16B-1 | 2000 Gate CMOS FPGA | 0.39 | 1.56 |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|--------------|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|----------------|------------------------|-----------|-------------------|
| X | CMGA15-PN | 84 | Pin grid array 1/ |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Actual number of pins is 85, including one index or orientation pin (C3).

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1.3 Absolute maximum ratings. 2/

| | |
|---|-------------------------|
| Supply voltage range (V_{CC}) | -2.0 V dc to +7.0 V dc |
| Programming supply voltage range (V_{PP}) | -2.0 V dc to +13.5 V dc |
| DC input voltage range | -2.0 V dc to +7.0 V dc |
| Maximum power dissipation | 2.5 W 3/ |
| Lead temperature (soldering, 10 seconds) | +300°C |
| Thermal resistance, junction-to-case (θ_{JC}): | |
| Case outline X | 5.3° C/W |
| Junction temperature (T_J) | +175°C 4/ |
| Storage temperature range | -65°C to +150°C |
| Data retention | 10 years (minimum) |

1.4 Recommended operating conditions. 5/

| | |
|--|--|
| Case operating temperature range (T_C) | -55°C to +125°C |
| Supply voltage relative to ground (V_{CC}) | +4.5 V dc minimum to +5.5 V dc maximum |
| Ground voltage (GND) | 0 V dc |
| Input high voltage (V_{IH}) | 2.0 V dc minimum |
| Input low voltage (V_{IL}) | 0.8 V dc maximum |

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

- 2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
5/ All voltage values in this drawing are with respect to V_{SS} .

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2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JESD 78 - IC Latch-Up Test.

(Application for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

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3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.11 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract.

3.11.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.11.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.12 Data Retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process changes which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with the test data.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Delete the sequence specified as initial (pre-burn-in) electrical parameters through interim (post-burn-in) electrical parameters of method 5004 and substitute lines 1 through 5 of table IIA herein.
- b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. Test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015. Use of built-in test circuitry testing the entire lot to verify programmability and AC performance without programming the user array is an option the manufacturer may use.
- c. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

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TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions 4.5 V ≤ V _{CC} ≤ 5.5 V -55°C ≤ T _C ≤ +125°C unless otherwise specified | Group A Subgroups | Device type | Limits | | Unit |
|---|------------------|--|----------------------|----------------|--------|-----------|------|
| | | | | | Min | Max | |
| High Level output voltage | V _{OH} | V _{CC} = 4.5 V, V _{IL} = 0.8V I _{OH} = -2.0 mA, V _{IH} = 2.0 V | 1, 2, 3 | All | 2.4 | | V |
| Low level output voltage | V _{OL} | V _{CC} = 4.5 V, I _{OL} = 8.0 mA V _{IL} = 0.8 V, V _{IH} = 2.0 V | 1, 2, 3 | All | | 0.4 | V |
| High level input voltage | V _{IH} | | 1, 2, 3 | All | 2.0 | | V |
| Low level input voltage | V _{IL} | | 1, 2, 3 | All | | 0.8 | V |
| Input leakage current | I _I | V _{CC} = 5.5 V, V _{IN} = 0 V and 5.5 V | 1, 2, 3 | All | -10 | +10 | μA |
| Output leakage current | I _{OZ} | V _{CC} = 5.5 V, V _{IN} = output disabled and 5.5 V | 1, 2, 3 | All | -10 | +10 | μA |
| Output short circuit current <u>1/ 2/ 3/</u> | I _{OS} | V _{CC} = 5.5 V, V _{OUT} = V _{CC} | 1, 2, 3 | All | -10 | -80 | mA |
| | | V _{CC} = 5.5 V, V _{OUT} = GND | | | 30 | 140 | |
| Dynamic Power supply current <u>4/</u> | I _{CCD} | V _{CC} = 5.5 V, I _{OUT} = 0 mA, V _{IN} = 0 V and 5.5 V | 1, 2, 3 | All | | <u>5/</u> | mA |
| Standby Power supply current <u>4/</u> | I _{CC} | V _{CC} = 5.5 V, I _{OUT} = 0 mA, V _{IN} = 0 V and 5.5 V | 1, 2, 3 | All | | 20 | mA |
| Input capacitance <u>2/</u> | C _{IN} | See 4.4.1e | 4 | All | | 10 | pF |
| Output capacitance <u>2/</u> | C _{OUT} | See 4.4.1e | 4 | All | | 10 | pF |
| Functional test | | See 4.4.1c | 7, 8A, 8B | All | | | |

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 4.5 V ≤ V _{CC} ≤ 5.5 V -55°C ≤ T _C ≤ +125°C unless otherwise specified | Group A Subgroups | Device type | Propagation Delays with Fanout of 3/ | | | | | Unit |
|---------------------------|--------------------|---|----------------------|----------------|---|-----|-----|-----|-----|------|
| | | | | | 1 | 2 | 3 | 4 | 8 | |
| Logic cells | | | | | | | | | | |
| Combinatorial Delay 5/ | t _{PD} | See figure 3 | 9, 10, 11 | All | 1.7 | 2.2 | 2.6 | 3.2 | 5.2 | ns |
| Set-up time 5/ | t _{SU} | | | | 2.1 | 2.1 | 2.1 | 2.1 | 2.1 | |
| Hold time | t _H | | | | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | |
| Clock to Q delay | t _{CLK} | | | | 1.0 | 1.5 | 1.9 | 2.5 | 4.6 | |
| Clock HIGH time | t _{CWHI} | | | | 2.0 | 2.0 | 2.0 | 2.0 | 2.0 | |
| Clock LOW time | t _{CWLO} | | | | 2.0 | 2.0 | 2.0 | 2.0 | 2.0 | |
| Set delay | t _{SET} | | | | 1.7 | 2.1 | 2.6 | 3.2 | 5.2 | |
| Reset delay | t _{RESET} | | | | 1.5 | 1.9 | 2.2 | 2.7 | 4.3 | |
| Set width | t _{SW} | | | | 1.9 | 1.9 | 1.9 | 1.9 | 1.9 | |
| Reset width | t _{RW} | | | | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | |

See footnotes at end of table.

| Test | Symbol | Conditions 4.5 V ≤ V _{CC} ≤ 5.5 V -55°C ≤ T _C ≤ +125°C unless otherwise specified | Group A Subgroups | Device type | Propagation Delays with Fanout of 3/ | | | | | | Unit |
|--|--------------------|---|----------------------|----------------|---|-----|-----|-----|-----|-----|------|
| | | | | | 1 | 2 | 3 | 4 | 6 | 8 | |
| Input cells | | | | | | | | | | | |
| Input delay (HIGH DRIVE) | t _{IN} | See figure 3 | 9, 10, 11 | All | 2.4 | 2.5 | 2.6 | 2.7 | 3.0 | 3.3 | ns |
| Input Inverting delay (HIGH DRIVE) | t _{INI} | | | | 2.5 | 2.6 | 2.7 | 2.8 | 3.1 | 3.4 | |
| Input Delay (Bidirectional Pad) | t _{IO} | | | | 1.4 | 1.9 | 2.2 | 2.8 | 3.7 | 4.6 | |
| Clock Buffer delay 6/ | t _{GCK} | | | | 2.7 | 2.8 | 2.8 | 2.9 | 2.9 | 3.0 | |
| Clock Buffer minimum HIGH 6/ | t _{GCKHI} | | | | 2.0 | 2.0 | 2.0 | 2.0 | 2.0 | 2.0 | |
| Clock Buffer minimum LOW 6/ | t _{GCKLO} | | | | 2.0 | 2.0 | 2.0 | 2.0 | 2.0 | 2.0 | |

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 4.5 V ≤ V _{CC} ≤ 5.5 V -55°C ≤ T _C ≤ +125°C unless otherwise specified | Group A Subgroups | Device type | Propagation Delays with Output load capacitance (pF) of <u>3</u> / ₁ | | | | | Unit |
|--|--------------------|---|----------------------|----------------|---|-----|-----|-----|-----|------|
| | | | | | 30 | 50 | 75 | 100 | 150 | |
| Output cells | | | | | | | | | | |
| Output delay LOW TO HIGH | t _{OUTLH} | See figure 3 | 9, 10, 11 | All | 2.7 | 3.4 | 4.2 | 5.0 | 6.7 | ns |
| Output delay HIGH to LOW | t _{OUTHL} | | | | 2.8 | 3.7 | 4.7 | 5.6 | 7.6 | |
| Output delay three-state to HIGH | t _{PZH} | | | | 4.0 | 4.9 | 6.1 | 7.3 | 9.7 | |
| Output delay three-state to LOW | t _{PZL} | | | | 3.6 | 4.2 | 5.0 | 5.8 | 7.3 | |
| Output delay HIGH to three- state (figure 3) | t _{PHZ} | | | | 2.9 | | | | | |
| Output delay LOW to three- state (figure 3) | t _{PLZ} | | | | 3.3 | | | | | |

High Drive Buffer:

| Test | Symbol | Conditions 4.5 V ≤ V _{CC} ≤ 5.5 V -55°C ≤ T _C ≤ +125°C unless otherwise specified | Group A Subgroups | Device type | # High Drives Wired together | Propagation Delays with Fanout of <u>3</u> / ₁ | | | | | Unit |
|--|------------------|---|----------------------|----------------|---------------------------------------|--|-----|-----|-----|-----|------|
| | | | | | | 12 | 24 | 48 | 72 | 96 | |
| High drive Input delay | t _{IN} | See figure 3 | 9, 10, 11 | All | 1 | 4.5 | 5.4 | | | | ns |
| | | | | | 2 | | 3.4 | 5.6 | | | |
| | | | | | 3 | | | 4.5 | 5.3 | 6.3 | |
| | | | | | 4 | | | | 4.6 | 5.3 | |
| High drive Input, Inverting delay | t _{INI} | See figure 3 | 9, 10, 11 | All | 1 | 4.7 | 5.6 | | | | ns |
| | | | | | 2 | | 4.0 | 5.8 | | | |
| | | | | | 3 | | | 4.6 | 5.5 | 6.4 | |
| | | | | | 4 | | | | 4.8 | 5.5 | |

1/ Only one output at a time. Duration should not exceed 30 seconds.

2/ C₁ = 20 pF max on I(SI) and I(P).

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TABLE I. Electrical performance characteristics - Continued.

3/ Worst case propagation delay times over process variation at $V_{CC} = 5.0$ V and $T_A = 25^\circ\text{C}$. Multiply by the appropriate delay factor, K (see 1.2.2), for speed grade to get worst case parameters over the full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3 ns linear transition time between 0 and 3 volts.

| | | |
|----|------------------------------------|-------------|
| 4/ | 1 CLB driving a 15 pF load | 0.38 mW/MHz |
| | 1 clock buffer | 0.36 mW/MHz |
| | 1 clock col buffer | 0.08 mW/MHz |
| | 1 clock load | 0.02 mW/MHz |
| | 1 macro cell driving a fanout of 4 | 0.44 mW/MHz |

5/ These limits are derived from worst case values for a representative selection of the slowest paths through the device logic cell including net delays. Guaranteed delay values for specific programmed part should be determined from simulation results.

6/ Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For device class M subgroups 7, 8A and 8B tests shall consist of verifying functionality of the device. These tests form a part of the vendors test tape and shall be maintained and available upon request. For device classes Q and V subgroups 7, 8A and 8B shall include verifying the functionality of the device.
- d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 3 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 78 may be used for reference.
- e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is three devices with no failures, and all input and output terminals tested.

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4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- b. $T_A = +125^{\circ}\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

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Case outline X

| Device type | All |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Terminal number | Terminal symbol |
| A1 | I/O | C1 | I/O | F9 | I/O | K2 | I/O |
| A2 | I/O | C2 | I/O | F10 | I/O | K3 | I/O |
| A3 | I/O | C3 | orientation pin | F11 | I/O | K4 | I/O |
| A4 | I/O | C5 | V _{CC} | G1 | I/O | K5 | I/(S1) |
| A5 | I/O | C6 | I/CLK/(SM) | G2 | I/O | K6 | I |
| A6 | I/O | C7 | GND | G3 | V _{CC} | K7 | I/(S0) |
| A7 | I/O | C10 | I/O | G9 | GND | K8 | I/O |
| A8 | I/O | C11 | I/O | G10 | I/O | K9 | I/O |
| A9 | I/O | D1 | I/O | G11 | I/O | K10 | I/O |
| A10 | I/O | D2 | I/O | H1 | I/O | K11 | I/O |
| A11 | I/O | D10 | I/O | H2 | I/O | L1 | I/O |
| B1 | I/O | D11 | I/O | H10 | I/O | L2 | I/O |
| B2 | I/O | E1 | I/O | H11 | I/O | L3 | I/O |
| B3 | I/O | E2 | I/O | J1 | I/O | L4 | I/O |
| B4 | I/O | E3 | GND | J2 | I/O | L5 | I/O |
| B5 | I | E9 | V _{CC} | J5 | GND | L6 | I/O |
| B6 | I(P) | E10 | I/O | J6 | I/CLK | L7 | I/O |
| B7 | I/(SCLK) | E11 | I/O | J7 | V _{CC} | L8 | I/O |
| B8 | I/O | F1 | I/O | J10 | I/O | L9 | I/O |
| B9 | I/O | F2 | I/O | J11 | I/O | L10 | I/O |
| B10 | I/O | F3 | I/O | K1 | I/O | L11 | I/O |
| B11 | I/O | | | | | | |

FIGURE 1. Terminal connections.

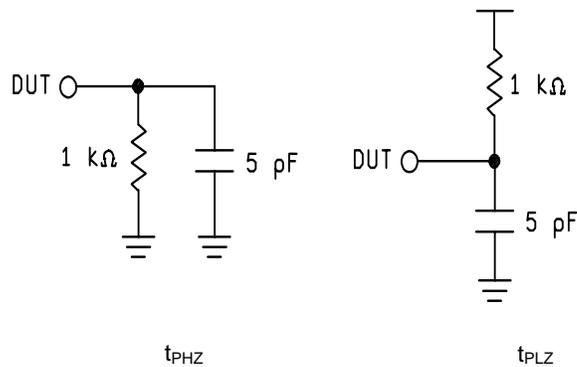


FIGURE 2. Output load circuits and test conditions.

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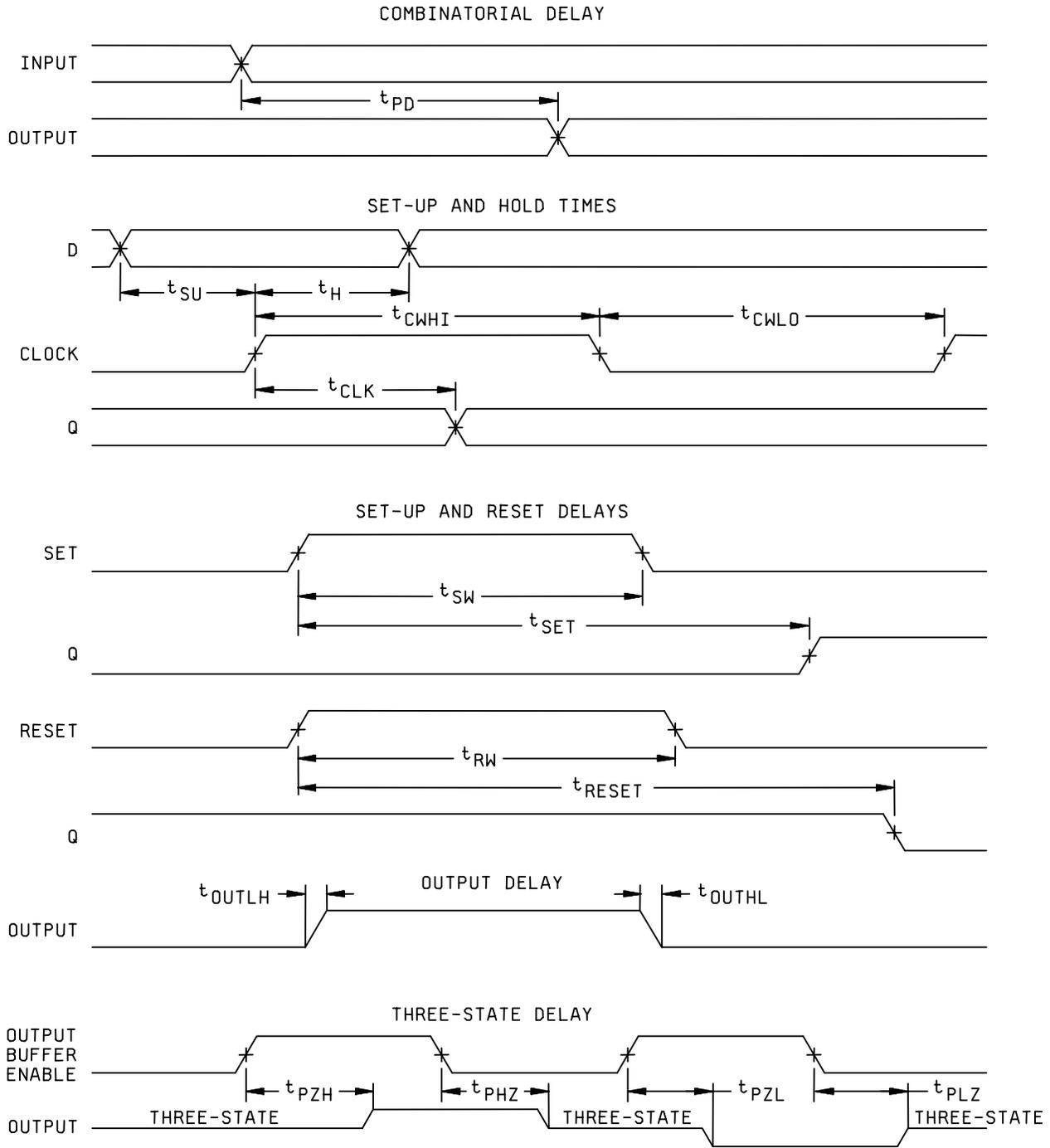


FIGURE 3. Switching waveforms.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

| Line no. | Test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|----------|---|--|---|------------------------------------|
| | | Device class M | Device class Q | Device class V |
| 1 | Interim electrical parameters (see 4.2) | | 1, 7, 9 | 1, 7, 9 or 2, 8A, 10 |
| 2 | Static burn-in (method 1015) | Not Required | Not Required | Required |
| 3 | Same as line 1 | | | 1*,7* Δ |
| 4 | Dynamic burn-in (method 1015) | Required | Required | Required |
| 5 | Final electrical parameters | 1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 | 1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 | 1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 |
| 6 | Group A test requirements | 1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 | 1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 | 1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 |
| 7 | Group C end-point electrical parameters | 2, 3, 7, 8A, 8B | 2, 3, 7, 8A,8B | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ |
| 8 | Group D end-point electrical parameters | 2, 3, 8A, 8B | 2, 3, 8A, 8B | 2, 3, 8A, 8B |
| 9 | Group E end-point electrical parameters | 1, 7, 9 | 1, 7, 9 | 1, 7, 9 |

- 1/ Blank spaces indicate tests are not applicable.
- 2/ Any or all subgroups may be combined when using high-speed testers.
- 3/ Subgroups 7 and 8 functional tests shall verify the truth table.
- 4/ * indicates PDA applies to subgroup 1 and 7.
- 5/ ** see 4.4.1e.
- 6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
- 7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

| Parameter 1/ | Device types |
|--------------|-------------------------------------|
| | All |
| I_{oz} | ±10% of specified value in table I. |
| I_l | ±10% of specified value in table I. |

- 1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

| | | | |
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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

| | | | |
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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-05-08

Approved sources of supply for SMD 5962-96836 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|-----------------------|--------------------------|
| 5962-9683601MXC | 0WGG6 | QL12X16B-0C84M/883C |
| 5962-9683602MXC | 0WGG6 | QL12X16B-1C84M/883C |

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

0WGG6

Vendor name
and address

QuickLogic Corporation
1277 Orleans Drive
Sunnyvale, CA 94089-1138

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.