REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21													
REV STATUS OF SHEETS				REV																
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
96-10-15

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 42316-5000

MICROCIRCUIT DIE, MEMORY, DIGITAL, CMOS, 4M X 1 DYNAMIC RANDOM ACCESS MEMORY (DRAM), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-96889**

SHEET 1 OF 21

DESC FORM 193
JUL 94

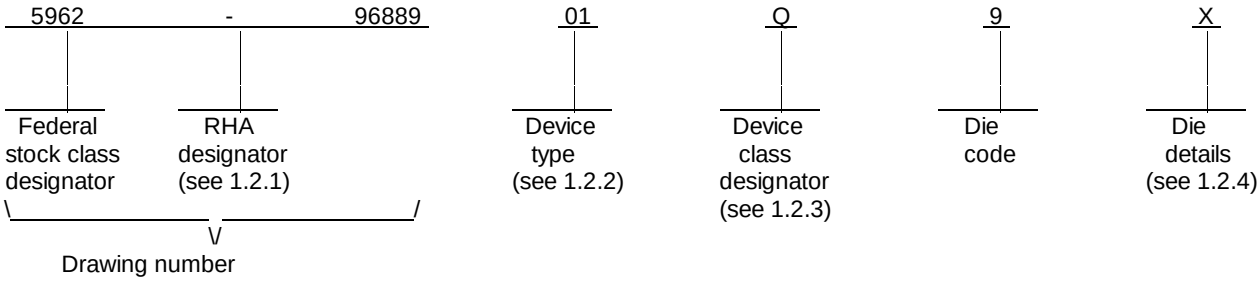
5962-E521-96

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high-reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels shall be reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	MT4C1004JD37M	4 MEG X 1 DRAM Die (5 V)	60 ns
02	MT4C1004JD37M	4 MEG X 1 DRAM Die (5 V)	70 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the die's product assurance level as follows:

Die class	Die requirements documentation
Q or V	Certification and qualification to die requirements of MIL-PRF-38535

1.2.4 Die details. The die details designator shall be a unique letter which identifies the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information for each product and variant supplied to this drawing.

1.2.4.1 Die physical dimensions.

Die type	Figure number
01	1
02	1

1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	1
02	1

1.2.4.3 Interface materials.

Die type	Figure number
01	1
02	1

1.2.4.4 Assembly related information.

Die type	Figure number
01	1
02	1

1.3 Absolute maximum ratings. 1/

Voltage on any pin relative to V_{SS} . . . . . - 1 V to + 7 V
Operating Temperature T_A ambient . . . . . 0°C to 70°C
Storage temperature . . . . . -55°C to +150°C
Power Dissipation . . . . . 1 W
Short circuit output current . . . . . 50 mA

1.4 Recommended operating conditions.

Supply voltage . . . . . 4.5 V to 5.5 V

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration management

HANDBOOK

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit and function of the die as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan for device classes Q and V and herein.

3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in 1.2.4.1 and on figure 1.

3.2.2 Die bonding pad locations. The die bonding pad locations shall be as specified in 1.2.4.2 and on figure 1.

3.2.3 Interface materials. The interface materials for the die shall be as specified in 1.2.4.3 and on figure 1.

3.2.4 Assembly related information. The assembly related information shall be as specified in 1.2.4.4 and on figure 1.

3.2.5 Truth table(s). The truth table shall be as specified on figure 2.

3.2.6 Timing waveforms. The timing waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits of the die are as specified in table I.

3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements of table I. Waferprobe speed sorting is available upon request by the customer.

3.5 Marking. As a minimum, each unique lot of die, loaded in a single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, a date code, the certification mark, the manufacturer's identification and the PIN specified in 1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

3.6 Certificate of compliance. For die classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for die classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance shall be required for device classes Q and V in accordance with the applicable requirements of MIL-PRF-38535 and shall be provided with each lot of microcircuit die delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures including screening and conformance inspection shall be in accordance with the applicable requirements of MIL-PRF-38535 for die or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function of the die as described herein.

4.2 Qualification inspection for die classes Q and V. For die classes Q and V, qualification inspection shall be in accordance with the applicable die requirements of MIL-PRF-38535. Die inspections to be performed shall be those specified in MIL-PRF-38535 and in the manufacturer's QM plan.

4.3 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

4.3.1 Wafer lot acceptance for class V. Wafer lot acceptance for class V product shall use the criteria of test method 5007 of MIL-STD-883 or an equivalent method approved by the qualifying activity.

4.3.2 Wafer probe. 100 percent wafer probe shall be required in accordance with 3.4 herein.

4.3.3 Internal visual. 100 percent internal visual inspection to the applicable class Q or V criteria of test method 2010 of MIL-STD-883 or an alternate procedures allowed in method 5004 of MIL-STD-883 or an inspection methodology approved by the qualifying activity.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $0°C \le T_C \le +70°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Notes	Device Type	Limits		Unit
					Min	Max	
Supply voltage	V_{CC}		1/ 3/ 5/ 6/	All	4.5	5.5	V
Input high voltage	V_{IH}		1/ 3/ 5/ 6/	All	2.4	V_{CC} + 1	V
Input low voltage	V_{IL}		1/ 3/ 5/ 6/	All	-1.0	0.8	V
Input leakage current	I_I	Any input $0\ V \le V_{IN} \le 6.5\ V$ All other pins not under test = 0 V	1/ 3/ 5/ 6/	All	-2	2	µA
Output leakage current	I_{OZ}	Q is disabled $0\ V \le V_{OUT} \le 5.5\ V$	1/ 3/ 5/ 6/	All	-10	10	µA
Output high voltage	V_{OH}	I_{OUT} = -5 mA	1/ 3/ 5/ 6/	All	2.4		V
Output low voltage	V_{OL}	I_{OUT} = 4.2 mA	1/ 3/ 5/ 6/	All		0.4	V
Standby current (TTL)	I_{CC1}	$\overline{RAS} = \overline{CAS} = V_{IH}$		All		2	mA
Standby current (CMOS)	I_{CC2}	$\overline{RAS} = \overline{CAS} = V_{CC}$ - 0.2 V		All		1	mA
Operating current (random read/write)	I_{CC3}	$\overline{RAS}$, $\overline{CAS}$ single address cycling, $t_{RC} = t_{RC}$ (min)	3/ 25/	01		110	mA
				02		100	
Operating current (fast page mode)	I_{CC4}	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ address cycling, $t_{RC} = t_{RC}$ (min)	3/ 25/	01		80	mA
				02		70	
Refresh current $\overline{RAS}$ only	I_{CC5}	$\overline{RAS}$ cycling, $\overline{CAS}$ = VIH, $t_{RC} = t_{RC}$ (min)	3/ 25/	01		110	mA
				02		100	
Refresh current CBR	I_{CC6}	$\overline{RAS}$, $\overline{CAS}$, address cycling, $t_{RC} = t_{RC}$ (min)	3/ 4/	01		110	mA
				02		100	
Input capacitance, A0-A10, D	C_{I1}		2/	All		5	pF
Input capacitance, $\overline{RAS}$ $\overline{CAS}$, $\overline{WE}$	C_{I2}		2/	All		7	pF
Output capacitance	C_O		2/	All		7	pF
Random read or write cycle time	t_{RC}	5/ 6/ 7/ 8/ 9/ 10/ 11/ 12/		01	110		ns
				02	130		
Read-write cycle time	t_{RWC}			01	130		ns
				02	155		
Fast page mode read or write cycle time	t_{PC}			01	35		ns
				02	40		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $0°C \le T_C \le +70°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Notes	Device Type	Limits		Unit
					Min	Max	
Fast page mode read-write cycle time	t_{PRWC}	5/ 6/ 7/ 8/ 9/ 10/ 11/ 12/		01	60		ns
				02	70		
Access time from $\overline{RAS}$	t_{RAC}		13/	01		60	ns
				02		70	
Access time from $\overline{CAS}$	t_{CAC}		14/	01		15	ns
				02		20	
Access time from column address	t_{AA}			01		30	ns
				02		35	
Access time from $\overline{CAS}$ precharge	t_{CPA}			01		35	ns
				02		40	
$\overline{RAS}$ pulse width	t_{RAS}		23/	01	60	10,000	ns
				02	70	10,000	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}		23/	01	60	100,000	ns
				02	70	100,000	
$\overline{RAS}$ hold time	t_{RSH}			01	15		ns
				02	20		
$\overline{RAS}$ precharge time	t_{RP}			01	40		ns
				02	50		
$\overline{CAS}$ pulse width	t_{CAS}			01	15	10,000	ns
				02	20	10,000	
$\overline{CAS}$ hold time	t_{CSH}			01	60		ns
				02	70		
$\overline{CAS}$ precharge time (CBR refresh)	t_{CPN}			All	10		ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}		15/	All	10		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}		16/	01	20	45	ns
				02	20	50	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}			All	10		ns
Row address setup time	t_{ASR}			All	0		ns
Row address hold time	t_{RAH}			All	10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $0°C \le T_C \le +70°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Notes	Device Type	Limits		Unit
					Min	Max	
$\overline{RAS}$ to column address delay time	t_{RAD}	5/ 6/ 7/ 8/ 9/ 10/ 11/ 12/	17/	01	15	30	ns
				02	15	35	
Column address setup time	t_{ASC}			All	0		ns
Column address hold time	t_{CAH}			01	10		ns
				02	15		
Column address hold time referenced to $\overline{RAS}$	t_{AR}			01	45		ns
				02	50		
Column address to $\overline{RAS}$ lead time	t_{RAL}			01	30		ns
				02	35		
Read command setup time	t_{RCS}			01	0		ns
				02	0		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}		18/	01	0		ns
				02	0		
Read command hold time referenced to $\overline{RAS}$	t_{RRH}		18/	01	0		ns
				02	0		
$\overline{CAS}$ to output in low Z	t_{CLZ}			01	0		ns
				02	0		
Output buffer turn-off delay	t_{OFF}		19/ 24/	01	3	15	ns
				02	3	20	
$\overline{WE}$ command setup time	t_{WCS}			All	0		ns
Write command hold time	t_{WCH}			01	10		ns
				02	15		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}			01	45		ns
				02	55		
Write command pulse width	t_{WP}			01	10		ns
				02	15		
Write command to $\overline{RAS}$ lead time	t_{RWL}			01	15		ns
				02	20		
Write command to $\overline{CAS}$ lead time	t_{CWL}			01	15		ns
				02	20		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

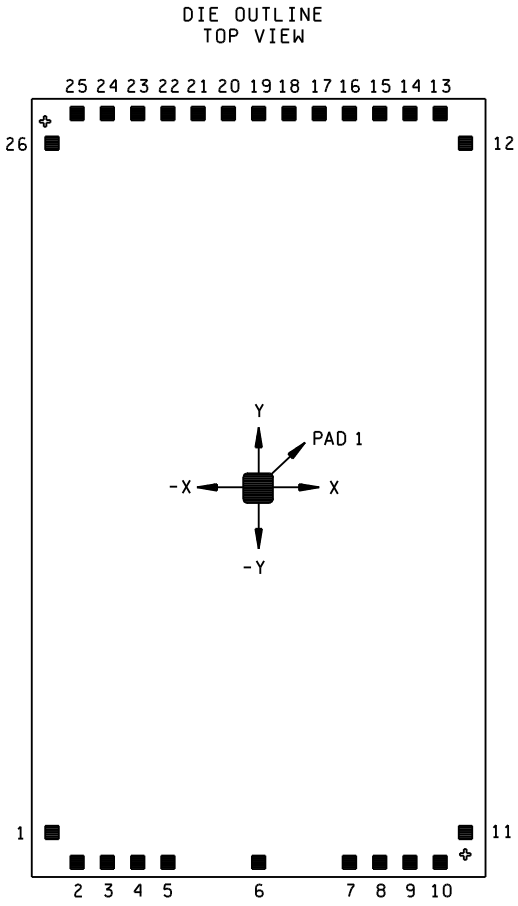
Test	Symbol	Conditions $0°C \le T_C \le +70°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Notes	Device Type	Limits		Unit
					Min	Max	
Data-in setup time	t_{DS}	5/ 6/ 7/ 8/ 9/ 10/ 11/ 12/	21/	All	0		ns
Data-in hold time	t_{DH}		21/	01	10		ns
				02	15		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}			01	45		ns
				02	55		
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}		20/	01	60		ns
				02	70		
Column address to $\overline{WE}$ delay time	t_{AWD}		20/	01	30		ns
				02	35		
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}		20/	01	15		ns
				02	20		
Transition time (rise and fall)	t_T			All	3	50	ns
Refresh period (1,024 cycles)	t_{REF}			All	16		ms
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}			01	0		ns
$\overline{CAS}$ setup time CBR refresh	t_{CSR}		4/	01	10		ns
$\overline{CAS}$ hold time CBR refresh	t_{CHR}		4/	01	10		ns
$\overline{WE}$ hold time CBR refresh	t_{WRH}		22/	01	10		ns
$\overline{WE}$ setup time CBR refresh	t_{WRP}		22/	01	10		ns

1/ All voltages referenced to V_{SS}.
2/ This parameter is sampled. V_{CC} = 5 V ±10%, f = 1 Mhz. Also, these capacitance values are based on the die packaged in a plastic SOJ. Bare die is approximately 1 pF lower.
3/ I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
4/ Enables on-chip refresh and address counters.
5/ The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
6/ An initial pause of 100 μs is required after power up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-only or CBR with $\overline{WE}$ high) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake ups should be repeated any time the t_{REF} refresh requirement is exceeded.
7/ AC characteristics assume t_T = 5ns.
8/ V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).

9/ In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10/ If $\overline{CAS}$ = V_{IH}, data output is high-Z.
11/ If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid read cycle.
12/ Measured with a load equivalent to two TTL gates and 100 pF.
13/ Assumes that $t_{RCD} < t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
14/ Assume that $t_{RCD} \geq t_{RCD}$ (max).
15/ If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$,Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed high for t_{CPN}.
16/ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
17/ Operation within the t_{RAD} (max) limit ensures that t_{RAC} (min) and t_{CAC} (min) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
18/ Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
19/ t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
20/ t_{WCS}, t_{RWD}, t_{AWD}, and t_{CWD} are restrictive operating parameters in late write, read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early-write cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a late-write and the state of data-out is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
21/ These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and $\overline{WE}$ leading edge in late write or read-write cycles.
22/ A hidden refresh may also be performed after a write cycle. In this case, $\overline{WE}$ = low.
23/ BBU current is reduced as t_{RAS} is reduced from its maximum specification during the BBU cycle.
24/ The 3 ns minimum is a parameter guaranteed by design.
25/ Column-address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

Bond Pad Location and Identification Table			
		From Center of #1	
Pad #	Function	"X"	"Y"
		microns	microns
1	A9	0.00	0.00
2	$\overline{CAS}$	106.7	-220.5
3	DNU	425.0	-220.6
4	DOUT	716.7	-220.6
5	VSS	1262.4	-225.1
6	VSS	1414.8	-225.1
7	DIN	1704.4	-220.6
8	DNU	1996.2	-220.6
9	$\overline{WE}$	2319.1	-220.5
10	$\overline{RAS}$	2612.6	-220.5
11	A10	2714.4	7.6
12	A0	2724.3	4880.3
13	A1	2623.7	5060.9
14	A2	2401.0	5060.9
15	DNU	2098.8	5061.1
16	A3	1949.4	5060.9
17	DNU	1749.0	5060.9
18	DNU	1529.7	5061.1
19	VCC	1389.4	5061.5
20	VCC	1214.2	5060.1
21	VBB	1000.4	5060.1
22	A4	799.9	5060.9
23	A5	578.6	5060.9
24	A6	338.8	5060.9
25	A7	97.9	5060.9
26	A8	-3.9	4858.8

NOTE: DNU stands for "do not use".



Wafer diameter:	200 mm
Wafer thickness:	0.47 ± 0.0125 mm
Die size:	5.613 x 3.048 mm
(stepping interval)	
Bond pad size:	.124 x .124 mm
Passivation openings:	.114 x .114 mm
(Typical)	
Bond pad material:	99.5% Al and 0.5% Cu
Backside material:	Polished bare silicon

FIGURE 1. Die details.

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses		Data	
					t_R	t_C	D (Data in)	Q (Data out)
Standby		H	H→X	X	X	X	X	High Z
Read		L	L	H	ROW	COL	X	Data out
Early write		L	L	L	ROW	COL	Data in	High Z
Read write		L	L	H→L	ROW	COL	Data in	Data out
Fast-page-mode read	1st cycle	L	H→L	H	ROW	COL	X	Data out
	2nd cycle	L	H→L	H	N/A	COL	X	Data out
Fast-page-mode early-write	1st cycle	L	H→L	L	ROW	COL	Data in	High Z
	2nd cycle	L	H→L	L	N/A	COL	Data in	High Z
Fast-page-mode read-write	1st cycle	L	H→L	H→L	ROW	COL	Data in	Data out
	2nd cycle	L	H→L	H→L	N/A	COL	Data in	Data out
$\overline{RAS}$-only refresh		L	H	X	ROW	N/A	X	High Z
Hidden refresh	Read	L	L	H	ROW	COL	X	Data out
	Write	L	L	L	ROW	COL	Data in	High Z
CBR refresh		L	L	H	X	X	X	High Z

FIGURE 2. Truth table.

Read cycle

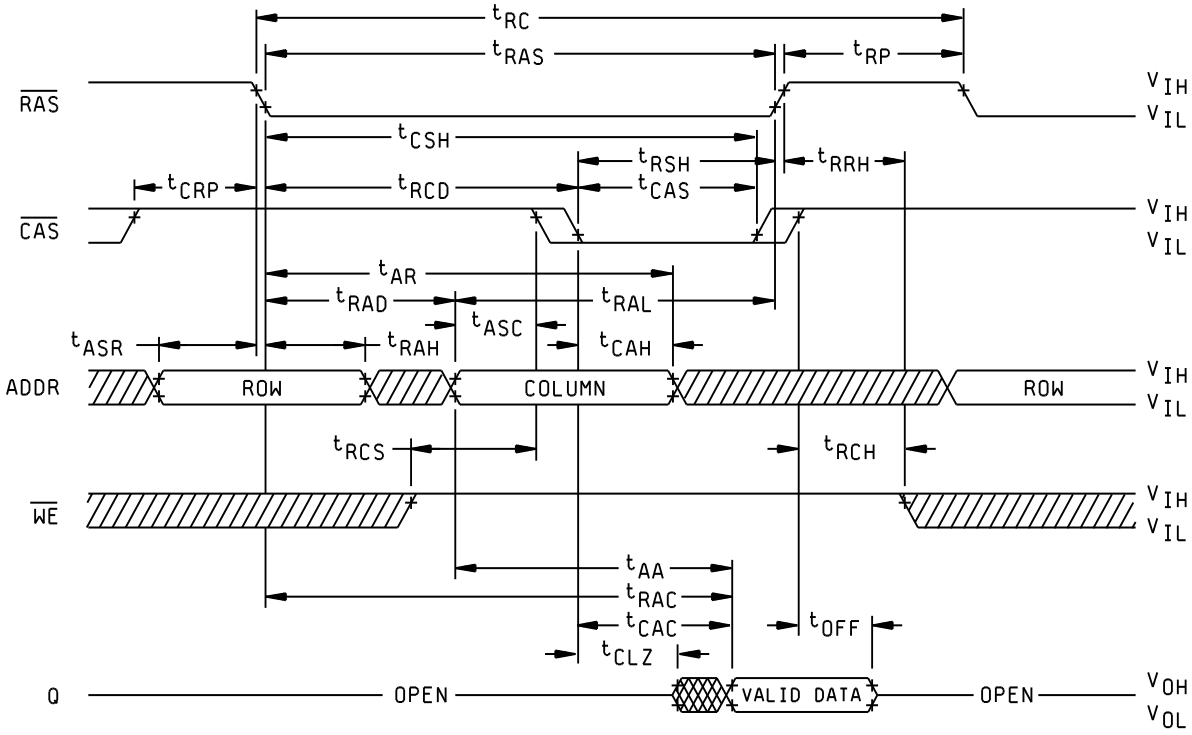


FIGURE 3. Timing waveforms.

Early write cycle

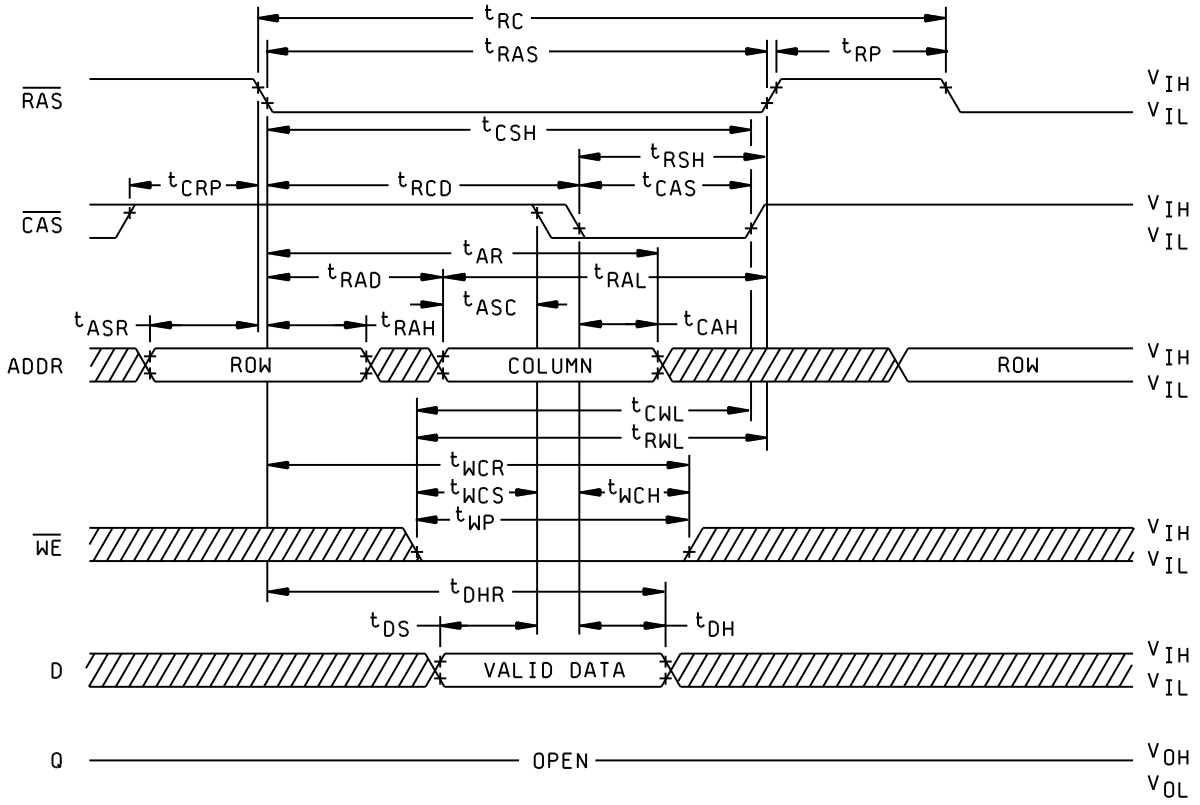


FIGURE 3. Timing waveforms - continued.

Read write cycle
(Late write and read-modify-write cycles)

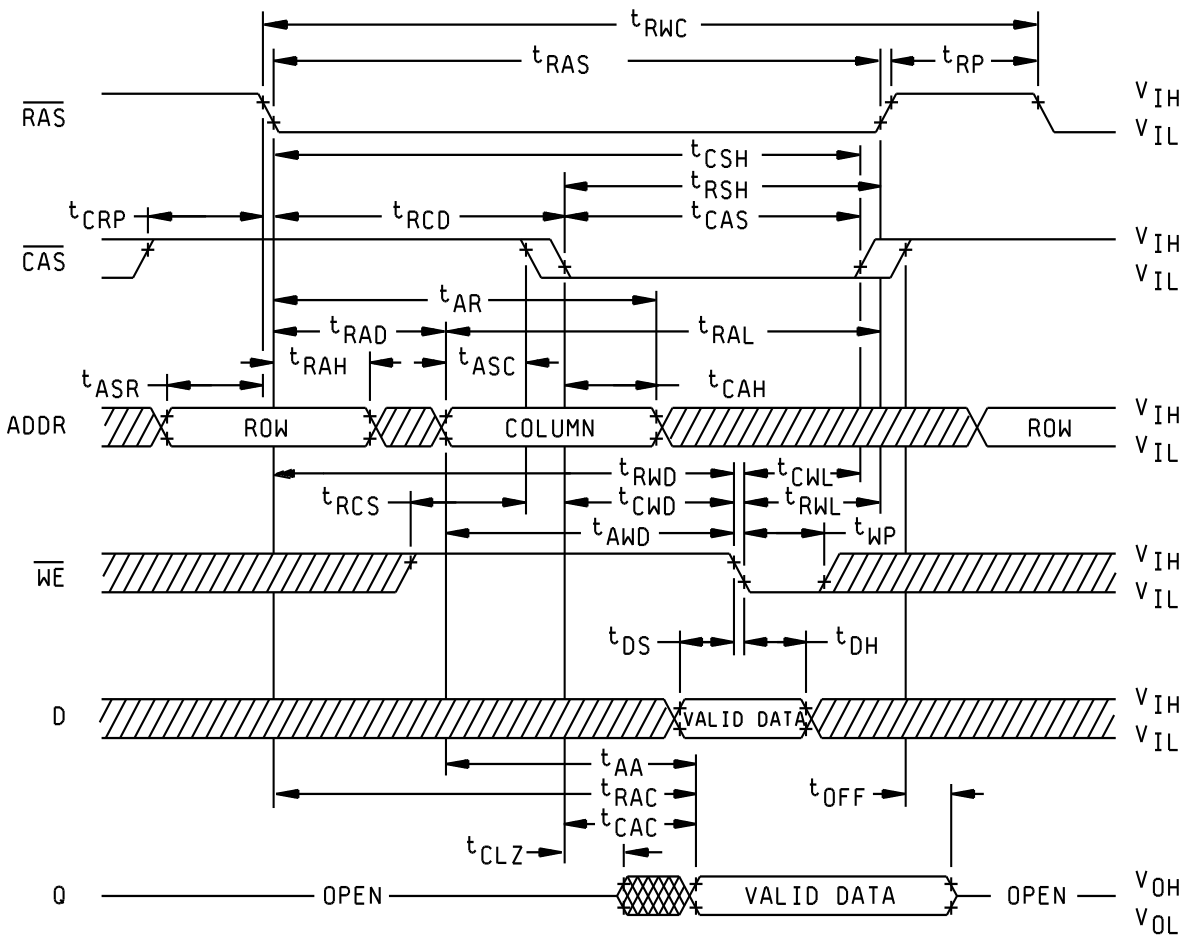


FIGURE 3. Timing waveforms - continued.

Fast-page-mode read cycle

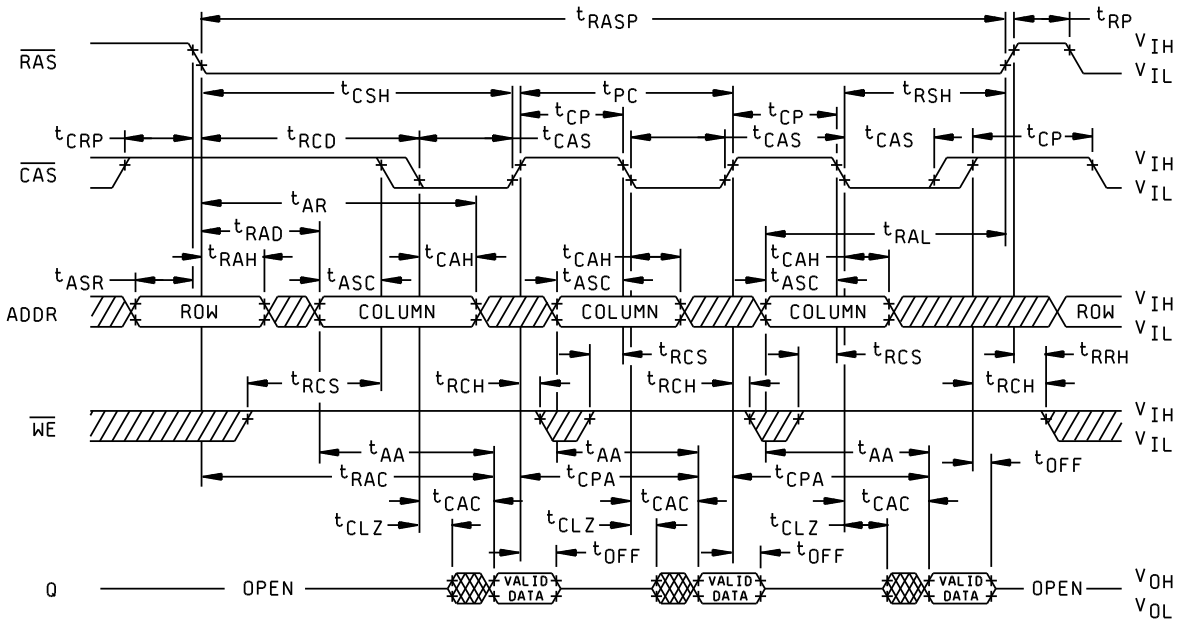


FIGURE 3. Timing waveforms - continued.

Fast-page-mode early-write cycle

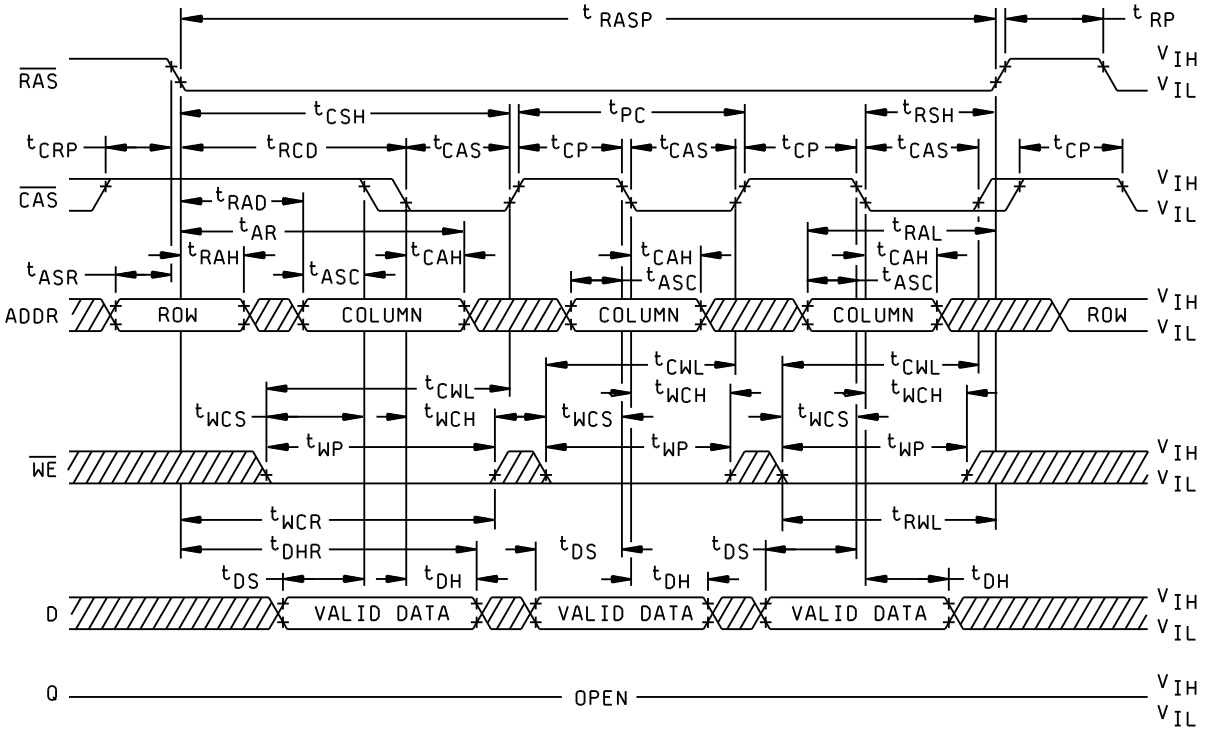
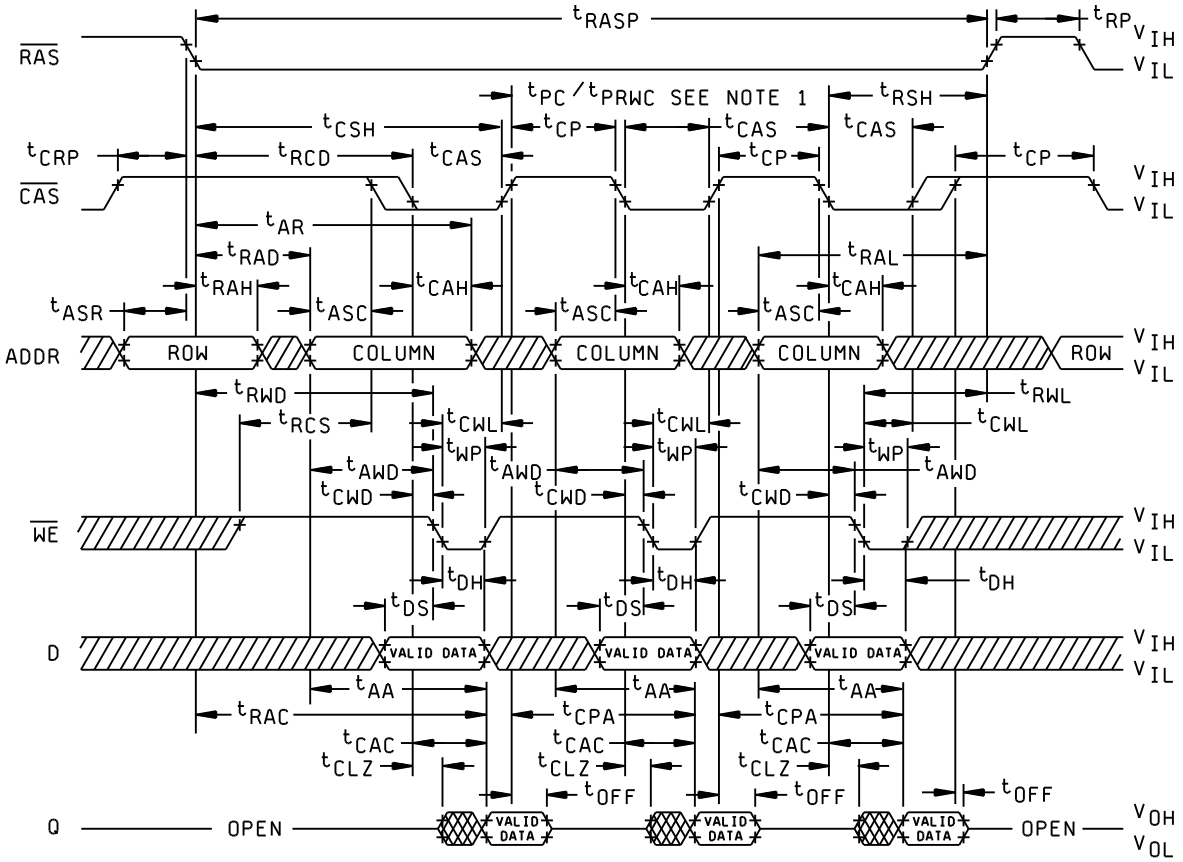


FIGURE 3. Timing waveforms - continued.

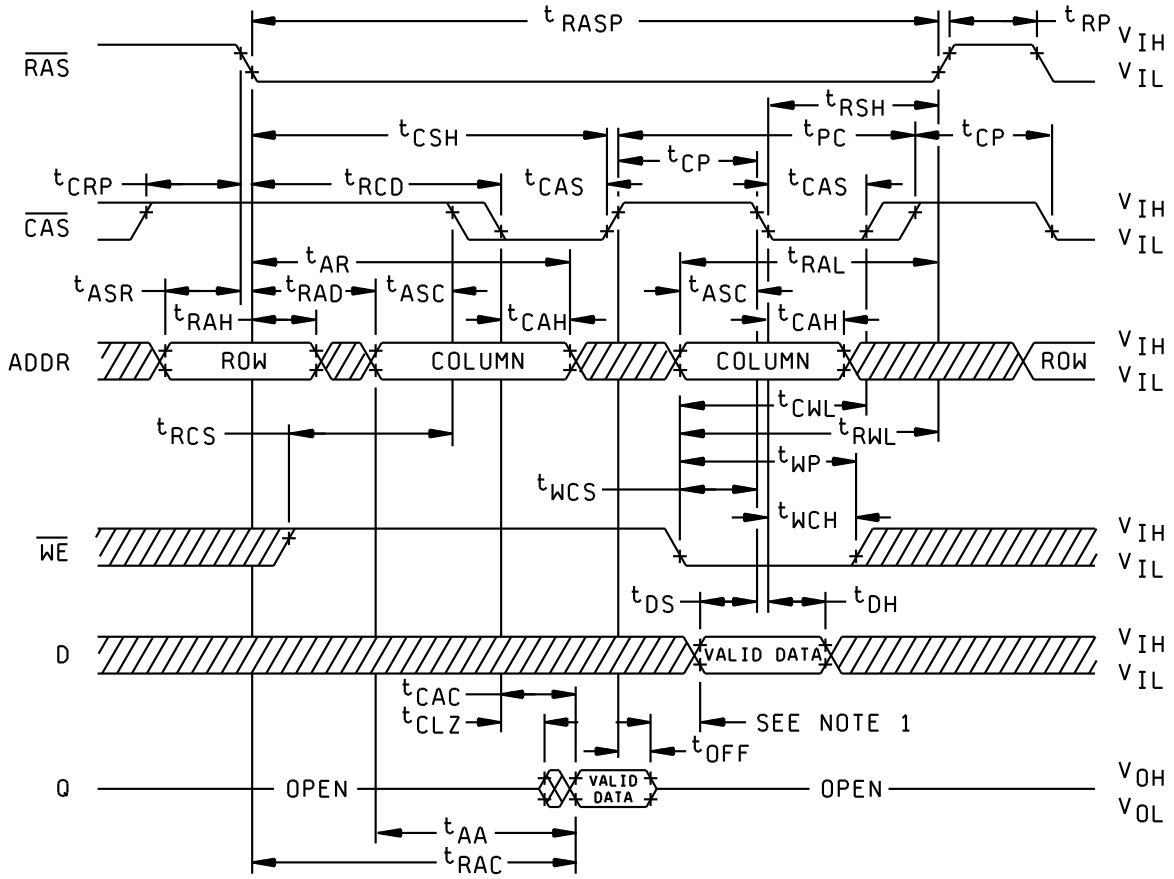
Fast-page-mode read-write cycle
(Late write and read-modify-write cycles)



NOTE: t_{PC} is for late write only.

FIGURE 3. Timing waveforms - continued.

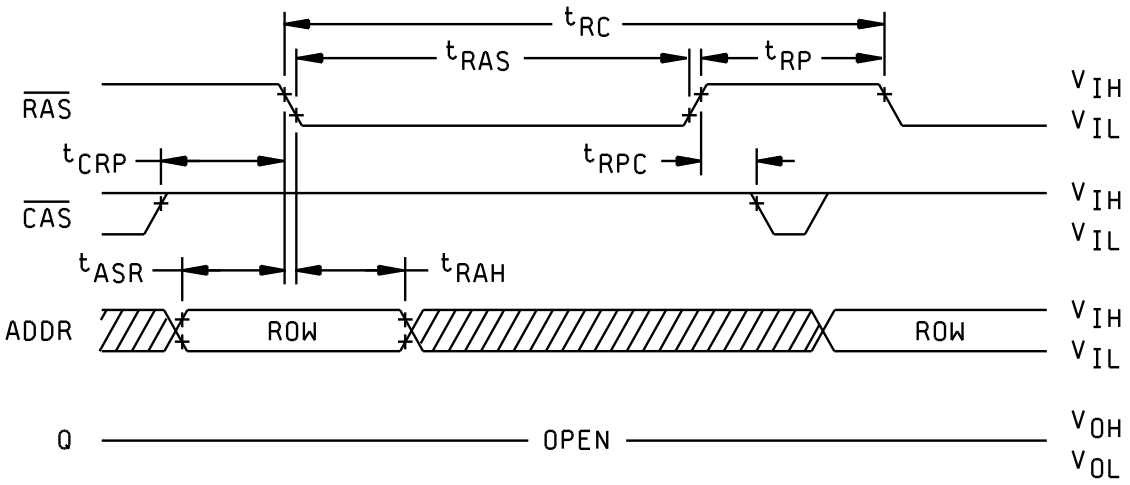
Fast-page-mode read-early-write cycle



NOTE: 1. Do not drive data prior to tri-state; assume D and Q are tied together.

FIGURE 3. Timing waveforms - continued.

$\overline{RAS}$-only refresh cycle
($\overline{WE}$ and A10 = don't care)



CBR refresh cycle
(Addresses = don't care)

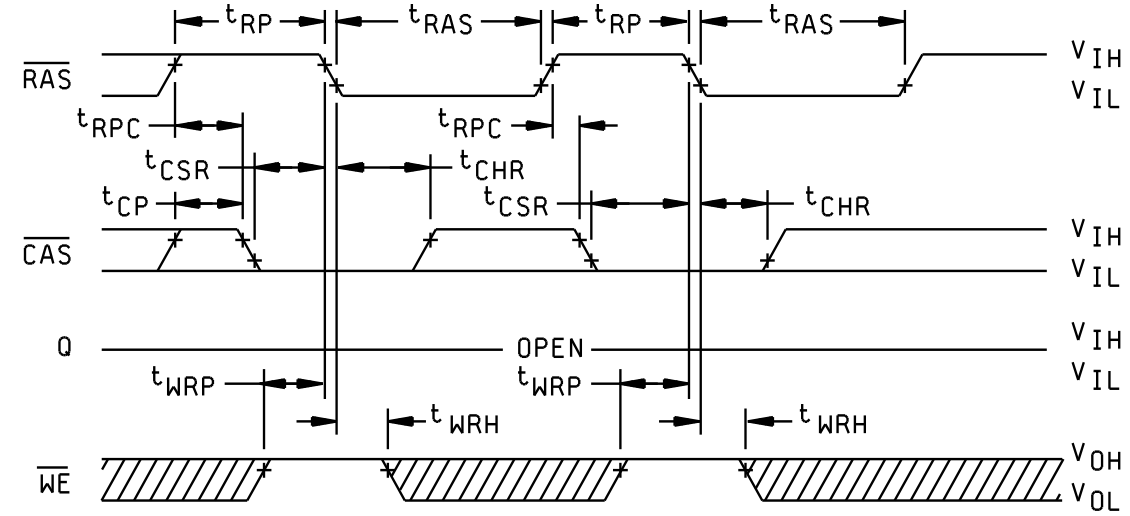


FIGURE 3. Timing waveforms - continued.

Hidden refresh cycle
($\overline{WE}$ = high)

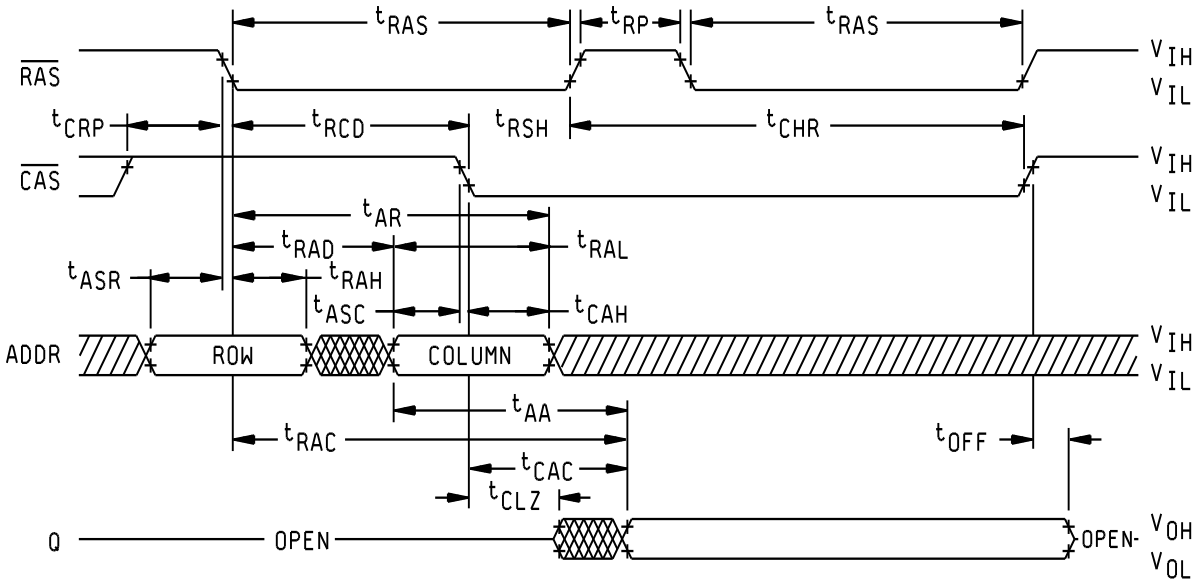


FIGURE 3. Timing waveforms - continued.

4.4 Conformance inspection.

4.4.1 Group E inspection. Group E inspection is required for parts intended to be identified as radiation hardness assured (see 3.5 herein). RHA levels for die classes Q and V shall be as specified in MIL-PRF-38535.

4.4.1.1 Endpoint electricals. Endpoint electrical testing of packaged die shall be as specified in table I herein.

4.4.1.2 RHA testing. For die classes Q and V, the die or test vehicles shall be subjected to radiation hardness assurance tests as specified in MIL-PRF-38535 for the RHA level being tested. All die shall meet the postirradiation endpoint electrical parameter limits as specified in table I at T_A = +25°C + 5°C after exposure.

4.4.1.3 RHA delta limits. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. DIE CARRIER

5.1 Die carrier requirements. The requirements for the die carrier shall be in accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

6. NOTES

6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 42316-5000, or telephone (614) 692-0674.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING DIE SOURCE APPROVAL BULLETIN

DATE: 96-10-15

Approved sources of supply for SMD 5962-96889 are listed below for immediate acquisition only and shall be added to QML-38535 during the next revision. QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38535.

Standard microcircuit die drawing PIN	Vendor CAGE number	Vendor similar die PIN 1/
5962-9688901Q9X	6Y440	MT4C1004JD22ADC3-6
5962-9688902Q9X	6Y440	MT4C1004JD22ADC3-7

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
6Y440	Micron Technology, Incorporated 8000 S. Federal Way P.O. Box 6 Boise, ID 83707-0006

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.