REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Paragraph 1.3, correct DV_{CC} from 0 V dc to +5.0 V dc to 0 V dc to +6.0 V dc. Table I, IMP, correct the limits of 55.5 and 53 dBc from maximum to minimum. Update drawing boilerplate.	02-12-18	Raymond Monnin

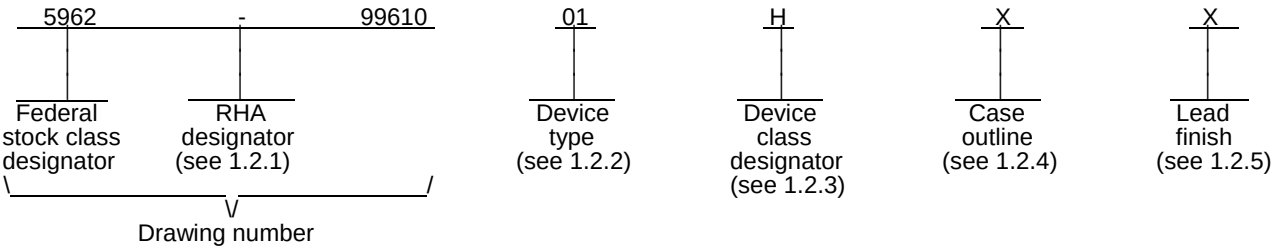
REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			A	A	A	A	A	A	A	A	A	A	A	A		
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A	PREPARED BY Gary Zahn	**DEFENSE SUPPLY CENTER COLUMBUS** **POST OFFICE BOX 3990** **COLUMBUS, OHIO 43216-5000**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Michael C. Jones	
	APPROVED BY Raymond Monnin	MICROCIRCUIT, HYBRID, DIGITAL-LINEAR, 12-BIT, DUAL CHANNEL, ANALOG TO DIGITAL CONVERTER
	DRAWING APPROVAL DATE 00-09-14	
	REVISION LEVEL A	SIZE A CAGE CODE **67268** **5962-99610** SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD10200TZ	Dual channel, 12-bit, 105 MSPS, MCM, analog to digital converter
02	AD10200BZ	Dual channel, 12-bit, 105 MSPS, MCM, analog to digital converter

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

Device class	Device performance documentation
K	Highest reliability class available. This level is intended for use in space applications.
H	Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required.
G	Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C, and D).
E	Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance.
D	Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	68	Leaded ceramic chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Analog positive supply voltage (AV_{CC})	0 V dc to +6.0 V dc
Digital positive supply voltage (DV_{CC})	0 V dc to +6.0 V dc
Analog input voltage	-0.5 V to AV_{CC} +0.5 V
Digital input voltage	-0.5 V to DV_{CC} +0.5 V
Digital output current	20 mA
Power dissipation (P_D)	2.2 W
Thermal resistance junction-to-case (θ_{JC})	2.22°C/W
Thermal resistance junction-to-ambient (θ_{JA})	24.3°C/W
Junction temperature (T_J)	+175°C
Storage temperature	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Analog positive supply voltage (AV_{CC})	+4.75 V dc to +5.25 V dc
Digital positive supply voltage (DV_{CC})	+3.14 V dc to +3.47 V dc
Case operating temperature range (T_C):	
Device type 01	-55°C to +125°C
Device type 02	-40°C to +85°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Furthermore, the manufacturer may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Output coding. The output coding shall be as specified on figure 3.

3.2.4 Timing diagram. The timing diagram shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output offset	OUT_{OFFSET}		1,2,3	01,02	-12	+12	LSB
Gain error 2/	AV_{ERROR}		1,2,3	01,02	-9	+9	%FS
Reference output voltage	V_{REF}		1,2,3	01,02	2.4	2.6	V
Analog positive supply current 3/	IA_{CC}		1,2,3	01,02		410	mA
Digital positive supply current 3/	ID_{CC}		1,2,3	01,02		40	mA
Power dissipation 4/	P_D		1,2,3	01,02		2.2	W
Digital output, logic "1" 5/ voltage	V_{OH}		1,2,3	01,02	+3.1		V
Digital output, logic "0" 5/ voltage	V_{OL}		1,2,3	01,02		0.2	V
Input voltage standing wave ratio (VSWR) 6/ 7/	VSWR		4,5,6	01,02		1.25:1	ratio
Analog input bandwidth high 6/	AINBWH		4,5,6	01,02	200		MHz
Analog input bandwidth low 6/	AINBWL		4,5,6	01,02	1		MHz
Maximum conversion rate	CNV_{MAX}		4,5,6	01,02	105		MSPS
Minimum conversion rate 6/	CNV_{MIN}		4,5,6	01,02		10	MSPS
Duty cycle 6/	DC		4,5,6	01,02	45	55	%

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Signal to noise ratio (without harmonics) 8/	SNR	f_{IN} = 41 MHz	4	01,02	64		dBFS
			5,6		62		
		f_{IN} = 71 MHz	4		62.5		
			5,6		61.5		
		f_{IN} = 121 MHz	4,5,6		61		
Signal to noise ratio (with harmonics) 9/	SINAD	f_{IN} = 41 MHz	4	01,02	63		dBFS
			5,6		60.5		
		f_{IN} = 71 MHz	4		61		
			5,6		57		
		f_{IN} = 121 MHz	4		56		
			5,6		53		
Spurious free dynamic range 10/	SFDR	f_{IN} = 41 MHz	4	01,02	73		dBFS
			5,6		67.5		
		f_{IN} = 71 MHz	4		67		
			5,6		60		
		f_{IN} = 121 MHz	4		61		
			5,6		55		
Two tone intermodulation distortion 11/	IMD	$f1_{IN}$ = 121 MHz, $f2_{IN}$ = 122 MHz	4	01,02	55.5		dBc
			5,6		53		
Power supply rejection ratio 3/ 6/	PSRR	+4.75 V $\leq AV_{CC} \leq$ +5.25 V	7,8	01,02		±5	mV/V
Differential nonlinearity 6/	DNL		7,8	01,02	-0.99	+0.99	LSB
Integral nonlinearity 6/	INL		7,8	01,02	-3	+3	LSB

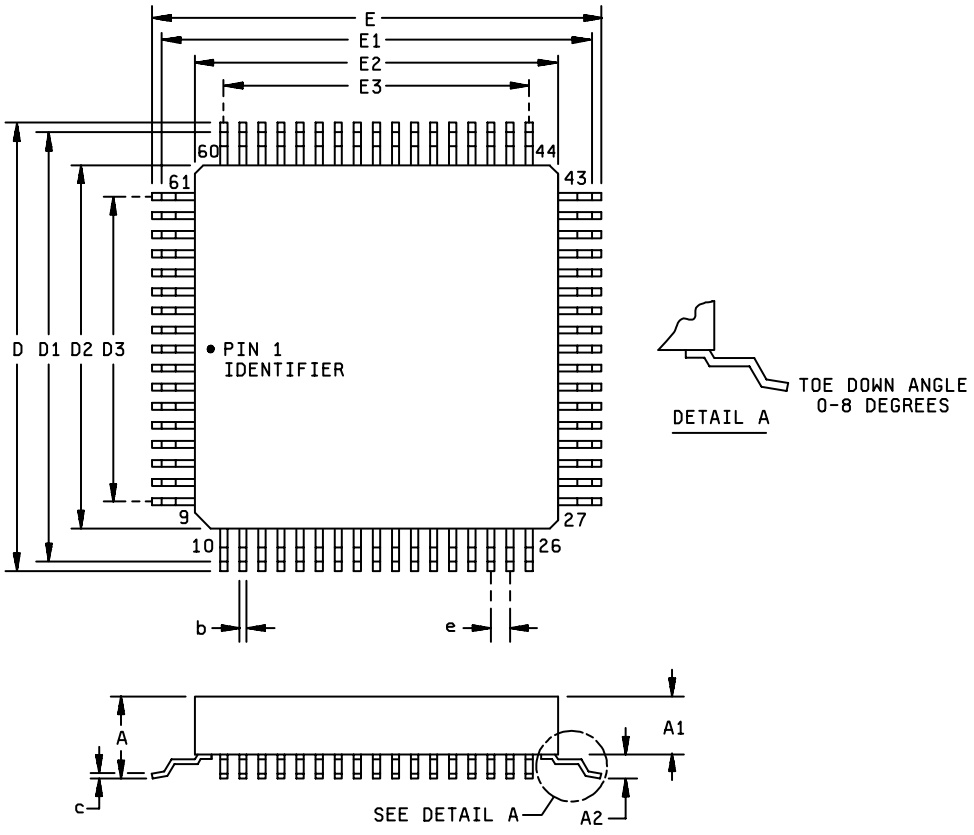
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Encode input common mode 6/	ENINCM		7,8	01,02	1.2	2.0	V
Encode input resistance, single-ended 6/	ENRIN		7,8	01,02	3	8	kΩ
Channel to channel isolation 6/ 12/	ISO		7,8	01,02	80		dB
Digital input, logic "1" voltage 3/ 6/	V_{IH}		9,10,11	01,02	2.0		V
Digital input, logic "0" voltage 3/ 6/	V_{IL}		9,10,11	01,02		0.8	V
Differential input (Encode, $\overline{\text{Encode}}$) 6/	DIFFIN		9,10,11	01,02	0.4	+5.0	V
Output valid time 5/ 6/ 13/	t_V		9,10,11	01,02	3.0		ns
Output propagation delay 5/ 6/ 14/	t_{PD}		9,10,11	01,02	4.5	8.0	ns

1/ Unless otherwise specified, AV_{CC} = +5.0 V dc and DV_{CC} = +3.3 V dc and ENCODE = 105 MSPS. Device type 01 test temperature is -55°C ≤ T_C ≤ +125°C. Device type 02 test temperature is -40°C ≤ T_C ≤ +85°C.
2/ Gain error measured at 2.5 MHz.
3/ Supply voltages should remain stable to within ±5 % for normal operation.
4/ Power dissipation is measured with encode at rated speed and 0 dBm analog input.
5/ The digital output load during test is not to exceed an ac load of 10 pF or a dc current of ±40 μA.
6/ Parameter shall be tested as part of device initial characterization and after design and process changes. Parameter shall be guaranteed to the limits specified in table I for all lots not specifically tested.
7/ Input voltage standing wave ratio is guaranteed from 10 MHz to 200 MHz for Z_O = 50 ohms.
8/ SNR is the total noise (first 5 harmonics removed) with analog input signal level at -1 dBFS. ENCODE = 105 MSPS. SNR is reported in dBFS, related back to converter full scale.
9/ SINAD is the total noise plus harmonics with analog input signal level at -1 dBFS. ENCODE = 105 MSPS. SINAD is reported in dBFS, related back to converter full scale.
10/ Analog input signal equals -1 dBFS; SFDR is the ratio of converter full scale to worst spur.
11/ Both input tones at -7 dBFS; two tone intermodulation distortion (IMD) rejection is the ratio of either tone to the worst third order intermod product. $f1_{IN}$ = X MHz ±100kHz, $f2_{IN}$ = X MHz ±100 kHz.
12/ Channel to channel isolation tested with A channel / 50 ohm terminated (Analog input A2, pin 7) grounded and a full scale signal applied to B channel (Analog input B2, pin 63).
13/ Output valid time (t_V) is defined as the time the outputs are above V_{OH} or below V_{OL}.
14/ t_{PD} is measured from the transition points of the Encode input to the 50%/50% levels of the digital outputs swing. The device has a pipeline delay of 10 clock cycles.

Case outline X.



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		7.87		0.310
A1		6.35		0.250
A2	0.18	1.02	0.040	0.060
b	0.36	0.51	0.014	0.020
c	0.18	0.25	0.007	0.010
e	1.14	1.40	0.045	0.055
D/E	29.72	30.23	1.170	1.190
D1/E1	27.18		1.070	
D2/E2	23.88	24.38	0.940	0.960
D3/E3	20.32 BSC		0.800 BSC	

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 dot and pin numbers are for reference only.

FIGURE 1. Case outline(s).

Device types	01 and 02	Device types	01 and 02	Device types	01 and 02
Case outline	X	Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	Shield	24	D8A	47	D3B
2	Channel A analog ground	25	D7A	48	D2B
3	VREF_A_OUT	26	Channel A digital ground	49	D1B
4	Do not connect	27	Channel A digital ground	50	D0B (LSB)
5	Channel A analog ground	28	D6A	51	DV_{CC}
6	No connection	29	D5A	52	Channel B analog ground
7	Analog input A2	30	D4A	53	Encode B
8	Do not connect	31	D3A	54	$\overline{\text{Encode B}}$
9	Channel A analog ground	32	D2A	55	Channel B analog ground
10	Channel A analog ground	33	D1A	56	VREF_B_OUT
11	Channel A analog ground	34	D0A (LSB)	57	Do not connect
12	Do not connect	35	Channel A analog ground	58	Do not connect
13	Channel A analog ground	36	Channel B analog ground	59	Channel B analog ground
14	AV_{CC}	37	D11B (MSB)	60	Channel B analog ground
15	Do not connect	38	D10B	61	Channel B analog ground
16	Channel A analog ground	39	D9B	62	No connect
17	$\overline{\text{Encode A}}$	40	D8B	63	Analog input B2
18	Encode A	41	D7B	64	Do not connect
19	Channel A analog ground	42	D6B	65	Channel B analog ground
20	DV_{CC}	43	Channel B digital ground	66	AV_{CC}
21	D11A (MSB)	44	Channel B digital ground	67	Do not connect
22	D10A	45	D5B	68	Channel B analog ground
23	D9A	46	D4B		

FIGURE 2. Terminal connections.

Code	AIN (V)	Digital Output
+2047	+1.024	0111 1111 1111
•	•	•
•	•	•
0	0	0000 0000 0000
-1	-0.00049	1111 1111 1111
•	•	•
•	•	•
-2048	-1.024	1000 0000 0000

NOTE:
1. Two's complement, V_{REF} = +2.5 V.

FIGURE 3. Output coding.

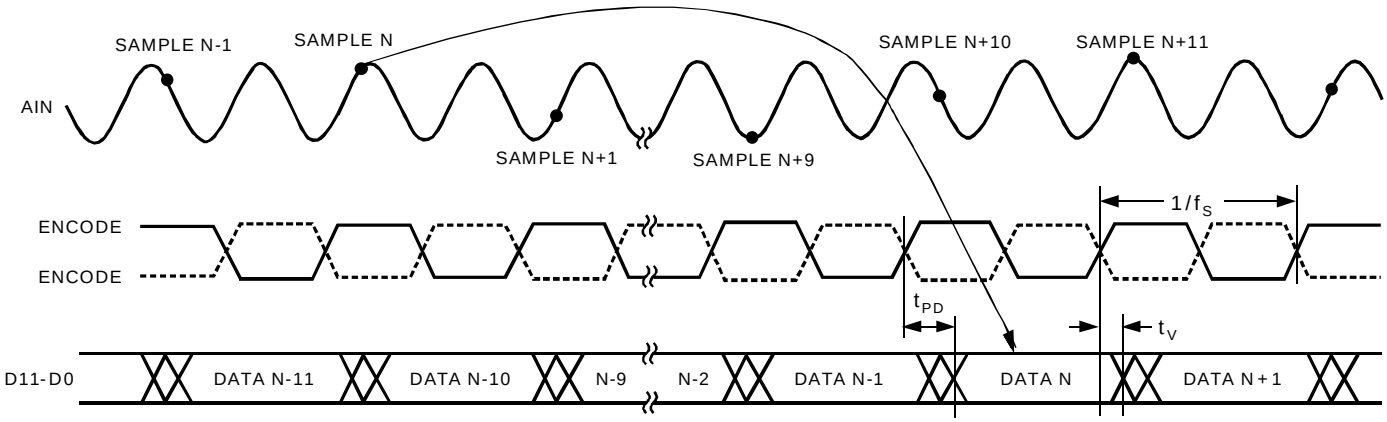


FIGURE 4. Timing diagram.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1
Final electrical parameters	1*,2,3,4,5,6,7,8,9,10,11
Group A test requirements	1,2,3,4,5,6,7,8,9,10,11
Group C end-point electrical parameters	1
End-point electrical parameters for radiation hardness assurance (RHA) devices	Not applicable

* PDA applies to subgroup 1.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and tests shall be as specified in table II herein.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-PRF-38534.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Post Office Box 3990, Columbus, Ohio 43216-5000, or telephone (614) 692-0536.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-12-18

Approved sources of supply for SMD 5962-99610 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9961001HXA	34031	AD10200TZ/QMLH
5962-9961002HXA	34031	AD10200BZ/QMLH

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34031	Analog Devices, Incorporated 7910 Triad Center Drive Greensboro, NC 27409-9605 Point of contact: Greensboro Manufacturing