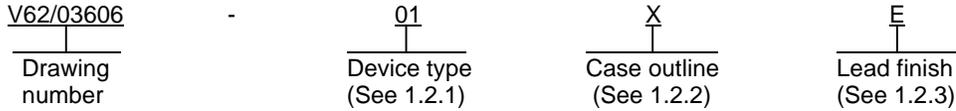


1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance analog multiplexer/demultiplexer microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	74HC4051-EP	Analog multiplexer/demultiplexer

1.2.2 Case outline(s). The case outlines shall be as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	16	MS-012	Plastic small-outline package

1.2.3 Lead finishes. The lead finishes shall be as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium

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1.3 Absolute maximum ratings. 1/

Supply voltage range ($V_{CC} - V_{EE}$).....	-0.5 V to 10.5 V 2/
Supply voltage range (V_{CC}).....	-0.5 V to 7.0 V
Supply voltage range (V_{EE}).....	+0.5 V to -7.0 V
Input clamp current (I_{IK}) ($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V).....	± 20 mA
Output clamp current (I_{OK}) ($V_O < V_{EE} - 0.5$ V or $V_O > V_{CC} + 0.5$ V).....	± 20 mA
Switch current ($V_I > V_{EE} - 0.5$ V or $V_I < V_{CC} + 0.5$ V).....	± 25 mA
Continuous current through V_{CC} or GND.....	± 50 mA
V_{EE} current (I_{EE}).....	-20 mA
Storage temperature range (T_{STG}).....	-65°C to 150°C
Maximum junction temperature (T_J).....	150°C
Lead temperature (during soldering):	
At distance $1/16 \pm 1/32$ inch (1.59 \pm 0.79 mm) from case for 10 s max.....	300°C
Package thermal impedance (θ_{JA}): 3/	
X package.....	73°C/W

1.4 Recommended operating conditions. 4/ 5/

Supply voltage range (V_{CC}).....	2.0 V to 6.0 V 6/
Supply voltage range ($V_{CC} - V_{EE}$) (See figure 1).....	2.0 V to 10.0 V
Supply voltage range (V_{EE}) (See figure 1).....	0.0 V to -6.0 V 6/
Input control voltage range (V_I).....	0.0 V to V_{CC}
Analog switch I/O voltage range (V_{IS}).....	V_{EE} to V_{CC}
Minimum high level input voltage (V_{IH}):	
$V_{CC} = 2.0$ V.....	1.5 V
$V_{CC} = 4.5$ V.....	3.15 V
$V_{CC} = 6.0$ V.....	4.20 V
Maximum low level input voltage (V_{IL}):	
$V_{CC} = 2.0$ V.....	0.5 V
$V_{CC} = 4.5$ V.....	1.35 V
$V_{CC} = 6.0$ V.....	1.80 V
Minimum input transition rise or fall time (t_i):	
$V_{CC} = 2.0$ V, 4.5 V, and 6.0 V.....	0.0 ns
Maximum input transition rise or fall time (t_f):	
$V_{CC} = 2.0$ V.....	1000 ns
$V_{CC} = 4.5$ V.....	500 ns
$V_{CC} = 6.0$ V.....	400 ns
Operating free-air temperature range (T_A).....	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltage referenced to GND unless otherwise specified.

3/ The package thermal impedance is calculated in accordance with JESD 51-7.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

6/ In certain applications, the external load resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6 V (calculated from r_{ON} values shown in table I, herein). No V_{CC} current flows through R_L if the switch current flows into the COM OUT/IN A terminal.

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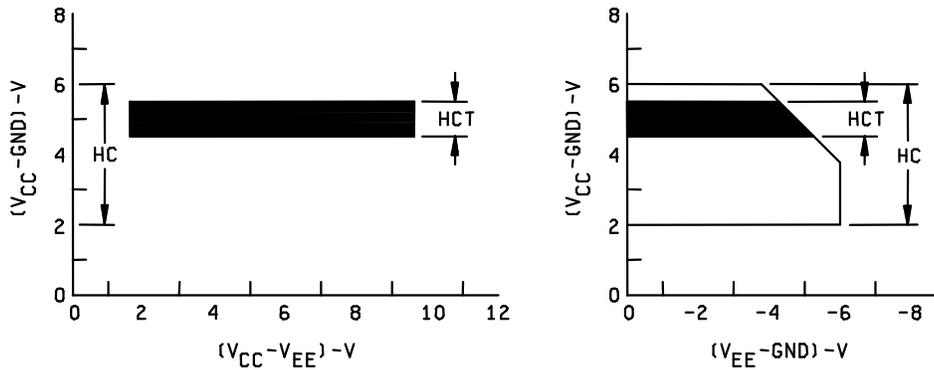


FIGURE 1. Recommended operating area as a function of supply voltages.

2. APPLICABLE DOCUMENTS

- JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices
- JEDEC STD 51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Applications for copies should be addressed to the Electronic Industry Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or at <http://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 2.

3.5.2 Truth table. The truth table shall be as shown in figure 3.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 5.

3.5.5 Test circuits and timing waveforms. The tests circuits and timing waveforms shall be as shown in figure 6.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions	V _{EE}	V _{CC}	Temperature, T _A	Device type	Limits		Unit
							Min	Max	
ON resistance	r _{ON}	V _{IS} = V _{CC} or V _{EE} I _O = 1 mA V _I = V _{IH} or V _{IL} 1/ See figure 7	0.0 V	4.5 V	25°C	All		160	Ω
					-55°C to 125°C			240	
			0.0 V	6.0 V	25°C		140		
					-55°C to 125°C		210		
			-4.5 V	4.5 V	25°C		120		
					-55°C to 125°C		180		
		V _{IS} = V _{CC} to V _{EE} I _O = 1 mA V _I = V _{IH} or V _{IL} 1/ See figure 7	0.0 V	4.5 V	25°C		180		
					-55°C to 125°C		270		
			0.0 V	6.0 V	25°C		160		
					-55°C to 125°C		240		
			-4.5 V	4.5 V	25°C		130		
					-55°C to 125°C		195		
Maximum ON resistance	Δr _{ON}	Between any two channels	0.0 V	4.5 V	25°C	All	10 typical		Ω
			0.0 V	6.0 V			8.5 typical		
			-4.5 V	4.5 V			5 typical		
Switch ON/OFF leakage current	I _{IZ}	For switch OFF: When V _{IS} = V _{CC} , V _{OS} = V _{EE} ; When V _{IS} = V _{EE} , V _{OS} = V _{CC} For switch ON: All applicable combinations of V _{IS} and V _{OS} voltage levels V _I = V _{IH} or V _{IL} 1/	0.0 V	6.0 V	25°C	All		±0.2	μA
					-55°C to 125°C			±2.0	
			-5.0 V	5.0 V	25°C		±0.4		
					-55°C to 125°C		±4.0		
Control input leakage current	I _{IL}	V _I = V _{CC} or GND	0.0 V	6.0 V	25°C	All		±0.1	μA
					-55°C to 125°C			±1.0	

See footnotes ant end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	V _{EE}	V _{CC}	Temperature, T _A	Device type	Limits		Unit
							Min	Max	
Quiescent supply current	I _{CC}	V _I = V _{CC} or GND I _O = 0 A When V _{IS} = V _{EE} , V _{OS} = V _{CC}	0.0 V	6.0 V	25°C	All		8	μA
					-55°C to 125°C			160	
		V _I = V _{CC} or GND I _O = 0 A When V _{IS} = V _{CC} , V _{OS} = V _{EE}	-5.0 V	5.0 V	25°C		16		
					-55°C to 125°C		320		
Input control capacitance	C _I	C _L = 50 pF			25°C, -55°C to 125°C	All		10	pF
Power dissipation capacitance	C _{PD} <u>2/</u>	t _r = t _f = 6 ns		5.0 V	25°C	All	50 typical		pF
Propagation delay time, switch IN to OUT	t _{pd}	C _L = 15 pF See figure 6		5.0 V	25°C	All		4	ns
					-55°C to 125°C			60	
		C _L = 50 pF See figure 6	0.0 V	2.0 V	25°C		90		
					-55°C to 125°C		12		
		0.0 V	4.5 V	25°C	18				
				-55°C to 125°C	10				
		0.0 V	6.0 V	25°C	15				
				-55°C to 125°C	8				
-4.5 V	4.5 V	25°C	12						
		-55°C to 125°C							
Propagation delay time, switch turn "ON" delay from S or \bar{E} to switch output	t _{en}	C _L = 15 pF See figure 6		5.0 V	25°C	All		19	ns
					-55°C to 125°C			225	
		C _L = 50 pF See figure 6	0.0 V	2.0 V	25°C		340		
					-55°C to 125°C		45		
		0.0 V	4.5 V	25°C	68				
				-55°C to 125°C	38				
		0.0 V	6.0 V	25°C	57				
				-55°C to 125°C	32				
-4.5 V	4.5 V	25°C	48						
		-55°C to 125°C							

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	V _{EE}	V _{CC}	Temperature, T _A	Device type	Limits		Unit
							Min	Max	
Propagation delay time, switch turn "OFF" delay from S or \bar{E} to switch output	t _{dis}	C _L = 15 pF See figure 6		5.0 V	25°C	All		19	ns
					-55°C to 125°C			225	
		C _L = 50 pF See figure 6	0.0 V	2.0 V		25°C	All		340
					-55°C to 125°C	45			
		0.0 V	4.5 V	25°C	All		68		
				-55°C to 125°C			38		
		0.0 V	6.0 V	25°C	All		57		
				-55°C to 125°C			32		
-4.5 V	4.5 V	25°C	All		48				
		-55°C to 125°C							

Analog channel characteristics

Switch input capacitance	C _{IN}				25°C	All	5 typical	pF
Common output capacitance	C _{COM}				25°C	All	25 typical	pF
Minimum switch frequency response at -3 dB	f _{MAX} <u>3/</u> <u>4/</u>	See figures 6 and 7	-2.25 V	2.25 V	25°C	All	145 typical	MHz
			-4.5 V	4.5 V			180 typical	
Sine-wave distortion		See figure 6	-2.25 V	2.25 V	25°C	All	0.035 typical	%
			-4.5 V	4.5 V			0.018 typical	
S or \bar{E} to switch feed-through noise	<u>4/</u> <u>5/</u>	See figure 6	-2.25 V	2.25 V	25°C	All	TBD	mV
			-4.5 V	4.5 V			TBD	
Switch "OFF" signal feed-through	<u>4/</u> <u>5/</u>	See figures 6 and 7	-2.25 V	2.25 V	25°C	All	-73 typical	dB
			-4.5 V	4.5 V			-75 typical	

1/ The values to be used for V_{IH} and V_{IL} shall be the V_{IH} minimum and V_{IL} maximum values listed in section 1.4 herein.

2/ C_{PD} is used to determine the dynamic power consumption, per package.

$$P_D = C_{PD} V_{CC}^2 f_I + \sum (C_L + C_S) V_{CC}^2 f_O$$

Where f_O is output frequency; f_I is input frequency; C_L is output load capacitance; C_S is switch capacitance; and V_{CC} is supply voltage.

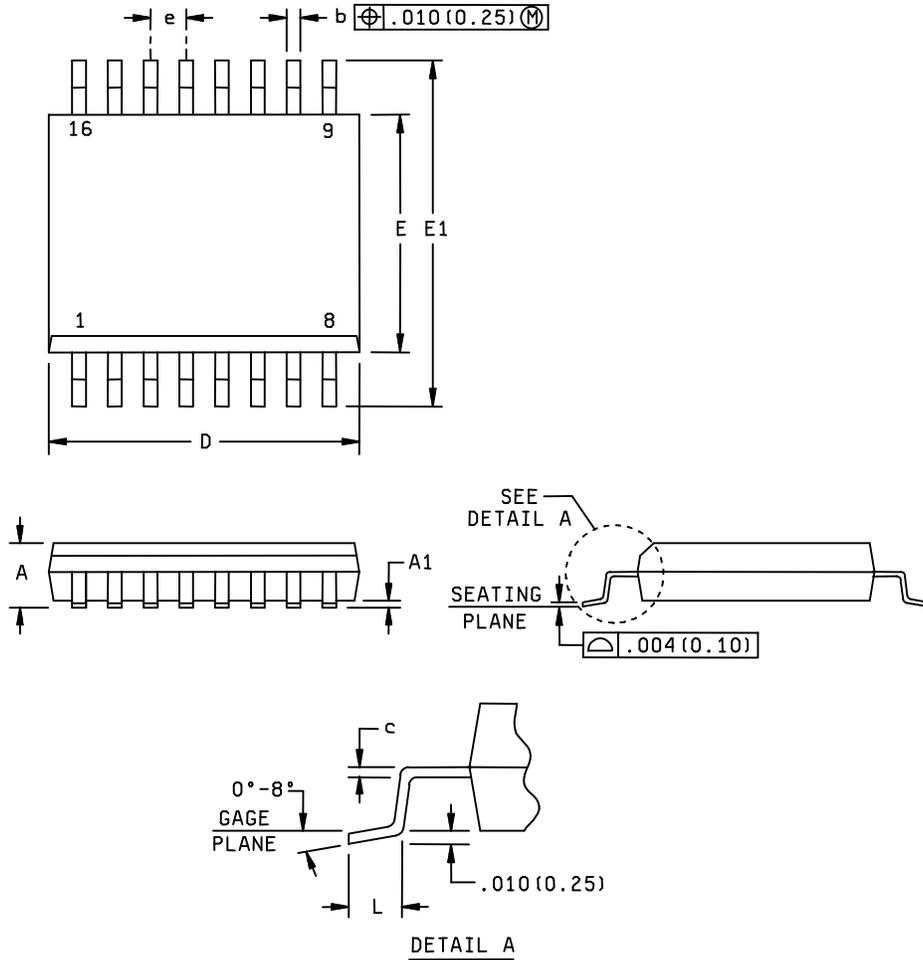
3/ Adjust input voltage to obtain 0 dBm at V_{OS} for f_{IN} = 1 MHz.

4/ V_{IS} is centered at (V_{CC} - V_{EE})/2.

5/ Adjust input for 0 dBm.

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Case X



NOTES:

1. All linear dimensions are in inches (millimeters).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed .006 inches.
4. Fall within JEDEC MS-012.

FIGURE 2. Case outline.

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Case X - Continued

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		.069		1.75
A1	.004	.010	0.10	0.25
b	.014	.020	0.35	0.51
c	.008 NOM		0.20 NOM	
D	.386	.394	9.80	10.00
E	.150	.157	3.81	4.00
E1	.228	.244	5.80	6.20
e	.050 BSC		1.27 BSC	
L	.016	.044	0.40	1.12

FIGURE 2. Case outline - Continued.

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Inputs				ON channel(s)
\bar{E}	S ₂	S ₁	S ₀	
L	L	L	L	A ₀
L	L	L	H	A ₁
L	L	H	L	A ₂
L	L	H	H	A ₃
L	H	L	L	A ₄
L	H	L	H	A ₅
L	H	H	L	A ₆
L	H	H	H	A ₇
H	X	X	X	None

H = High voltage level
L = Low voltage level
X = Don't care

FIGURE 3. Truth table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03606
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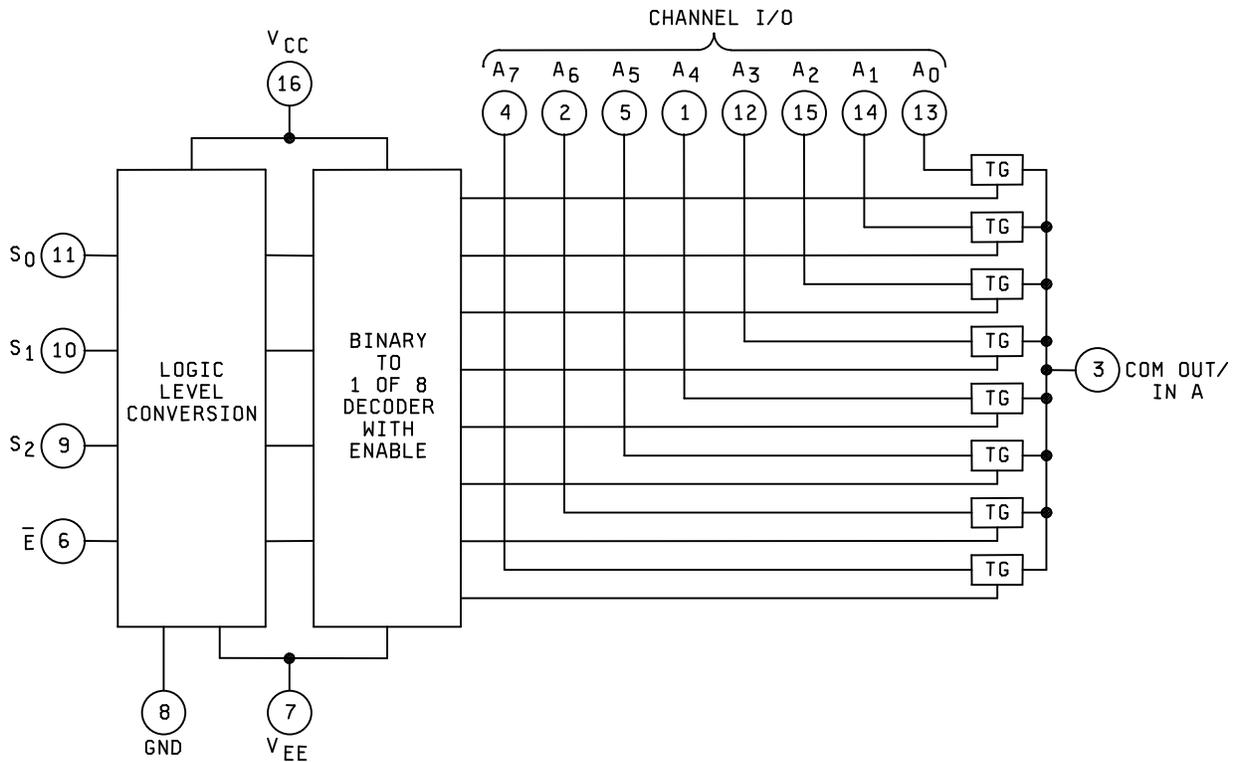


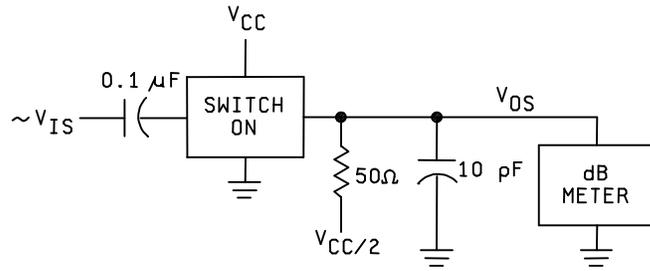
FIGURE 4. Logic diagram.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/03606</p>
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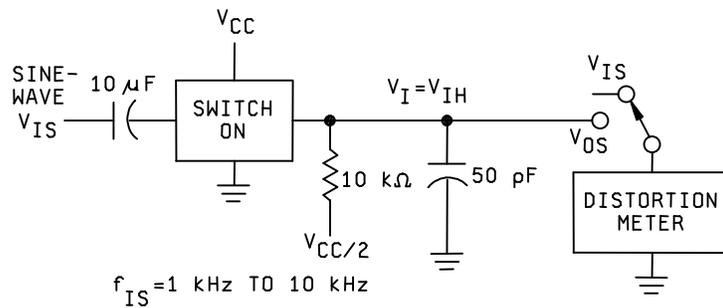
Device type 01	
Case outline	X
Terminal number	Terminal symbol
1	CHANNEL I/O A ₄
2	CHANNEL I/O A ₆
3	COM OUT/IN A
4	CHANNEL I/O A ₇
5	CHANNEL I/O A ₅
6	\bar{E}
7	V _{EE}
8	GND
9	ADDRESS SEL S ₂
10	ADDRESS SEL S ₁
11	ADDRESS SEL S ₀
12	CHANNEL I/O A ₃
13	CHANNEL I/O A ₀
14	CHANNEL I/O A ₁
15	CHANNEL I/O A ₂
16	V _{CC}

FIGURE 5. Terminal connections.

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FREQUENCY-RESPONSE TEST CIRCUIT



SINE-WAVE DISTORTION TEST CIRCUIT

FIGURE 6. Test circuits and timing waveforms.

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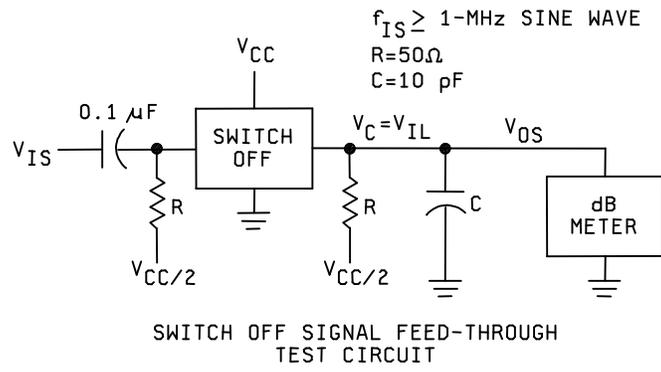
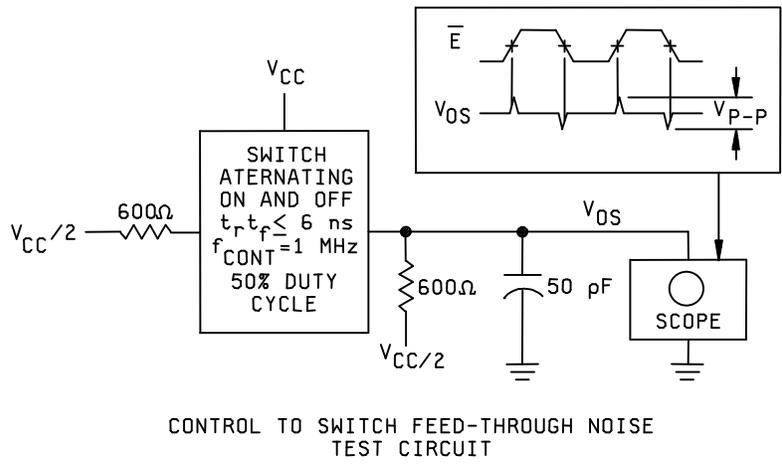
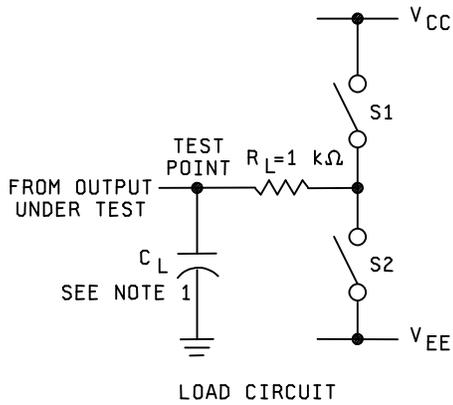
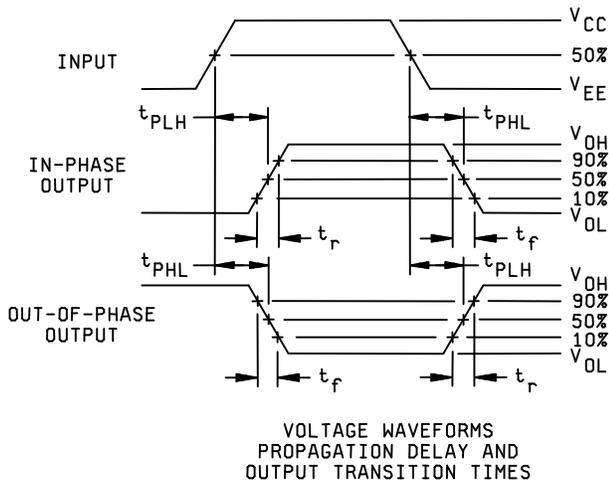


FIGURE 6. Test circuits and timing waveforms - Continued.

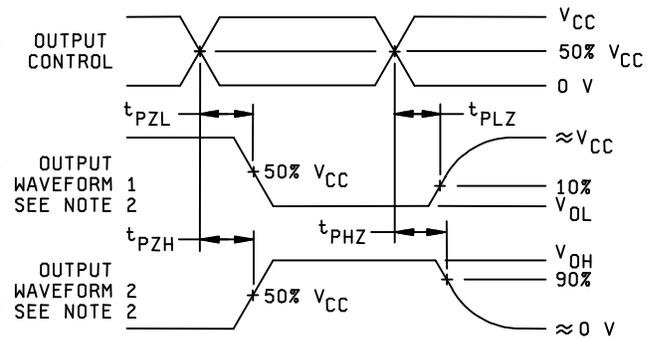
DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03606
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PARAMETER		S1	S2
t_{en}	t_{PZH}	OPEN	CLOSED
	t_{PZL}	CLOSED	OPEN
t_{dis}	t_{PHZ}	OPEN	CLOSED
	t_{PLZ}	CLOSED	OPEN
t_{pd}		OPEN	OPEN



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND
OUTPUT TRANSITION TIMES



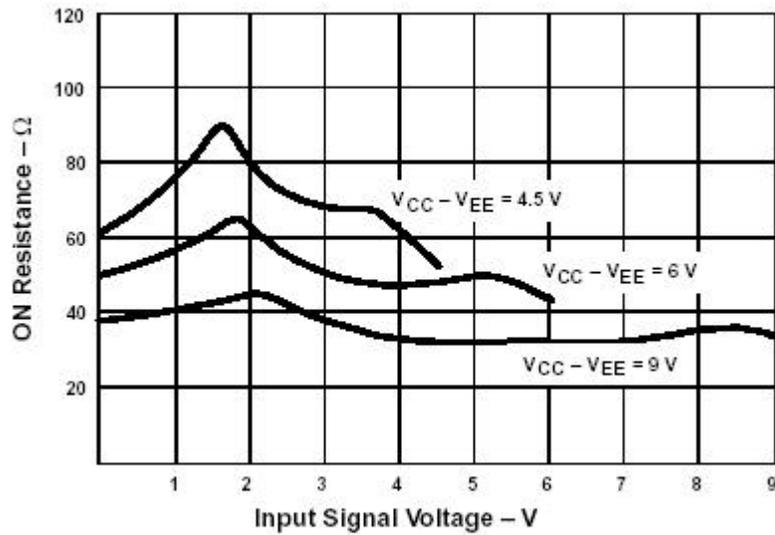
VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES:

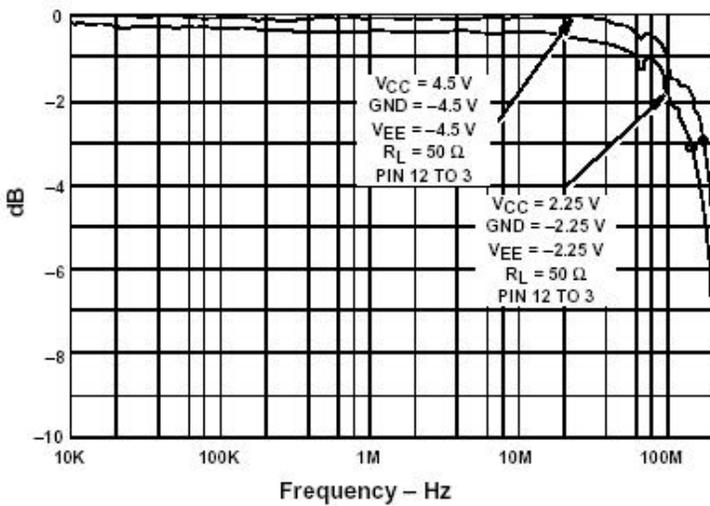
1. C_L includes probe and test-fixture capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
4. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
5. The outputs are measured one at a time with one input transition per measurement.
6. t_{PLZ} and t_{PHZ} are the same as t_{dis} ; t_{PZL} and t_{PZH} are the same as t_{en} ; t_{PLH} and t_{PHL} are the same as t_{pd} .

FIGURE 6. Test circuits and timing waveforms - Continued.

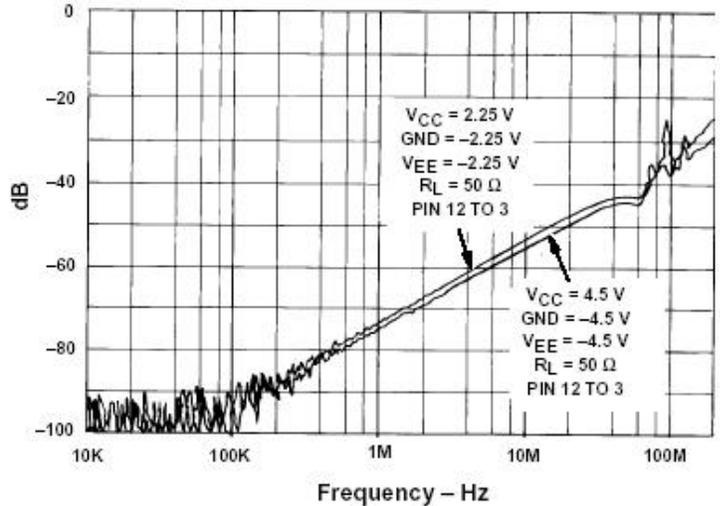
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TYPICAL ON RESISTANCE VS INPUT SIGNAL VOLTAGE



CHANNEL ON BANDWIDTH



CHANNEL OFF FEED THROUGH

FIGURE 7. Typical characteristics.

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4.0 QUALITY ASSURANCE PROVISIONS

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5.0 PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6.0 NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/03606-01XE	01295	CD74HC4051MM96EP	HC4051DEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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