

USING DIE from an EXTERNAL SOURCE

1. INTRODUCTION

Some part manufacturers would like to supply products that comply with MIL-PRF-38535, or with MIL-STD-883 / paragraph 1.2.1, but want to purchase the die from external sources. The part manufacturer may have no control of the die. or may control certain aspects, e.g., die design.

To assist a part manufacturer in meeting the requirements for obtaining die from external sources, the Defense Supply Center Columbus (DSCC-VQC, Custom Devices office) has developed the attached checklists.

Self-Audit Requirements, paragraph A.4.9. of MIL-PRF-38535, requires a part manufacturer to conduct a site audit of a subcontractor. See the attached checklist, item #4, "Site Audit of External Wafer Fab".

Design and Construction, paragraph A.3.5. of MIL-PRF-38535, require a part manufacturer to document the identity of the die, and the circuit design, and wafer process, used for the die. See the attached checklist #5, "Die Evaluation".

The Site Audit of External Wafer Fab, and Die Evaluation, as applicable, are to be conducted by the DSCC-certified part manufacturer (MIL-PRF-38535), or the "self-certified" manufacturer (MIL-STD-883, paragraph 1.2.1).

2. DEFINITIONS

- DSCC-VQC (Custom Devices office) is Michael Adams.
- A part manufacturer sells packaged die on the open market. Subcontractors may be used for some operations.
- A part specification is the standardized document controlled by DSCC that defines the requirements for an integrated circuit (i.e., 38510 detail spec or Standard Microcircuit Drawing, SMD).
- Certified manufacturing operations are those that have undergone a site audit and have been certified by DSCC, or a TRB, for having demonstrated compliance with MIL-PRF-38535 and applicable appendices, including applicable paragraphs of Appendix A.
- A wafer fab line is a set of equipment used to process wafers, e.g., Fab A, Fab 3
 - A wafer fab flow is a sequence of operations using a wafer fab line to fabricate various die families.
 - A part number traveler uses the sequence of a wafer flow and the process specifications for the grade, electrical parameters, etc., of a particular die, e.g., the die process for QML grade, 1.5 A, 5 volt, voltage regulator
- A die re-seller, die dealer, etc., purchases a die for the purpose of re-selling it in die form.
- A certificate of conformance (C of C) to MIL-PRF-38535 signifies that
 1. All requirements of that specification are complied with, including the die design (e.g., metallization current density, etc.) and wafer processing (e.g., wafer re-work restrictions, etc.) requirements of Appendix A.
OR
 2. All reductions of the requirements of that specification, including the die design (e.g., metallization current density, etc.) and wafer processing (e.g., wafer re-work restrictions, etc.) requirements of Appendix A, have been approved by the TRB.

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3. EXTERNAL SOURCES

Possible external sources of die are discussed below. If the external source being considered by a part manufacturer is not included below, call DSCC-VQC to discuss the requirements.

1. Die listed on QML38535, Section I, Table V (i.e., SMD contains requirements for selling die)
Part manufacturer is:
 - Required to conduct qualification testing for the die / package combination to be made.
2. Die Processed to a Certified Wafer Flow
 - A. Contact DSCC-VQC (Custom Devices office) to determine status of wafer flow
 - B. Each shipment is accompanied by a certificate of conformance to MIL-PRF-38535 and signed by the QML program manager (or the QML program manager's designee).
Part manufacturer is required to:
 - Conduct qualification testing for the die / package combination to be made
 - C. Each shipment is not accompanied by a certificate of conformance to MIL-PRF-38535 and signed by the QML program manager (or the QML program manager's designee).
Part manufacturer is required to:
 - Perform Die Evaluation
 - Conduct qualification testing for the die / package combination to be made
3. Die Processed to an Uncertified Wafer Flow
 - A. Contact DSCC-VQC (Custom Devices office) to determine status of wafer flow
 - B. Wafer flow audited by DSCC
Part manufacturer is required to:
 - Perform Die Evaluation
 - Conduct qualification testing for the die / package combination to be made
 - C. Wafer flow not audited by DSCC
Part manufacturer is required to:
 - Conduct Site Audit of external wafer fab
 - Perform Die Evaluation
 - Conduct qualification testing for the die / package combination to be made
4. Die Obtained from a Re-Seller
 - A. Contact DSCC-VQC (Custom Devices office) to determine status of die manufacturer.
 - B. Each shipment is accompanied by a certificate of conformance to MIL-PRF-38535, and signed by the QML program manager (or the QML program manager's designee) of the die manufacturer.
Part manufacturer is required to:
 - Conduct qualification testing for the die / package combination to be made
 - C. Each shipment is not accompanied by a certificate of conformance to MIL-PRF-38535.
Part manufacturer is required to:
 - Conduct Site Audit of external wafer fab
 - Perform Die Evaluation
 - Conduct qualification testing for the die / package combination to be made

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4. SITE AUDIT of EXTERNAL WAFER FAB

The part manufacturer is to complete following checklist for the die to be purchased by conducting a site audit of the external wafer fab. The completed checklist, and summary of the audit, is to be submitted to DSCC-VQC. Paragraph 3.1, MIL-PRF-38535, may used to respond to the checklist items, as appropriate.

NOTE: THE PART MANUFACTURER IS TO CONTACT DSCC-VQC IF A SITE AUDIT CANNOT BE ARRANGED.

Wafer Fab Plant

- Name of company, and name of owner (if other than name of company)
- Address of plant (physical location)
- Point of contact
 - Name
 - Job title
 - Phone number
 - Email

Process Used to Make Die

- Name, number, etc., of the fab line
- Name, number, revision, etc., of wafer flow
- Name, number, revision, etc., of part number traveler
- Technology (bipolar, CMOS, etc.)
- Method used by external wafer fab to ensure using part number traveler assigned to part manufacturer

Site Verification Audit of Wafer Fab Flow

- Verify control of process steps used to make die to be purchased
 - Enter rooms used for wafer fab
 - Use controlled audit checklist to conduct audit
- Control of each process step
 - Documented procedures
 - Used by operators
 - All wafers in a fab lot are processed to ensure the homogeneity of the wafers
 - Check the accuracy of information entered on fab lot traveler
- Equipment calibration
 - Calibrated as appropriate
 - Labels used
 - Records are maintained
- Training
 - Documented procedures
 - Records maintained
- SPC
 - Documented procedures
 - Critical nodes identified and monitored
 - Out-of-control rules are defined
 - Corrective actions taken are recorded
- Self-audit
 - Documented procedures
 - Records are maintained
- Re-do (re-work, repair, re-process, additional processing, continuation of processing, etc.)
 - Allowances, and restrictions, documented
 - Recorded on fab lot traveler when performed

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4. SITE AUDIT of EXTERNAL WAFER FAB

Metal Deposition Monitor

- Documented procedure
- Monitor each system or provide correlation data
- Specified thickness for each metal level
- Specified thickness for each metal layer
- Name of method used to measure thickness
- Each metal level monitored
- Required for Appendix A, MIL-PRF-38535
 - SEM is used for inspection
 - Frequency of sample (no longer than one month)
 - Monitor process family or product
 - Sample size and accept number
 - Monitor is failed
 - Recover all products at risk since last monitor acceptance
 - Disposition of products at risk
- Sampling
 - Wafer location in chamber
 - Die location on wafer
- Acceptance criteria
 - General metal criteria
 - Metal over passivation steps
 - Metal over contacts
- Records
 - Photos are used
 - Other

Glassivation Monitor (passivation applied after metal)

- Monitor each chamber
- Composition of each layer (if "multi-layer" used)
- Specified thickness of each layer

Final Die Thickness Monitor

- Specified thickness
- Monitored

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4. SITE AUDIT of EXTERNAL WAFER FAB

Parametric Monitors (PM)

THESE MONITORS ARE CONTAINED IN APPENDIX H. THEY ARE INCLUDED TO ASSIST THE PART MANUFACTURER CONDUCT ITS EVALUATION OF THE EXTERNAL WAFER FAB.

These monitors are electrical measurements obtained from a set of test structures after the completion of wafer fab. The measurements are used to monitor wafer fab process steps, and to provide data for the circuit simulation program, design rules, and wafer fab process rules. Alternate methods, e.g., in-line monitors, are acceptable if properly documented. The following parameters are to be used as a guideline in formulating the monitors

1. General Process Parameters

Parameters

<i>Test Structure</i>	Sheet resistance (each metal level)	Junction breakdown (each diffusion)	Contact resistance (each interlevel)	Ionic contamination	Other
Design specified					
Location provides wafer uniformity info (1)					
Test procedure and pass / fail criteria					
Relation between measurement and circuit simulation					

(1) Suggested locations are one near the center and one in each quadrant, at least 2/3 of the radius from the center

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4. SITE AUDIT of EXTERNAL WAFER FAB

Parametric Monitors (cont.)

2. MOS (unipolar) Process Parameters

Minimum Transistor Set

- Large geometry transistor
- Short channel effect allowed by design rule
- Narrow width effect allowed by design rule

<i>Test Structure</i>	<i>Parameters</i>			
	Gate oxide thickness	Threshold voltage	Linear transconductance	Effective channel length
Gate oxide				
Design specified				
Location provides wafer uniformity info (1)				
Test procedure and pass / fail criteria				
Relation between measurement and circuit simulation				

(1) Suggested locations are one near the center and one in each quadrant, at least 2/3 of the radius from the center

<i>Test Structure</i>	<i>Parameters</i>			
	Ion & Ioff	Prop delay	Field leakage	Other
Design specified				
Location provides wafer uniformity info (1)				
Test procedure and pass / fail criteria				
Relation between measurement and transistor simulation value				

(1) Suggested locations are one near the center and one in each quadrant, at least 2/3 of the radius from the center

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4. SITE AUDIT of EXTERNAL WAFER FAB

Parametric Monitors (cont.)

3. Bipolar Process Parameters

Parameters

<i>Test Structure</i>	Sheet resistance (each diffusion)	Schottky diode reverse leakage	Schottky diode reverse breakdown	Schottky diode forward voltage
Design specified				
Location provides wafer uniformity info (1)				
Test procedure and pass / fail criteria				
Relation between measurement and circuit simulation				

(1) Suggested locations are one near the center and one in each quadrant, at least 2/3 of the radius from the center

Parameters

<i>Test Structure</i>	hFE (DC beta)	Leakage currents	Breakdown voltages	Forward voltages	Prop delay	Isolation leakage
Design specified						
Location provides wafer uniformity info (1)						
Test procedure and pass / fail criteria						
Relation between measurement and circuit simulation						

(1) Suggested locations are one near the center and one in each quadrant, at least 2/3 of the radius from the center

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4. SITE AUDIT of EXTERNAL WAFER FAB

Reliability

Data available from external wafer fab

- Process flow that makes die to be purchased
- Die / package material combination used
- Die to be purchased
- Package material used

THE FOLLOWING ARE CONTAINED IN APPENDIX H. THEY ARE INCLUDED TO ASSIST THE PART MANUFACTURER CONDUCT ITS EVALUATION OF THE EXTERNAL WAFER FAB.

1. Technology Characterization Vehicle (TCV) A set of test structures used to monitor the susceptibility of the die (materials, construction geometry, and physical dimensions) to failure due to wear-out mechanisms (aka intrinsic reliability). The following items are the minimum to be addressed.

Wear-out mechanisms

- Hot carrier aging
 - MOS
 - Bipolar
- Metal electromigration
- Time dependent dielectric breakdown
- Fast-test structures
- Ohmic contact degradation
- Other

For each wear-out mechanism

- Location of test structure
- Test procedure, and pass / fail criteria, are specified

2. Standard Evaluation Circuit (SEC) A single test structure used to monitor the susceptibility of the die (circuit design, circuit layout software, wafer fab flow, and wafer fab process steps) to failure due to operating-stress mechanisms interacting with a die defect (aka extrinsic reliability) The following items should be addressed.

Test structure used

- Production die
- Special die

Construction of SEC

- Complexity
 - Digital is to be one-half the number of transistors that would be used for the most complex part
 - Analog is to be a representative complexity and major circuit elements
- Functionality capable of being screened, and tested, as are production parts
- Design---a circuit design that requires the maximum capability of each design rule
- Wafer fab---same flow, and process steps, that are used for production parts
- Package---a qualified package

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4. SITE AUDIT of EXTERNAL WAFER FAB

Change Control

- Major changes are defined and documented
 - Process change
 - Product (i.e., die)
- Major changes comply with Table A-1, MIL-PRF-38535
- Major changes notice is sent to die customer

Quality Assurance

- Minimum yield gates
- Critical parametric monitors
 - Name of parameter
 - Range of acceptable value
- Part manufacturer's die purchase spec
 - Quality manager of external wafer fab received copy
 - Part manufacturer actions
 - Obtain certification of conformance to die purchase spec
 - Verify certificate of conformance to purchase order, or die purchase spec, complies with MIL-PRF-38535
- Shipping die to part manufacturer
 - Traceability for each fab lot number

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5. DIE EVALUATION

The part manufacturer is to complete following checklist for the die to be purchased. It is intended to baseline the die, and to identify the boundaries of its electrical, environmental, reliability, etc., performance. Some of the information may be available from the external wafer fab. The completed checklist, and data obtained, is to be submitted to DSCC-VQC.

The qualification of the die / package combination to be made by the part manufacturer is in addition to the die evaluation.

If any item is not used for evaluation, provide the technical reason.

Electrical Performance Characterization

Source of parts for characterization

- Manufacturer
- Distributor
- Other (specify)
- Temperature rating
- Package material
 - Plastic
 - Hermetic
 - Other (specify)

Pre-characterization testing

- None
- Tests used
 - Purpose
 - Parts used for characterization (accept or reject)

Wafer fab process stability

- Use more than one fab lot made by the external wafer fab
- Performance margin. This is the ability of die to meet the part spec when operated slightly outside of recommended operating conditions (ROC) of the military part spec. Use of Tcase = 10C outside of the ROC, and Vcc = + / - 15% beyond the nominal Vcc
 - Determine if Tjunction (actual) will exceed Tjunction (absolute max)
 - Determine DC input conditions required to operate die
 - Determine change in DC output signals of die
 - Determine AC input conditions required to operate die
 - Determine change in AC output signals of die

Performance de-rating

- Changes to part spec by part manufacturer because the range of part spec ROC is wider than range of purchased die ROC
- Reduce one, or more, parameters, e.g., power, speed, etc., to ensure Tj (actual) does not exceed Tj (absolute max)

Performance assurance

- Additions to part spec by part manufacturer because range of part spec ROC is wider than range of purchased die ROC
- Add one, or more, parameters, e.g., gate current, substrate current, trigger current for latch-up, etc., to ensure performance throughout ROC

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5. DIE EVALUATION

Product Baseline

Procurement documents used by part manufacturer contain sufficient information

Absolute maximum ratings for electrical and temperature

Recommended operating conditions (ROC) for electrical and temperature

Die part number and mask set revision (assigned by die manufacturer) that is purchased by part manufacturer

Die part number (assigned by part manufacturer) that is used on purchase order

Marking on die (visible by using magnification)

Process used to make the die (this is also on the "External Wafer Fab Evaluation" checklist)

Name, number, etc., of the fab line at the external wafer fab plant

Name, number, etc., of wafer fab flow, fab traveler, etc., assigned by external wafer fab

Technology (bipolar, CMOS, etc.)

Test Data Supplied by External Wafer Fab

Evaluation of data by part manufacturer

Reason for using test

Conclusions from results

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5. DIE EVALUATION

Wafer Fab Process Baseline

Materials, construction, workmanship, etc.

Information obtained by destructive physical analysis (DPA), cross-section etc.

Obtain cross-section of area used for current density calculation

DPA report maintained on file for use as reference

Metallization

Number of levels (for "multi-level" metal, each level is separated by inter-metal dielectric)

Each level

Measured thickness

Location of measurement

Layers for each level (for "multi-layer" metal, each layer is not separated by inter-metal dielectric)

Each layer

Composition

Measured thickness

Location of measurement

Current density

Calculation made using paragraph A.3.5.5 in Appendix A, MIL-PRF-38535

Diagram of metal cross-sectional area used for calculation (may be obtained from DPA)

Show all dimensions

Show undercutting

Current used for calculation

Amount of current

Method used to obtain amount of current

Reason for using method

Calculations

Location on die for each calculation

Value of calculation

Reason for selecting locations

Worst case calculation

Location on die

Reason for selecting location

Discussion of worst case area that would result from using process limits (e.g., critical dimensions allowed for after-develop inspect of metal etch resist)

Discussion of worst case amount of current

Worst case value of calculation

Glassivation

Number of layers used for glassivation?

Each layer

Composition

Thickness

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5. DIE EVALUATION

Life Test by Part Manufacture

Source of parts used

- Manufacturer
 - Packaged by die manufacturer
 - Packaged by part manufacturer
- Distributor
- Other (specify)

Package

- Material
 - Plastic
 - Hermetic
 - Other (specify)
- Style

Designator used in part spec

Lead finish

Sample quantity

- Use sample size = 45, acc. nr. = 0
- Reason for using other sample size, acc. nr.

Testing of parts before life test

- None
- Tests used
 - Purpose

Test conditions

- Static or dynamic (specify)
- Minimum value of Vcc during test
- Ambient temperature
- Hours required to pass life test

Electrical tests

- Use electrical requirements (i.e., subgroups) from part spec, or most similar part spec
- End point electricals
 - Data log for pre-life test
 - Go-no go test for interim electricals
 - Data log for post-life test
- Deltas
 - Use parameters on part spec, most similar part specification, or determined by the part manufacturer to be critical for reliability

Other Testing by Part Manufacturer

- Submit information describing each test (use the items in # 3 for guidance)
- Discussion
 - Reason for using test
 - Conclusions from results