

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. -gjc.	03-03-13	Raymond Monnin
B	Update drawing to the latest requirements. -sld	07-03-27	Robert M. Heber
C	Made changes to paragraphs 1.3 and 1.4 along with footnote 3, sheet 3. Table I, made corrections to Supply currents test, Address input currents test, Enable input current tests, Output leakage current tests, and the Switching tests. Changed footnote 1 to add power supply turn on sequence. Made corrections to Figures 2, 3, 4, and 5. -sld	10-05-05	Charles F. Saffle



REV																			
SHEET																			
REV	C	C	C	C	C														
SHEET	15	16	17	18	19														
REV STATUS OF SHEETS	REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A	PREPARED BY Gary Zahn	<p align="center"><b>DEFENSE SUPPLY CENTER COLUMBUS</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="http://www.dscc.dla.mil/">http://www.dscc.dla.mil/</a></p>																		
<p align="center"><b>STANDARD MICROCIRCUIT DRAWING</b></p> <p align="center">THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Greg Cecil																			
	APPROVED BY Raymond Monnin	<p align="center"><b>MICROCIRCUIT, HYBRID, LINEAR, 64 CHANNEL, ANALOG MULTIPLEXER</b></p>																		
	DRAWING APPROVAL DATE 02-11-14																			
	REVISION LEVEL <b>C</b>																			SIZE A
		SHEET	1 OF 19																	



1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	96	Ceramic quad flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. <sup>1/</sup>

Positive supply voltage between +V <sub>EE</sub> and GND .....	+16.5 V dc
Negative supply voltage between -V <sub>EE</sub> and GND.....	-16.5 V dc
V <sub>REF</sub> to GND.....	+16.5 V dc
Digital input overvoltage range:	
V <sub>EN</sub> (pins 5, 6, 91, and 92).....	(< V <sub>REF</sub> + 4)V, (> GND - 4)V
V <sub>A</sub> (pins 1, 3, 93, and 95).....	(< V <sub>REF</sub> + 4)V, (> GND - 4)V
V <sub>B</sub> (pins 2, 4, 94, and 96).....	(< V <sub>REF</sub> + 4)V, (> GND - 4)V
Analog input overvoltage range .....	-18 V dc ≤ V <sub>S</sub> ≤ +18 V dc
Power dissipation (P <sub>D</sub> ), T <sub>C</sub> = -55°C to +125°C:	
Device type 01.....	99 mW
Device type 02.....	66 mW
Thermal resistance junction-to-case (θ <sub>JC</sub> ).....	5.5°C/W <sup>2/</sup>
Storage temperature.....	-65°C to +150°C
Lead temperature (soldering, 10 seconds) .....	+300°C

1.4 Recommended operating conditions.

Positive supply voltage (+V <sub>EE</sub> ) <sup>3/</sup> .....	+15 V dc
Negative supply voltage (-V <sub>EE</sub> ) <sup>3/</sup> .....	-15 V dc
V <sub>REF</sub> <sup>3/</sup> .....	+5 V dc
Logic low level voltage (V <sub>AL</sub> ).....	+0.8 V dc
Logic high level voltage (V <sub>AH</sub> ).....	+4.0 V dc
Case operating temperature range (T <sub>C</sub> ).....	-55°C to +125°C

## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

### DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

- <sup>1/</sup> Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.  
<sup>2/</sup> Based on the maximum power dissipation spread over all six die.  
<sup>3/</sup> Recommended power supply turn on sequence : +V<sub>EE</sub>, -V<sub>EE</sub>, followed by V<sub>REF</sub>.

<b>STANDARD MICROCIRCUIT DRAWING</b>  DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-00502</b>
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DEPARTMENT OF DEFENSE HANDBOOKS

- MIL-HDBK-103 - List of Standard Microcircuit Drawings.
- MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 shall include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. The manufacturer may eliminate, modify or optimize the tests and inspections herein, however the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. In addition, the modification in the QM plan shall not affect the form, fit, or function of the device for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Switching waveform(s). The switching waveform(s) shall be as specified on figure 4.

3.2.5 Block diagram. The block diagram shall be as specified on figure 5.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
Supply currents	+I <sub>EE</sub>	V <sub>EN(0-63)</sub> = V <sub>A(0-3)</sub> = V <sub>B(0-3)</sub> = 0	1,2,3	01	0.3	3	mA	
				02	0.2	2		
	-I <sub>EE</sub>	V <sub>EN(0-63)</sub> = V <sub>A(0-3)</sub> = V <sub>B(0-3)</sub> = 0	1,2,3	01	-3	-0.3	mA	
				02	-2	-0.2		
	+I <sub>SBY</sub>	V <sub>EN(0-63)</sub> = 4 V, V <sub>A(0-3)</sub> = V <sub>B(0-3)</sub> = 0 <u>3/</u>	1,2,3	01	0.3	3	mA	
				02	0.2	2		
	-I <sub>SBY</sub>	V <sub>EN(0-63)</sub> = 4 V, V <sub>A(0-3)</sub> = V <sub>B(0-3)</sub> = 0 <u>3/</u>	1,2,3	01	-3	-0.3	mA	
				02	-2	-0.2		
Address input currents	I <sub>AL(0-3)B</sub>	V <sub>B</sub> = 0 V <u>2/</u>	1,2,3	01,02	-2	2	μA	
	I <sub>AH(0-3)B</sub>	V <sub>B</sub> = 5 V <u>2/</u>	1,2,3	01,02	-2	2	μA	
	I <sub>AL(0-3)A</sub>	V <sub>A</sub> = 0 V <u>2/</u>	1,2,3	01	-4	4	μA	
				02	-2	2		
	I <sub>AH(0-3)A</sub>	V <sub>A</sub> = 5 V <u>2/</u>	1,2,3	01	-4	4	μA	
				02	-2	2		
	Enable input current	I <sub>ENL(0-15)</sub>	V <sub>EN(0-15)</sub> = 0 V	1,2,3	01,02	-1	1	μA
		I <sub>ENH(0-15)</sub>	V <sub>EN(0-15)</sub> = 5 V	1,2,3	01,02	-1	1	μA
I <sub>ENL(16-31)</sub>		V <sub>EN(16-31)</sub> = 0 V	1,2,3	01,02	-1	1	μA	
I <sub>ENH(16-31)</sub>		V <sub>EN(16-31)</sub> = 5 V	1,2,3	01,02	-1	1	μA	
I <sub>ENL(32-47)</sub>		V <sub>EN(32-47)</sub> = 0 V	1,2,3	01	-2	2	μA	
				02	-1	1		
I <sub>ENH(32-47)</sub>		V <sub>EN(32-47)</sub> = 5 V	1,2,3	01	-2	2	μA	
				02	-1	1		
I <sub>ENL(48-63)</sub>	V <sub>EN(48-63)</sub> = 0 V	1,2,3	01	-2	2	μA		
			02	-1	1			
I <sub>ENH(48-63)</sub>	V <sub>EN(48-63)</sub> = 5 V	1,2,3	01	-2	2	μA		
			02	-1	1			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <sup>1/ 2/</sup> -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Positive input leakage current (CH0-CH63)	+I <sub>SOFFOUTPUT(ALL)</sub>	V <sub>IN</sub> = +10 V, V <sub>EN</sub> = 4 V, output and all unused inputs = -10 V <u>4/ 5/</u>	1,2,3	01,02	-100	+700	nA
	+I <sub>SOFFCURRENT(ALL)</sub>	V <sub>IN</sub> = +10 V, V <sub>EN</sub> = 4 V, output and all unused inputs = -10 V <u>4/ 5/</u>	1,2,3	01,02	-100	+700	nA
Negative input leakage current (CH0-CH63)	-I <sub>SOFFOUTPUT(ALL)</sub>	V <sub>IN</sub> = -10 V, V <sub>EN</sub> = 4 V, output and all unused inputs = +10 V <u>4/ 5/</u>	1,2,3	01,02	-100	+700	nA
	-I <sub>SOFFCURRENT(ALL)</sub>	V <sub>IN</sub> = -10 V, V <sub>EN</sub> = 4 V, output and all unused inputs = +10 V <u>4/ 5/</u>	1,2,3	01,02	-100	+700	nA
Output leakage current outputs (pins 25, 26, 68, and 70) Currents (pins 67 and 69 Device Type 01 only)	+I <sub>DOFFOUTPUT(ALL)</sub>	V <sub>OUT</sub> = +10 V, V <sub>EN</sub> = 4 V, output and all unused inputs = -10 V <u>5/ 6/</u>	1,2,3	01,02	-100	+100	nA
	+I <sub>DOFFCURRENT(ALL)</sub>	V <sub>OUT</sub> = +10 V, V <sub>EN</sub> = 4 V, output and all unused inputs = -10 V <u>5/ 6/</u>	1,2,3	01,02	-100	+100	nA
	-I <sub>DOFFOUTPUT(ALL)</sub>	V <sub>OUT</sub> = -10 V, V <sub>EN</sub> = 4 V, output and all unused inputs = +10 V <u>5/ 6/</u>	1,2,3	01,02	-100	+100	nA
	-I <sub>DOFFCURRENT(ALL)</sub>	V <sub>OUT</sub> = -10 V, V <sub>EN</sub> = 4 V, output and all unused inputs = +10 V <u>5/ 6/</u>	1,2,3	01,02	-100	+100	nA
Input clamped voltage (CH0-CH63)	+V <sub>CLMP(0-63)</sub>	V <sub>EN</sub> = 4 V, all unused inputs are open <u>5/</u>	1	01,02	18.0	23.0	V
			2		18.0	23.5	
			3		17.5	22.5	
	-V <sub>CLMP(0-63)</sub>	V <sub>EN</sub> = 4 V, all unused inputs are open <u>5/</u>	1	01,02	-23.0	-18.0	V
			2		-23.5	-18.0	
			3		-22.5	-17.5	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> <u>2/</u> -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Switch ON resistance outputs (pins 25, 26, 68, and 70)	R <sub>DS(ON)(0-63)A</sub>	V <sub>IN</sub> = +15 V, V <sub>EN</sub> = 0.8 V, I <sub>OUT</sub> = -1 mA <u>4/</u> <u>5/</u> <u>7/</u>	1,2,3	01,02	500	3000	Ω
	R <sub>DS(ON)(0-63)B</sub>	V <sub>IN</sub> = +5 V, V <sub>EN</sub> = 0.8 V, I <sub>OUT</sub> = -1 mA <u>4/</u> <u>5/</u> <u>7/</u>	1,2,3	01,02	500	3000	Ω
	R <sub>DS(ON)(0-63)C</sub>	V <sub>IN</sub> = -5 V, V <sub>EN</sub> = 0.8 V, I <sub>OUT</sub> = +1 mA <u>4/</u> <u>5/</u> <u>7/</u>	1,2,3	01,02	500	3000	Ω
Switch ON resistance outputs (pins 67 and 69 Device type 01 only)	R <sub>DS(ON)(32-63)A</sub>	V <sub>IN</sub> = +15 V, V <sub>EN</sub> = 0.8 V, I <sub>OUT</sub> = -1 mA <u>4/</u> <u>5/</u> <u>7/</u>	1,2,3	01	500	3000	Ω
	R <sub>DS(ON)(32-63)B</sub>	V <sub>IN</sub> = +5 V, V <sub>EN</sub> = 0.8 V, I <sub>OUT</sub> = -1 mA <u>4/</u> <u>5/</u> <u>7/</u>	1,2,3	01	500	3000	Ω
	R <sub>DS(ON)(32-63)C</sub>	V <sub>IN</sub> = -5 V, V <sub>EN</sub> = 0.8 V, I <sub>OUT</sub> = +1 mA <u>4/</u> <u>5/</u> <u>7/</u>	1,2,3	01	500	3000	Ω
Switching tests	t <sub>AHL</sub>	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 50 pF, see figure 4.	9,10,11	01,02	10	1500	ns
	t <sub>ALH</sub>	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 50 pF, see figure 4.	9,10	01,02	10	2000	ns
			11		10	5000	
	t <sub>ONEN</sub>	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 50 pF, see figure 4.	9,10,11	01,02	10	1500	ns
t <sub>OFFEN</sub>	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 50 pF, see figure 4.	9,10,11	01,02	10	1000	ns	

- 1/ +V<sub>EE</sub> = +15 V dc, -V<sub>EE</sub> = -15 V dc, and V<sub>REF</sub> = +5 V dc, unless otherwise specified. Recommended power supply turn on sequence : +V<sub>EE</sub>, -V<sub>EE</sub>, followed by V<sub>REF</sub>.
- 2/ Measure inputs sequentially. Ground all unused inputs. V<sub>A</sub> is the applied input voltage to the address lines A(0-3). V<sub>B</sub> is the applied input voltage to the address lines B(0-3).
- 3/ If not tested, shall be guaranteed to the limits specified in table I.
- 4/ V<sub>IN</sub> is the applied input voltage to the input channels (CH0-CH63).
- 5/ V<sub>EN</sub> is the applied input voltage to the enable lines EN(0-15), EN(16-31), EN(32-47), and EN(48-63).
- 6/ V<sub>OUT</sub> is the applied input voltage to the output lines (OUTPUT(1-15), OUTPUT(16-31), OUTPUT(32-47), OUTPUT(48-63), CURRENT(32-47), and CURRENT(48-63). (Current outputs for device type 01 only).
- 7/ Negative current is the current flowing out of each of the pins. Positive current is the current flowing into each of the pins.

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Case outline X.

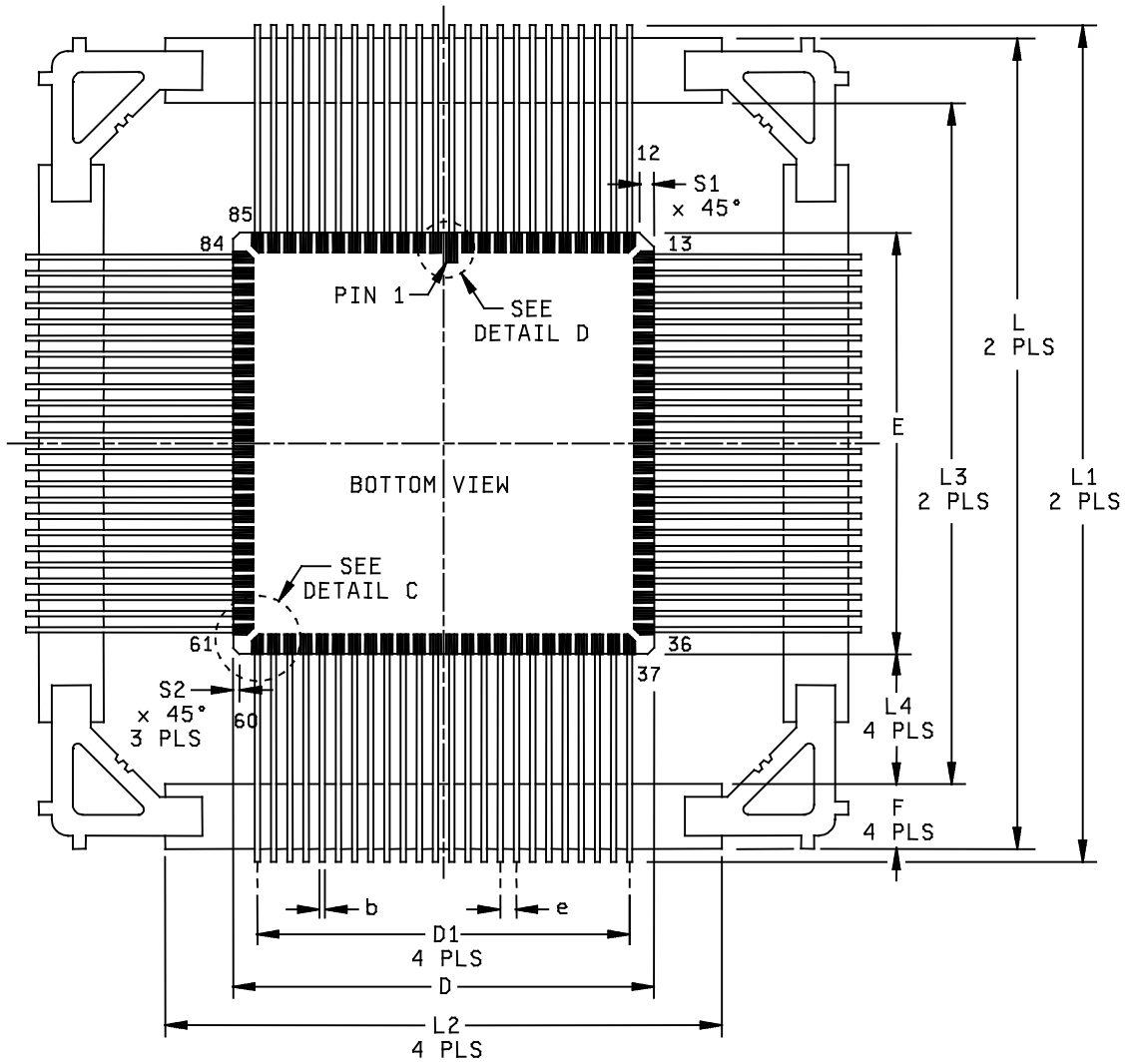


FIGURE 1. Case outline(s).

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Case outline X - Continued.

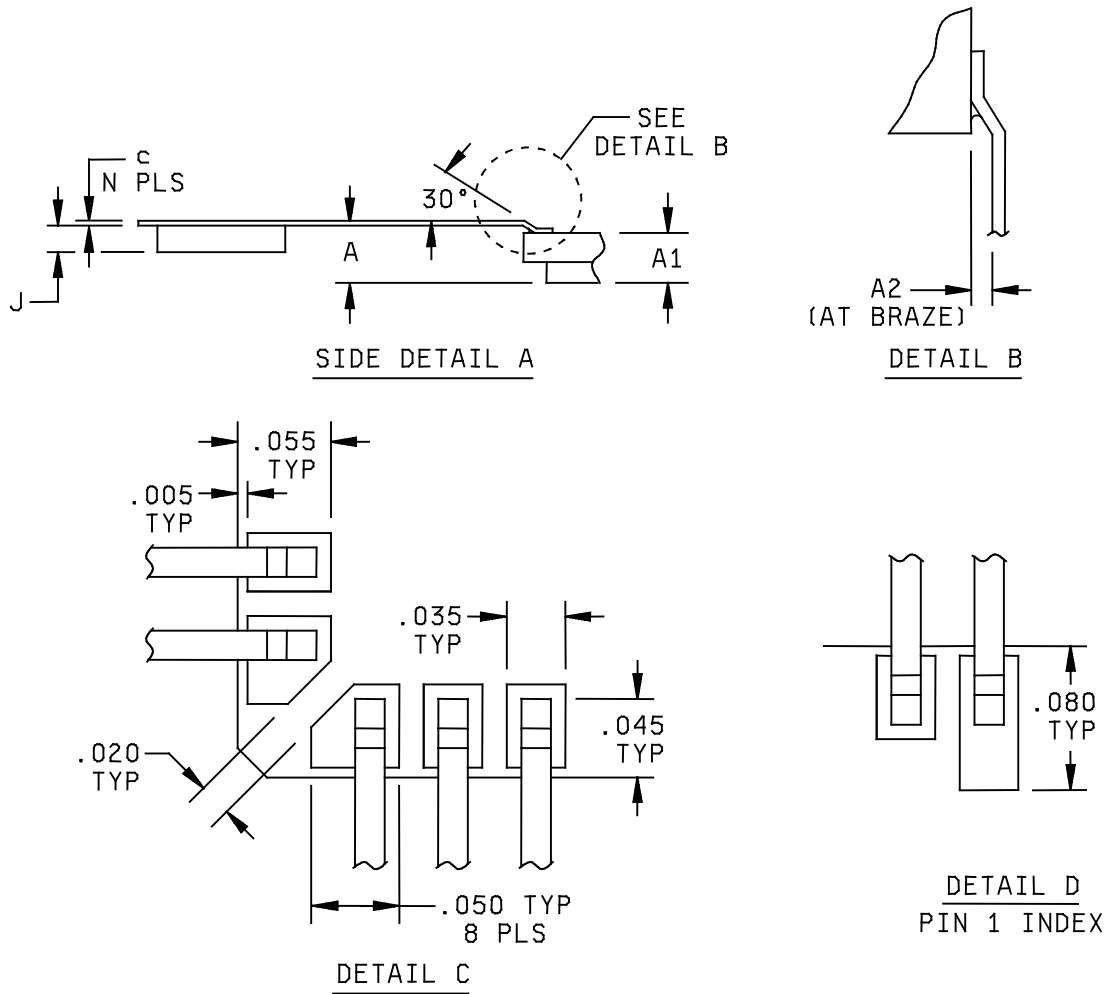


FIGURE 1. Case outline(s) - Continued.

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Case outline X - Continued.

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
A1		.180		4.57
A2	.005	.011	0.13	0.28
b	.0135	.0195	0.34	0.50
c	.005	.008	0.13	0.20
D/E	1.287	1.313	32.69	33.35
D1	1.145	1.155	29.08	29.34
e	.050 BSC		1.27 BSC	
F	.200 TYP		5.08 TYP	
J	.035 TYP		0.89 TYP	
L	2.490	2.510	63.25	63.75
L1		2.580		65.53
L2	1.700	1.740	43.18	44.20
L3	2.090	2.110	53.09	53.59
L4	.400 TYP		10.16 TYP	
N	96		96	
S1	.030 TYP		0.76 TYP	
S2	.015 TYP		0.38 TYP	

NOTES:

1. Pin 1 is indicated by an ESD triangle on top of the package and by an index on the bottom of the package.
2. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
3. N equals 96, the total number of leads on the package.
4. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

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Device type	01				
Case outline	X				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A2	33	CH11	65	CH49
2	B2	34	CH27	66	CH48
3	A3	35	CH12	67	OUTPUT I(48-63)
4	B3	36	CH28	68	OUTPUT V(48-63)
5	$\overline{EN}$ (0-15)	37	CH13	69	OUTPUT I(32-47)
6	$\overline{EN}$ (16-31)	38	CH29	70	OUTPUT V(32-47)
7	CH0	39	CH14	71	GND
8	CH16	40	CH30	72	GND
9	CH1	41	CH15	73	CH47
10	CH17	42	CH31	74	CH46
11	CH2	43	NC	75	CH45
12	CH18	44	+V <sub>EE</sub>	76	CH44
13	CH3	45	NC	77	CH43
14	CH19	46	-V <sub>EE</sub>	78	CH42
15	CH4	47	NC	79	CH41
16	CH20	48	V <sub>REF</sub>	80	CH40
17	CH5	49	NC	81	CH39
18	CH21	50	Case GND	82	CH38
19	CH6	51	CH63	83	CH37
20	CH22	52	CH62	84	CH36
21	CH7	53	CH61	85	CH35
22	CH23	54	CH60	86	CH34
23	GND	55	CH59	87	CH33
24	GND	56	CH58	88	CH32
25	OUTPUT V(0-15)	57	CH57	89	GND
26	OUTPUT V(16-31)	58	CH56	90	GND
27	CH8	59	CH55	91	$\overline{EN}$ (48-63)
28	CH24	60	CH54	92	$\overline{EN}$ (32-47)
29	CH9	61	CH53	93	A0
30	CH25	62	CH52	94	B0
31	CH10	63	CH51	95	A1
32	CH26	64	CH50	96	B1

NOTE: NC is a no connect pin. NC pins should be grounded to eliminate or minimize electrostatic discharge (ESD) or static buildup.

FIGURE 2. Terminal connections.

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Device type	02				
Case outline	X				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A2	33	CH11	65	CH49
2	B2	34	CH27	66	CH48
3	A3	35	CH12	67	NC
4	B3	36	CH28	68	OUTPUT V(48-63)
5	$\overline{EN}$ (0-15)	37	CH13	69	NC
6	$\overline{EN}$ (16-31)	38	CH29	70	OUTPUT V(32-47)
7	CH0	39	CH14	71	GND
8	CH16	40	CH30	72	GND
9	CH1	41	CH15	73	CH47
10	CH17	42	CH31	74	CH46
11	CH2	43	NC	75	CH45
12	CH18	44	+V <sub>EE</sub>	76	CH44
13	CH3	45	NC	77	CH43
14	CH19	46	-V <sub>EE</sub>	78	CH42
15	CH4	47	NC	79	CH41
16	CH20	48	V <sub>REF</sub>	80	CH40
17	CH5	49	NC	81	CH39
18	CH21	50	Case GND	82	CH38
19	CH6	51	CH63	83	CH37
20	CH22	52	CH62	84	CH36
21	CH7	53	CH61	85	CH35
22	CH23	54	CH60	86	CH34
23	GND	55	CH59	87	CH33
24	GND	56	CH58	88	CH32
25	OUTPUT V(0-15)	57	CH57	89	GND
26	OUTPUT V(16-31)	58	CH56	90	GND
27	CH8	59	CH55	91	$\overline{EN}$ (48-63)
28	CH24	60	CH54	92	$\overline{EN}$ (32-47)
29	CH9	61	CH53	93	A0
30	CH25	62	CH52	94	B0
31	CH10	63	CH51	95	A1
32	CH26	64	CH50	96	B1

NOTE: NC is a no connect pin. NC pins should be grounded to eliminate or minimize electrostatic discharge (ESD) or static buildup.

FIGURE 2. Terminal connections.

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Truth table (CH0-CH15) and (CH16-CH31)							
B3	B2	B1	B0	$\overline{EN}$ (0-15)	"ON" Channel <u>1</u> /	$\overline{EN}$ (16-31)	"ON" Channel <u>2</u> /
X	X	X	X	H	None	H	None
L	L	L	L	L	CH0	L	CH16
L	L	L	H	L	CH1	L	CH17
L	L	H	L	L	CH2	L	CH18
L	L	H	H	L	CH3	L	CH19
L	H	L	L	L	CH4	L	CH20
L	H	L	H	L	CH5	L	CH21
L	H	H	L	L	CH6	L	CH22
L	H	H	H	L	CH7	L	CH23
H	L	L	L	L	CH8	L	CH24
H	L	L	H	L	CH9	L	CH25
H	L	H	L	L	CH10	L	CH26
H	L	H	H	L	CH11	L	CH27
H	H	L	L	L	CH12	L	CH28
H	H	L	H	L	CH13	L	CH29
H	H	H	L	L	CH14	L	CH30
H	H	H	H	L	CH15	L	CH31

1/ Between (CH0-CH15) and OUTPUT(0-15).

2/ Between (CH16-CH31) and OUTPUT(16-31).

Truth table (CH32-CH47) and (CH48-CH63)							
A3	A2	A1	A0	$\overline{EN}$ (32-47)	"ON" Channel <u>1</u> /	$\overline{EN}$ (48-63)	"ON" Channel <u>2</u> /
X	X	X	X	H	None	H	None
L	L	L	L	L	CH32	L	CH48
L	L	L	H	L	CH33	L	CH49
L	L	H	L	L	CH34	L	CH50
L	L	H	H	L	CH35	L	CH51
L	H	L	L	L	CH36	L	CH52
L	H	L	H	L	CH37	L	CH53
L	H	H	L	L	CH38	L	CH54
L	H	H	H	L	CH39	L	CH55
H	L	L	L	L	CH40	L	CH56
H	L	L	H	L	CH41	L	CH57
H	L	H	L	L	CH42	L	CH58
H	L	H	H	L	CH43	L	CH59
H	H	L	L	L	CH44	L	CH60
H	H	L	H	L	CH45	L	CH61
H	H	H	L	L	CH46	L	CH62
H	H	H	H	L	CH47	L	CH63

1/ Between (CH32-CH47) and OUTPUT(32-47) and CURRENT(32-47).

2/ Between (CH48-CH63) and OUTPUT(48-63) and CURRENT(48-63).

FIGURE 3. Truth table(s). (Device type 01).

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Truth table (CH0-CH15) and (CH16-CH31)							
B3	B2	B1	B0	$\overline{EN}$ (0-15)	"ON" Channel <u>1/</u>	$\overline{EN}$ (16-31)	"ON" Channel <u>2/</u>
X	X	X	X	H	None	H	None
L	L	L	L	L	CH0	L	CH16
L	L	L	H	L	CH1	L	CH17
L	L	H	L	L	CH2	L	CH18
L	L	H	H	L	CH3	L	CH19
L	H	L	L	L	CH4	L	CH20
L	H	L	H	L	CH5	L	CH21
L	H	H	L	L	CH6	L	CH22
L	H	H	H	L	CH7	L	CH23
H	L	L	L	L	CH8	L	CH24
H	L	L	H	L	CH9	L	CH25
H	L	H	L	L	CH10	L	CH26
H	L	H	H	L	CH11	L	CH27
H	H	L	L	L	CH12	L	CH28
H	H	L	H	L	CH13	L	CH29
H	H	H	L	L	CH14	L	CH30
H	H	H	H	L	CH15	L	CH31

1/ Between (CH0-CH15) and OUTPUT(0-15).

2/ Between (CH16-CH31) and OUTPUT(16-31).

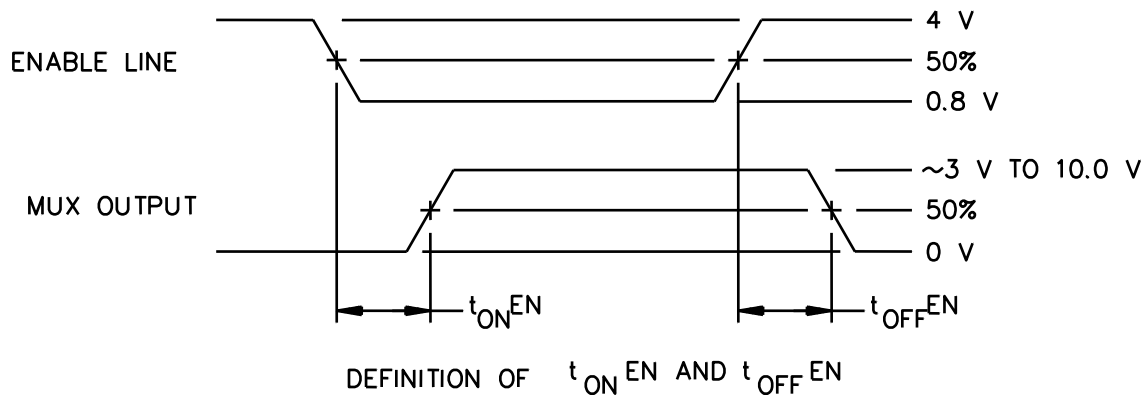
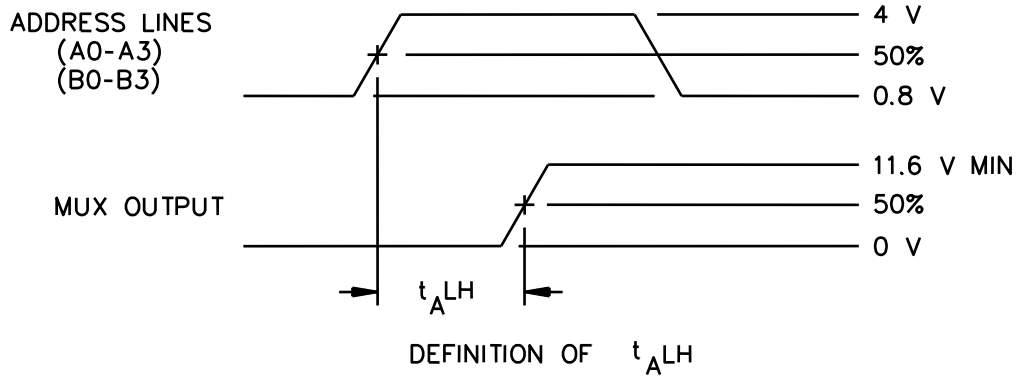
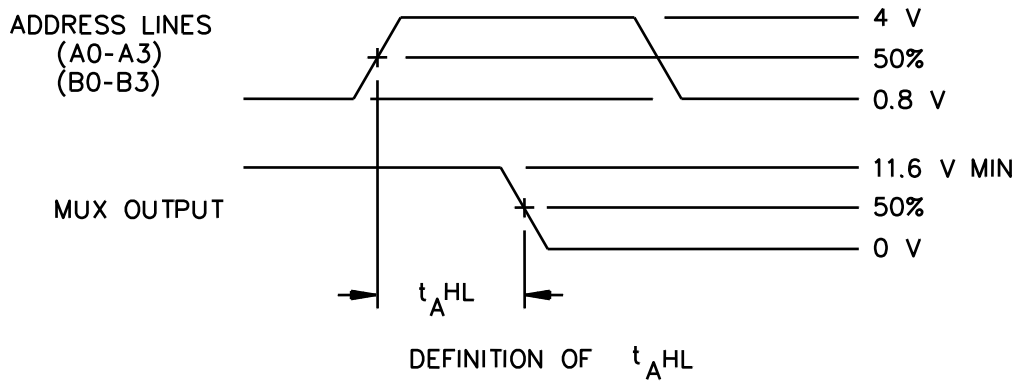
Truth table (CH32-CH47) and (CH48-CH63)							
A3	A2	A1	A0	$\overline{EN}$ (32-47)	"ON" Channel <u>1/</u>	$\overline{EN}$ (48-63)	"ON" Channel <u>2/</u>
X	X	X	X	H	None	H	None
L	L	L	L	L	CH32	L	CH48
L	L	L	H	L	CH33	L	CH49
L	L	H	L	L	CH34	L	CH50
L	L	H	H	L	CH35	L	CH51
L	H	L	L	L	CH36	L	CH52
L	H	L	H	L	CH37	L	CH53
L	H	H	L	L	CH38	L	CH54
L	H	H	H	L	CH39	L	CH55
H	L	L	L	L	CH40	L	CH56
H	L	L	H	L	CH41	L	CH57
H	L	H	L	L	CH42	L	CH58
H	L	H	H	L	CH43	L	CH59
H	H	L	L	L	CH44	L	CH60
H	H	L	H	L	CH45	L	CH61
H	H	H	L	L	CH46	L	CH62
H	H	H	H	L	CH47	L	CH63

1/ Between (CH32-CH47) and OUTPUT(32-47).

2/ Between (CH48-CH63) and OUTPUT(48-63).

FIGURE 3. Truth table(s). (Device type 02)

<b>STANDARD MICROCIRCUIT DRAWING</b>  DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-00502</b>
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NOTE:  $f = 10 \text{ kHz}$ , duty cycle = 50%.

FIGURE 4. Switching test waveform(s).

<b>STANDARD MICROCIRCUIT DRAWING</b>  DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-00502</b>
		REVISION LEVEL <b>C</b>	SHEET <b>15</b>

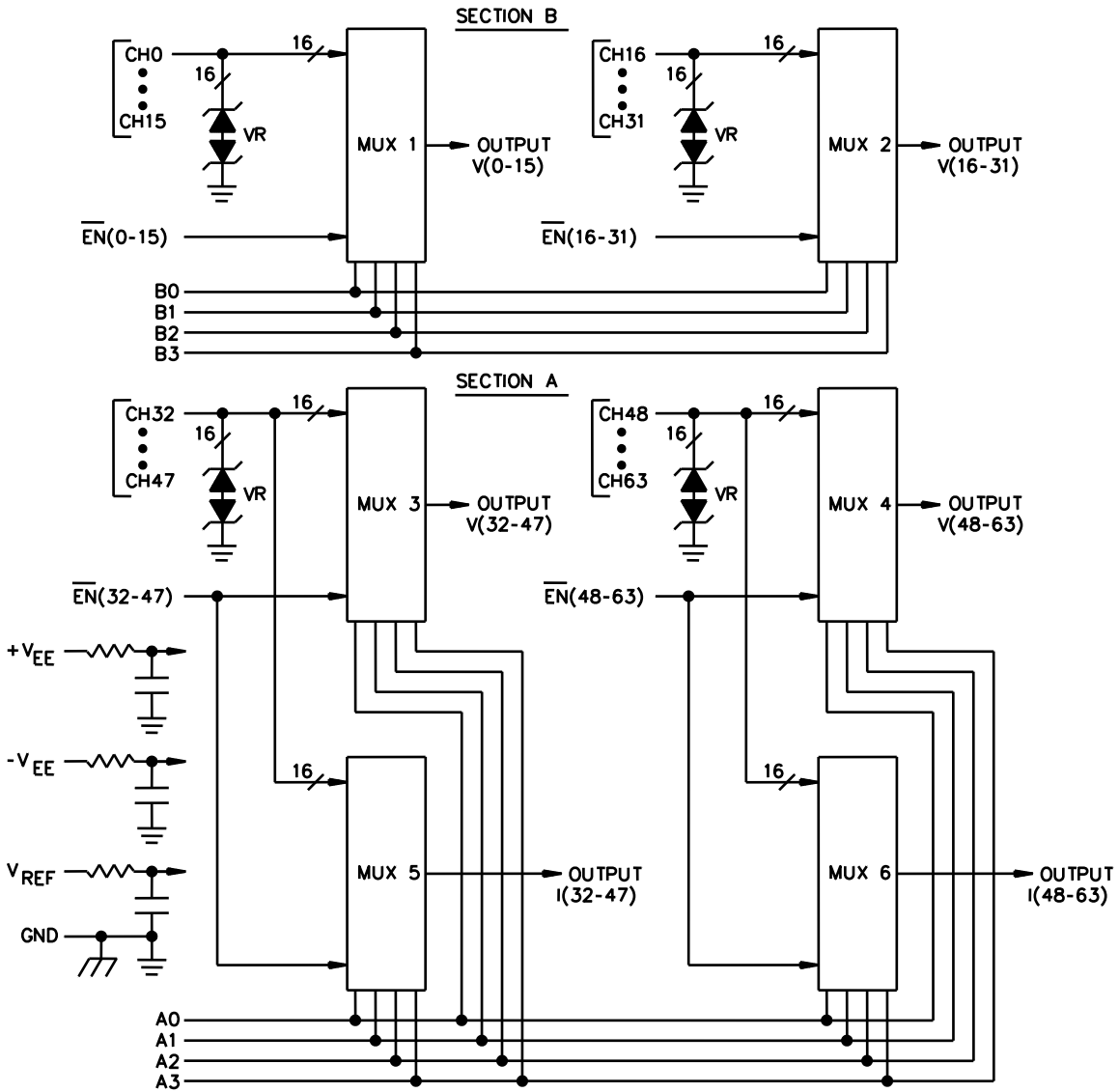


FIGURE 5. Block diagram. (Device Type 01)

<b>STANDARD MICROCIRCUIT DRAWING</b>  DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-00502</b>
		REVISION LEVEL <b>C</b>	SHEET <b>16</b>

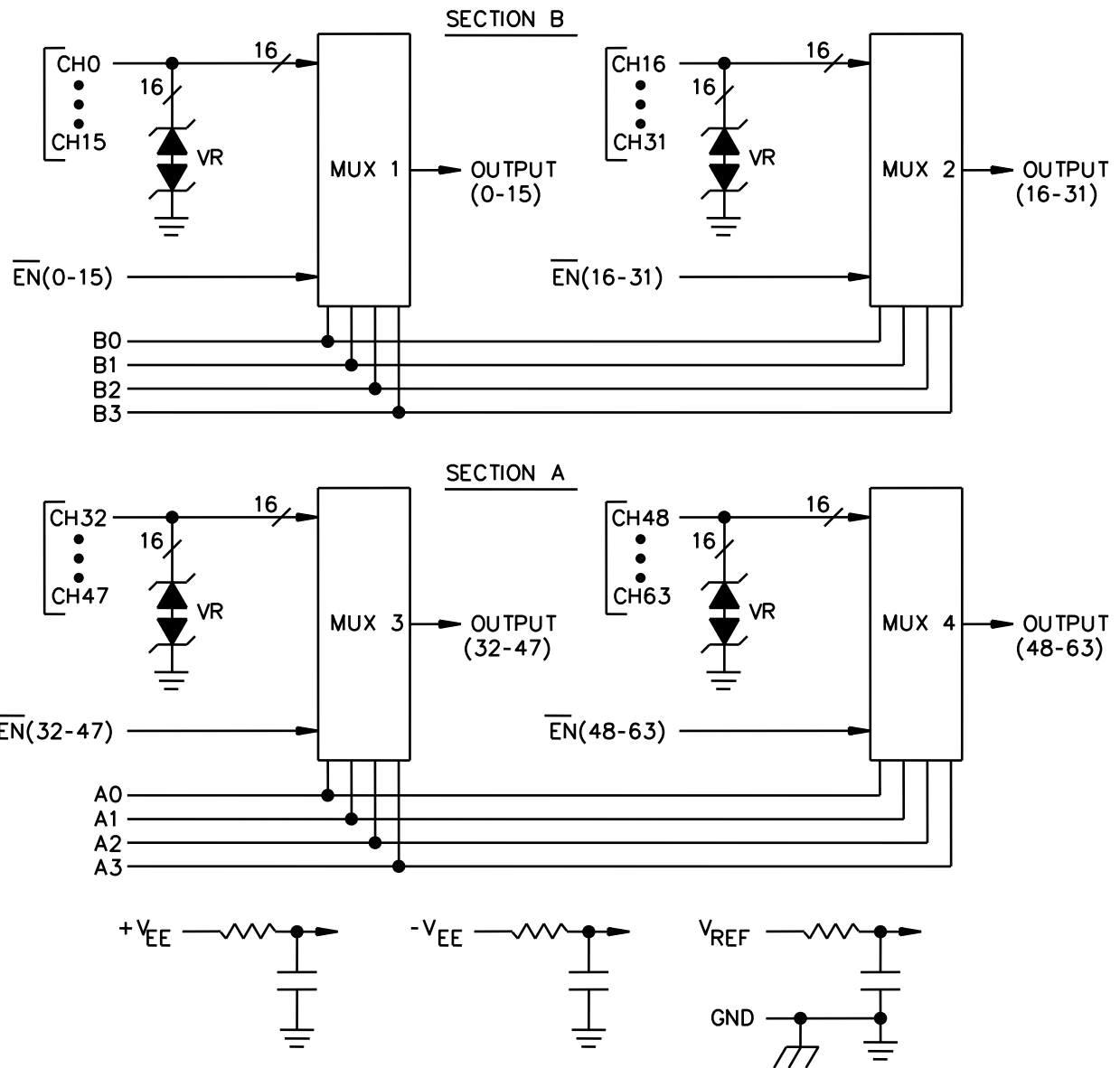


FIGURE 5. Block diagram - Continued. (Device Type 02)

<b>STANDARD MICROCIRCUIT DRAWING</b>  DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-00502</b>
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TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1, 9
Final electrical parameters	1*, 2, 3, 9, 10, 11
Group A test requirements	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters	1, 2, 3, 9, 10, 11
End-point electrical parameters for radiation hardness assurance (RHA) devices	Not applicable

\* PDA applies to subgroup 1.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
  - (2) T<sub>A</sub> as specified in accordance with table I of method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, 6, 7, and 8 shall be omitted.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

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4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test, method 1005 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
  - (2)  $T_A$  as specified in accordance with table I of method 1005 of MIL-STD-883.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-1081.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

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		REVISION LEVEL C	SHEET <b>19</b>

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-05-05

Approved sources of supply for SMD 5962-00502 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-0050201KXC	88379	ACT8500-S
5962-0050202KXC	88379	ACT8501-S

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

88379

Vendor name and address

Aeroflex Plainview Incorporated,  
 (Aeroflex Microelectronics Solutions)  
 35 South Service Road  
 Plainview, NY 11803-4193

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.