

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make title and symbol changes to both tests specified under the UVLO section in table I. - ro	00-12-18	R. MONNIN
B	Made a change to the minimum ambient operating temperature in 1.4 and table I. Changes also made to the delay to output test and PSRR test in table I. - rp	01-03-21	R. MONNIN
C	Add footnote to the error amp section as specified in table I and add footnote to figure 2. - ro	01-07-10	R. MONNIN
D	Make changes to output voltage test, total output variation test, and input voltage test as specified in table I. Also, make change to footnote 2/ as specified in table I and footnote 1/ as specified in figure 2. - ro	01-08-16	R. MONNIN
E	Add new footnote to figure 2 and to the Oscillator section as specified under table I. Make change to RTCT description as specified under figure 2. Make change to V_{IN} test condition as specified under table I. - ro	03-09-19	R. MONNIN
F	Add a new footnote under paragraph 1.5 and Table I. - ro	05-06-03	R. MONNIN
G	Add OSCGND and V_C pin descriptions to figure 2. - ro	08-10-16	R. HEBER

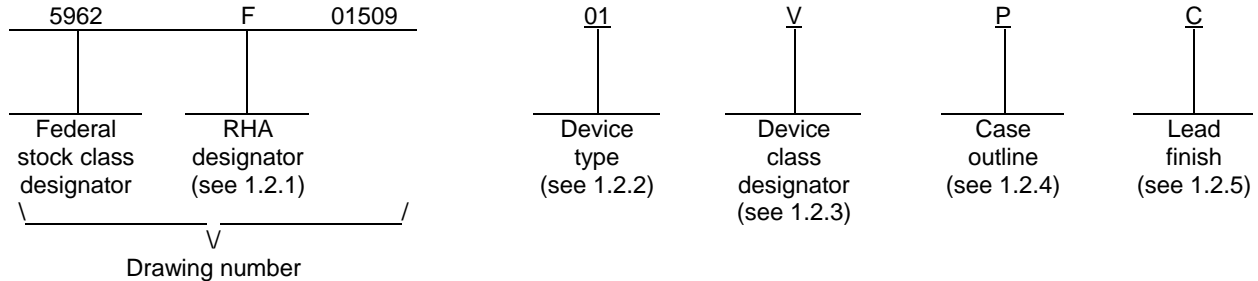


REV																				
SHEET																				
REV	G	G	G	G	G	G	G	G												
SHEET	15	16	17	18	19	20	21	22												
REV STATUS OF SHEETS	REV			G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			
PMIC N/A	PREPARED BY RICK OFFICER								DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 http://www.dscc.dla.mil											
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY RAJESH PITHADIA																			
	APPROVED BY RAYMOND MONNIN								MICROCIRCUIT, DIGITAL-LINEAR, CURRENT MODE PULSE WIDTH MODULATOR, MONOLITHIC SILICON											
	DRAWING APPROVAL DATE 00-11-30																			
	REVISION LEVEL G								SIZE A	CAGE CODE 67268	5962-01509									
										SHEET 1 OF 22										

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	IS-1845ASRH	High speed, current mode pulse width modulator

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
P	CDIP2-T8	8	Dual-in-line
X	See figure 1	18	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/

Supply voltage (V _{CC})	+35 V dc
Maximum storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+265°C
Power dissipation (P _D)	1.5 W
Junction temperature (T _J)	+175°C
Thermal resistance, junction-to-case (θ _{JC}):	
Case P	25°C/W
Case X	8°C/W
Thermal resistance, junction-to-ambient (θ _{JA}):	
Case P	100°C/W
Case X	90°C/W

1.4 Recommended operating conditions.

Supply voltage (V _{CC})	+12 V dc to +20 V dc
Ambient operating temperature range (TA)	-50°C to +125°C

1.5 Radiation features. 2/

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s)	300 Krads (Si)
Latch-up	None 3/
Single event latch-up	> 83 MEV / (cm ² /mg) 3/
Single event upset	> 35 MEV / (cm ² /mg) 3/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ These parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A.
- 3/ Guaranteed by design or process but not tested.

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2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 116 (see MIL-PRF-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/2/</u> -50°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Reference section							
Output voltage	V _{REF}	I _{OUT} = 1 mA	1	01	4.90	5.10	V
			M,D,P,L,R,F		1	4.90	
Line regulation	V _{RLINE}	12 V ≤ V _{CC} ≤ 25 V	1,2,3	01	-20	20	mV
			M,D,P,L,R,F		1	-20	
Load regulation	V _{RLOAD}	1 mA ≤ I _O ≤ 20 mA	1	01	-25	25	mV
			2,3		-60	60	
			M,D,P,L,R,F		1	-60	
Total output variation	V _{WC}	Line, Load, Temp	1,2,3	01	4.82	5.18	V
			M,D,P,L,R,F		1	4.82	
Output short circuit	I _{SC}		1,2,3	01	-100	-30	mA
			M,D,P,L,R,F		1	-100	
Oscillator section <u>3/</u>							
Initial accuracy	IA	T _A = 25°C	4	01	47	57	kHz
			M,D,P,L,R,F		4	47	
Voltage stability	VS	12 V ≤ V _{CC} ≤ 25 V	4,5,6	01	-1	1	%
			M,D,P,L,R,F		4	-1	
Discharge current	I _{DIS}	V _{RT/CT} = 2 V	1,2,3	01	7.5	14	mA
			M,D,P,L,R,F		1	7.5	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/2/</u> -50°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Error Amp section <u>4/</u>							
Input voltage	V _{IN}	V _{COMP} = 2.5 V	1,2,3	01	2.42	2.58	V
			M,D,P,L,R,F		1	2.42	
Input bias current	I _{IB}		1,2,3	01	-2	2	μA
			M,D,P,L,R,F		1	-2	
Open loop voltage gain	A _{VOL}	2 V ≤ V _{COMP} ≤ 4 V	4	01	65		dB
			5,6		60		
			M,D,P,L,R,F		4	60	
Unity gain bandwidth <u>5/</u>	UGBW	T _A = +25°C	4	01	2		MHz
Power supply rejection ratio	PSRR (EA)	12 V ≤ V _{CC} ≤ 25 V	4	01	60		dB
			5,6		55		
			M,D,P,L,R,F		4	55	
Output sink current	I _{SINK}	V _{FB} = 2.7 V, V _{COMP} = 1.1 V	1	01	4.5		mA
			2,3		4.0		
			M,D,P,L,R,F		1	4.0	
Output source current	I _{SC}	V _{FB} = 2.3 V, V _{COMP} = 5 V	1,2,3	01		-0.5	mA
			M,D,P,L,R,F		1		
High output voltage	V _{OH(EA)}	V _{FB} = 2.3 V, I _L = 500 μA	1,2,3	01	5		V
			M,D,P,L,R,F		1	5	
Low output voltage	V _{OL(EA)}	V _{FB} = 2.7 V, I _L = 500 μA	1,2,3	01		1.1	V
			M,D,P,L,R,F		1		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/2/</u> -50°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
Output section								
Low output voltage	V _{OL(OS)}	I _{SINK} = 20 mA	1	01		0.85	V	
			2,3			0.90		
			M,D,P,L,R,F		1			0.90
		I _{SINK} = 200 mA	1			2.2		
			2,3			2.5		
			M,D,P,L,R,F		1	2.5		
High output voltage	V _{OH(OS)}	I _{SINK} = 20 mA	1,2,3	01	13	16	V	
			M,D,P,L,R,F		1	13		16
		I _{SINK} = 200 mA	1		12	16		
			2,3		11	16		
			M,D,P,L,R,F		1	11		16
Current Sense section								
Gain <u>6/</u>	A _V		4,5,6	01	3	4	V/V	
			M,D,P,L,R,F		4	3		4
Maximum input signal voltage	V _{INS}	V _{COMP} = 5 V	1,2,3	01	0.8	1.1	V	
			M,D,P,L,R,F		1	0.8		1.1
Input bias current	I _{IB}		1,2,3	01	-10		μA	
			M,D,P,L,R,F		1	-10		
Delay to output <u>5/</u>		V _{ISENSE} = 0 V to 3 V	4,5,6	01		125	ns	
Power supply rejection ratio	PSRR (CS)	12 V ≤ V _{CC} ≤ 25 V	1,2,3	01	70		dB	
			M,D,P,L,R,F		1	70		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions ^{1/ 2/} -50°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Undervoltage Lockout (UVLO) section							
Stop threshold voltage	V _{STOP}		1,2,3	01	7.0	8.2	V
			M,D,P,L,R,F		1	7.0	
Start threshold voltage	V _{START}		1,2,3	01	7.8	9.0	V
			M,D,P,L,R,F		1	7.8	
Pulse Width Modulation (PWM) section							
Maximum duty cycle	DC _{MAX}		1,2,3	01	47	50	%
			M,D,P,L,R,F		1	47	
Minimum duty cycle ^{5/}	DC _{MIN}		1,2,3	01		0	%
Total Standby Current section							
Startup current	I _{SU}		1	01		0.5	mA
			2,3			1.0	
			M,D,P,L,R,F		1		
Operating supply current	I _{CC}	V _{FB} – V _{ISENSE} = 0 V	1,2,3	01		17	mA
			M,D,P,L,R,F		1		
Zener voltage	V _Z	I _{CC} = 25 mA	1,2,3	01	30		V
			M,D,P,L,R,F		1	30	

- ^{1/} Devices supplied to this drawing have been characterized through all levels M, D, P, L, R, F of irradiation. However, this device is only tested at the “F” level. Pre and Post irradiation values are identical unless otherwise specified in table I. When performed post irradiation electrical measurements for any RHA level, T_A = +25°C.
- ^{2/} These parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A.
- ^{3/} Part should be operated with C_T = 3.3 nF and R_T = 10 kΩ timing components only.
- ^{4/} Grounding the COMP pin does not disable the output. The output may be disabled by raising the voltage on the ISENSE pin to > 1.1 V.
- ^{5/} This parameter is guaranteed but not tested. This parameter is characterized upon initial design or process changes which affect this characteristic.
- ^{6/} Gain is defined as ΔV_{COMP} / ΔV_{CS}, 0.1 ≤ V_{CS} ≤ 0.8 V.

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Case X

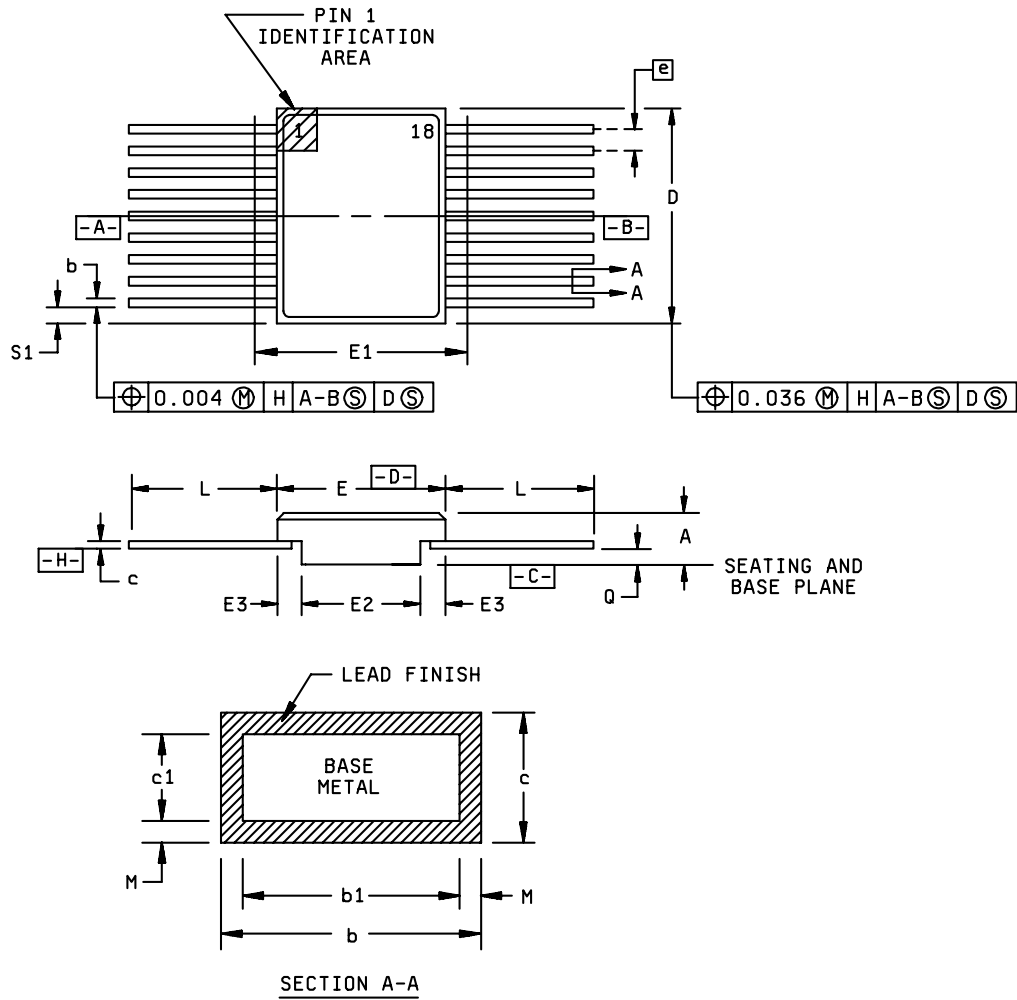


FIGURE 1. Case outline.

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Case X

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	0.045	0.115	1.14	2.92	
b	0.015	0.022	0.38	0.56	
b1	0.015	0.019	0.38	0.48	
c	0.004	0.009	0.10	0.23	
c1	0.004	0.006	0.10	0.15	
D	0.430	0.450	10.92	11.43	3
E	0.320	0.340	8.13	8.64	
E1	---	0.360	---	9.14	3
E2	0.220	0.240	5.59	6.10	
E3	0.030	---	0.76	---	7
e	0.050 BSC		1.27 BSC		
k	0.008	0.015	0.20	0.38	2
L	0.280	0.320	7.11	8.13	
Q	0.026	0.045	0.66	1.14	8
S1	0.000	---	0.00	---	
M	---	0.0015	---	0.04	
N	18		18		

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finish lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038 mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M – 1982.
10. Controlling dimension: INCH.

FIGURE 1. Case outline – Continued.

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Device type	01	
Case outlines	P	X
Terminal number	Terminal symbol	
1	COMP <u>1/</u>	NC <u>2/</u>
2	VFB	COMP <u>1/</u>
3	ISENSE	VFB
4	RTCT <u>3/</u>	NC <u>2/</u>
5	GND	NC <u>2/</u>
6	OUTPUT	NC <u>2/</u>
7	VCC	ISENSE
8	VREF	RTCT <u>3/</u>
9	---	NC <u>2/</u>
10	---	NC <u>2/</u>
11	---	OSCGND
12	---	GND
13	---	NC <u>2/</u>
14	---	OUTPUT
15	---	V _C
16	---	VCC
17	---	VREF
18	---	NC <u>2/</u>

NOTES

- 1/ Grounding the COMP pin does not disable the output. The output may be disabled by raising the voltage on the ISENSE pin to > 1.1 V.
- 2/ NC = No connection
- 3/ Part should be operated with C_T = 3.3 nF and R_T = 10 kΩ timing components.

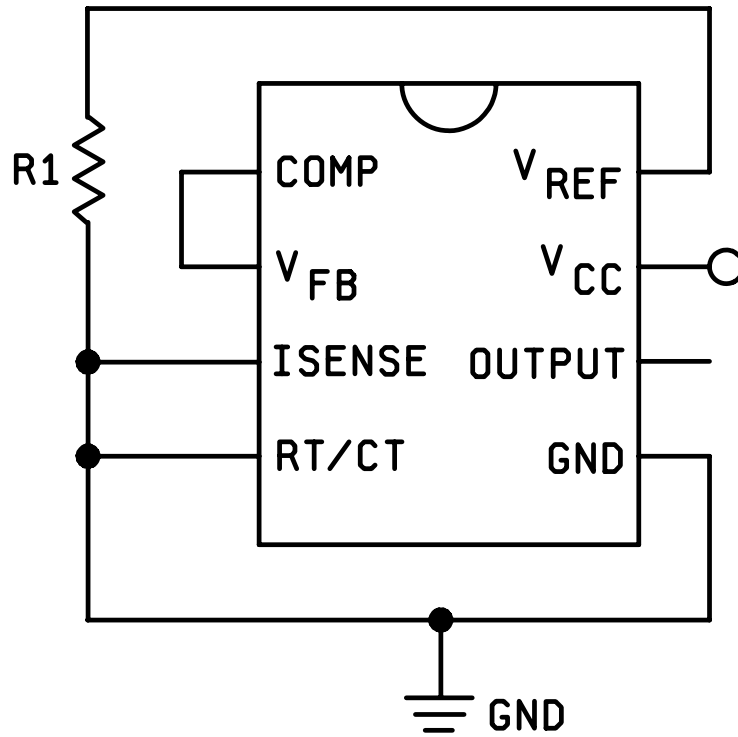
FIGURE 2. Terminal connections.

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Terminal symbol	Description
COMP	This is the output of the error amplifier and is the difference between the sampled voltage on V_{FB} and an internal 2.5 V reference voltage. This point is internally connected to the inverting input of the current sense comparator.
V_{FB}	This is the inverting input of the error amplifier. A scaled sample of the converter output voltage should be connected to this pin. The difference of this voltage and an internal 2.5 V reference is fed to the current sense comparator.
ISENSE	This is the non-inverting input of the current sense comparator. A small series resistor used to sense the current through the switching FET should be connected to this input. The switch is turned off when this current reaches a peak controlled by the error amplifier.
RTCT	This is the connection for the resistor and capacitor timing components that set the frequency of the oscillator. A 10 k Ω resistor to V_{REF} and a 3.3 nF capacitor to ground are the values used to verify 55 kHz operation.
GND	This is the return for all of the internal circuitry. On the die, there is a double bond pad for the oscillator ground, a pad for the logic ground, and a pad for the output stage ground. These pads must all be bonded to ground in hybrid applications and are all bonded to the GND pin on the dual-in-line package. On the flat pack option, the oscillator ground is double bonded to OSCGND pin, while the logic and output stage grounds are bonded to the GND pin.
OUTPUT	This is the main pulse width modulator output for the FET control.
V_{CC}	This is the supply voltage input pin. The device is specified for an operating supply range of 12 V to 25 V. An under voltage lockout circuit disables the outputs (tri-state) and prevents damage to the switching FET, if power-up voltage has not reached 8.2 V, or if the supply voltage drops below 9.0 V after start-up.
V_{REF}	This is the reference voltage output. It is designed to provide an extremely stable 5 V reference voltage over temperature and post irradiation. The oscillator timing resistor (RT) is connected to this pin.
OSCGND	Ground of the internal oscillator. This pin should be connected to system ground.
V_C	Open collector of the output stage. This pin should be connected to the V_{CC} supply voltage.

FIGURE 2. Terminal connections – Continued.

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NOTES:

$V_{CC} = 15\text{ V} \pm 0.5\text{ V}$ and $R1 = 10\text{ k}\Omega, \frac{1}{4}\text{ W} \pm 1\%$

FIGURE 3. Radiation exposure circuit.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,4	1,4	1,4
Final electrical parameters (see 4.2)	1,2,3,4,5,6 <u>1/</u>	1,2,3,4,5,6 <u>1/</u>	1,2,3, <u>2/ 3/</u> 4,5,6
Group A test requirements (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6	1,2,3,4,5,6
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6	1,2,3, <u>3/</u> 4,5,6
Group D end-point electrical parameters (see 4.4)	1,4	1,4	1,4
Group E end-point electrical parameters (see 4.4)	1,4	1,4	1,4

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroup 1 and deltas.

3/ Delta limits as specified in table IIB herein shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters (see table I).

TABLE IIB. Delta parameters (+25°C).

Parameters	Symbol	Delta limits
Input bias current	I _B	±0.1 µA
Operating supply current	I _{CC}	±2.0 mA

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. T_A = +125°C, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

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4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated aging testing. Accelerated aging testing shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limits at $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate burnout. When required by the customer, test shall be performed on devices, SEC, or approved test structures at technology qualifications and after any design or process changes which may effect the RHA capability of the process. Dose rate burnout shall be performed in accordance with test method 1023 of MIL-STD-883 and as specified herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

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6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

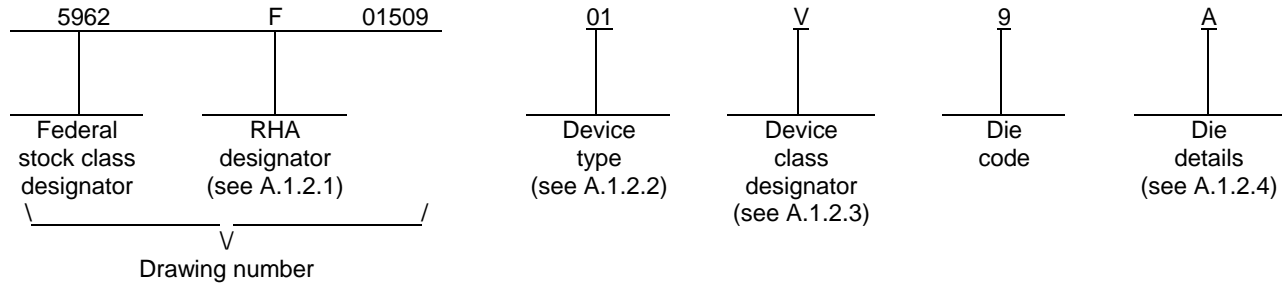
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A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	IS-1845ASRH	Radiation hardened current mode pulse width modulator

A.1.2.3 Device class designator.

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

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A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

<u>Die type</u>	<u>Figure number</u>
01	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

<u>Die type</u>	<u>Figure number</u>
01	A-1

A.1.2.4.3 Interface materials.

<u>Die type</u>	<u>Figure number</u>
01	A-1

A.1.2.4.4 Assembly related information.

<u>Die type</u>	<u>Figure number</u>
01	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

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A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.3 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

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A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

- a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.
- b. 100% wafer probe (see paragraph A.3.4 herein).
- c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.1.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

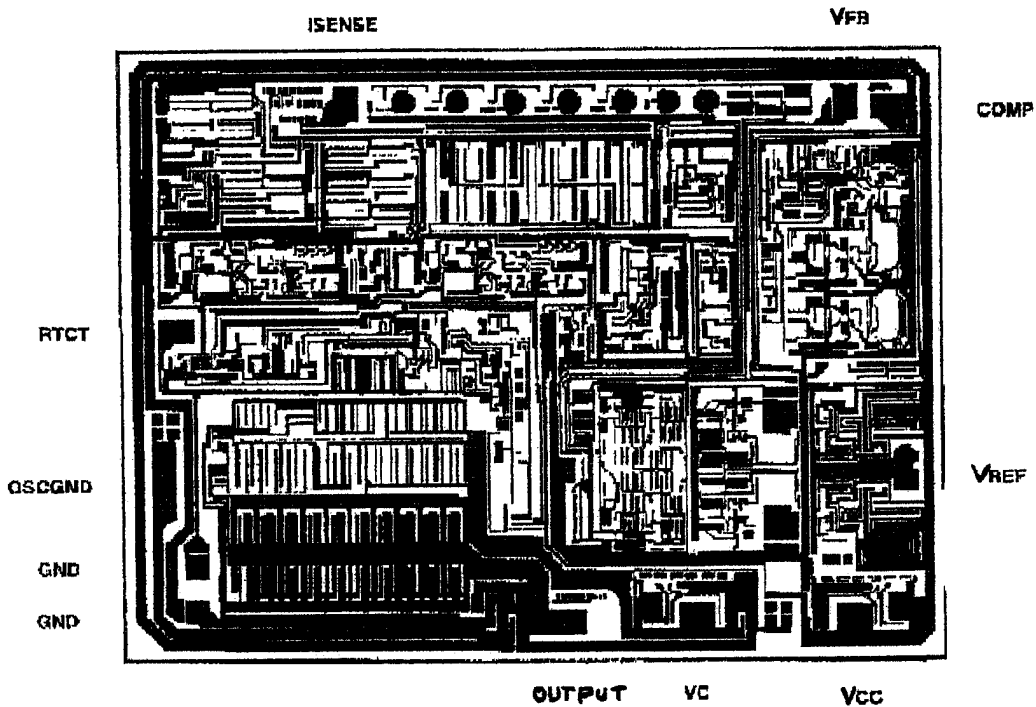
A.6.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0547.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DSCC-VA and have agreed to this drawing.

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Die physical dimensions.

Die size: 121.6 mils x 159.0 mils.

Die thickness: 19 ±1 mils

Interface materials.

Top metallization: Al Si Cu 16.0 kÅ ±2.0 kÅ

Backside metallization: None (Silicon)

Glassivation.

Type: Phosphorus silicon glass (PSG)

Thickness: 8 kÅ ± 1 kÅ

Substrate: DI (dielectric isolation)

Assembly related information.

Substrate potential: Unbiased.

Special assembly instructions:

1. Both the GND pads must be bonded to ground.
2. The OUTPUT double-sized bond pad must be double bonded for current sharing purposes.
3. The OSCGND double-sized bond pad must be double bonded to ground for current sharing purposes

FIGURE A-1. Die bonding pad locations and electrical functions.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 08-10-16

Approved sources of supply for SMD 5962-01509 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962F0150901QPC	34371	IS7-1845ASRH-8
5962F0150901QXC	34371	IS9-1845ASRH-8
5962F0150901VPC	34371	IS7-1845ASRH-Q
5962F0150901VXC	34371	IS9-1845ASRH-Q
5962F0150901V9A	34371	IS0-1845ASRH-Q

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

34371

Vendor name and address

Intersil Corporation
 1001 Murphy Ranch Road
 Milpitas, CA 95035-6803
 Point of contact: 1650 Robert J. Conlan Blvd.
 Palm Bay, FL 32905

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