

**REVISIONS**

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes to table I. Clarification made in figure 1. Technical changes to table IIA. Replaced pin description in section 6.7. Editorial changes throughout.	93-02-24	Monica L. Poelking
B	Update boilerplate to MIL-PRF-38535 requirements. - CFS	03-08-05	Charles F. Saffle
C	Update boilerplate to current MIL-PRF-38535 requirements. - CFS	08-07-17	Thomas M. Hess

REV																				
SHEET																				
REV	C	C	C	C																
SHEET	15	16	17	18																

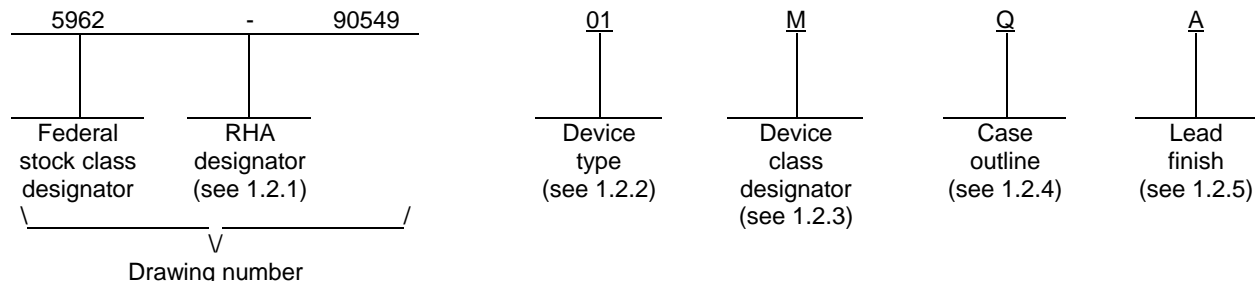
REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Jeffery Tunstall	<p align="center"><b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</b>  <a href="http://www.dsccl.dla.mil">http://www.dsccl.dla.mil</a></p>																	
<p align="center"><b>STANDARD MICROCIRCUIT DRAWING</b></p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Thomas M. Hess																		
	APPROVED BY Monica L. Poelking	<p align="center"><b>MICROCIRCUIT, DIGITAL, MANCHESTER ENCODER/DECODER, MONOLITHIC SILICON</b></p>																	
	DRAWING APPROVAL DATE 92-09-04																		
	REVISION LEVEL C	<table border="1"> <tr> <td>SIZE A</td> <td>CAGE CODE <b>67268</b></td> <td><b>5962-90549</b></td> </tr> </table>	SIZE A	CAGE CODE <b>67268</b>	<b>5962-90549</b>														
SIZE A	CAGE CODE <b>67268</b>	<b>5962-90549</b>																	
		SHEET 1 OF 18																	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example.



1.3 Absolute maximum ratings. 1/

Supply voltage.....	+7.0 V dc
Input, output or I/O voltage applied .....	GND – 0.5 V dc to V <sub>CC</sub> + 0.5 V dc
Junction temperature (T <sub>J</sub> ).....	+175°C
Storage temperature range .....	-65°C to +150°C
Lead temperature (soldering, 10 seconds).....	+300°C
Power dissipation (P <sub>D</sub> ).....	1.44 W
Thermal resistance, junction-to-case (θ <sub>JC</sub> ) .....	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ <sub>JA</sub> ) .....	34.8°C/W

1.4 Recommended operating conditions.

Supply voltage range (V <sub>CC</sub> ) .....	+4.5 V dc to +5.5 V dc
Encoder/decoder clock rise time (t <sub>ECR</sub> , t <sub>DCR</sub> ).....	8.0 ns max
Encoder/decoder clock fall time (t <sub>ECF</sub> , t <sub>DCF</sub> ) .....	8.0 ns max
Sync transition span (t <sub>D2</sub> ) .....	18 t <sub>DC</sub> 2/
Short data transition span (t <sub>D4</sub> ).....	6.0 t <sub>DC</sub> 2/
Long data transition span (t <sub>D5</sub> ).....	12 t <sub>DC</sub> 2/
Case operating temperature range (T <sub>C</sub> ) .....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ t<sub>DC</sub> = decoder clock period = 1/f<sub>DC</sub>.

<b>STANDARD                  MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-90549</b>
		REVISION LEVEL <b>C</b>	SHEET <b>3</b>

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T <sub>C</sub> ≤ +125°C +4.5 V ≤ V <sub>CC</sub> ≤ +5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	V <sub>IL</sub>	V <sub>CC</sub> = 4.5 V and 5.5 V	1, 2, 3	All		0.2(V <sub>CC</sub> )	V
Input high voltage	V <sub>IH</sub>	V <sub>CC</sub> = 4.5 V and 5.5 V	1, 2, 3	All	0.7(V <sub>CC</sub> )		V
Input low clock voltage	V <sub>ILC</sub>	V <sub>CC</sub> = 4.5 V and 5.5 V	1, 2, 3	All		GND +0.5	V
Input high clock voltage	V <sub>IHC</sub>	V <sub>CC</sub> = 4.5 V and 5.5 V	1, 2, 3	All	V <sub>CC</sub> -0.5		V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1.8 mA, V <sub>CC</sub> = 4.5 V <u>2/</u>	1, 2, 3	All		0.4	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -3.0 mA, V <sub>CC</sub> = 4.5 V <u>2/</u>	1, 2, 3	All	2.4		V
Input leakage current	I <sub>I</sub>	V <sub>I</sub> = GND, V <sub>CC</sub> = 5.5 V	1, 2, 3	All	-1.0	0	μA
		V <sub>I</sub> = V <sub>CC</sub> , V <sub>CC</sub> = 5.5 V			0	+1.0	
Operating power supply current	I <sub>CCOP</sub>	V <sub>CC</sub> = 5.5 V, f = 1.0 MHz <u>3/</u>	1, 2, 3	All		10	mA
Standby supply current	I <sub>CCSB</sub>	V <sub>IN</sub> = V <sub>CC</sub> = 5.5 V, Output open	1, 2, 3	All		2.0	mA
Input capacitance	C <sub>I</sub>	All measurements referenced to device ground.	4	All		25	pF
Input/output capacitance	C <sub>I/O</sub>	V <sub>CC</sub> = open, f = 1.0 MHz, See 4.4.1b	4	All		25	pF
Functional test <u>4/</u>		f = 15 MHz, C <sub>L</sub> = 50 pF, V <sub>CC</sub> = 4.5 V and 5.5 V V <sub>IH</sub> = 0.7V <sub>CC</sub> , V <sub>IL</sub> = 0.2V <sub>CC</sub> V <sub>IHC</sub> = V <sub>CC</sub> - 0.5 V, V <sub>ILC</sub> = GND +0.5 V, See 4.4.1c	7, 8	All			

Encoder Timing

Encoder clock frequency	f <sub>EC</sub>	V <sub>CC</sub> = 4.5 V and 5.5 V, V <sub>IH</sub> = 0.7V <sub>CC</sub> , V <sub>IL</sub> = 0.2V <sub>CC</sub> , CL = 50 pF, See figure 3.	9, 10, 11	01		15	MHz
				02		30	
Send clock frequency	f <sub>ESC</sub>	See figure 3.	9, 10, 11	01		2.5	MHz
				02		5.0	
Encoder data rate	f <sub>ED</sub>		9, 10, 11	01		1.25	MHz
				02		2.50	
Master reset pulse width	t <sub>MR</sub>		9, 10, 11	All	150		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ T <sub>C</sub> ≤ +125°C +4.5 V ≤ V <sub>CC</sub> ≤ +5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Encoder Timing - Continued.							
Shift clock delay	t <sub>E1</sub>	V <sub>CC</sub> = 4.5 V and 5.5 V, V <sub>IH</sub> = 0.7V <sub>CC</sub> , V <sub>IL</sub> = 0.2V <sub>CC</sub> , CL = 50 pF, See figure 3.	9, 10, 11	01		125	ns
				02		80	
Serial data setup	t <sub>E2</sub>		9, 10, 11	01	75		ns
				02	50		
Serial data hold	t <sub>E3</sub>		9, 10, 11	01	75		ns
				02	50		
Enable setup	t <sub>E4</sub>		9, 10, 11	All	90		ns
Enable pulse width	t <sub>E5</sub>		9, 10, 11	All	100		ns
Sync setup	t <sub>E6</sub>		9, 10, 11	All	55		ns
Sync pulse width	t <sub>E7</sub>		9, 10, 11	All	150		ns
Send data delay	t <sub>E8</sub>		9, 10, 11	All	0	50	ns
Bipolar output delay	t <sub>E9</sub>	9, 10, 11	All		130	ns	
Enable hold	t <sub>E10</sub>	9, 10, 11	All	10		ns	
Sync hold	t <sub>E11</sub>	9, 10, 11	All	95		ns	
Decoder Timing							
Decoder clock frequency	f <sub>DC</sub>	V <sub>CC</sub> = 4.5 V and 5.5 V, V <sub>IH</sub> = 0.7V <sub>CC</sub> , V <sub>IL</sub> = 0.2V <sub>CC</sub> , CL = 50 pF, See figure 3.	9, 10, 11	01		15	MHz
				02		30	
Decoder sync clock	f <sub>DS</sub>		9, 10, 11	01		2.5	MHz
				02		5.0	
Decoder data rate	f <sub>DD</sub>		9, 10, 11	01		1.25	MHz
				02		2.50	
Decoder reset pulse width	t <sub>DR</sub>		9, 10, 11	All	150		ns
Decoder reset setup time	t <sub>DRS</sub>		9, 10, 11	All	75		ns
Decoder reset hold time	t <sub>DRH</sub>		9, 10, 11	All	75		ns
Master reset pulse	t <sub>MR</sub>		9, 10, 11	All	150		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ T <sub>C</sub> ≤ +125°C +4.5 V ≤ V <sub>CC</sub> ≤ +5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Decoder Timing - Continued.							
Bipolar data pulse width	t <sub>D1</sub>	V <sub>CC</sub> = 4.5 V and 5.5 V, V <sub>IH</sub> = 0.7V <sub>CC</sub> , V <sub>IL</sub> = 0.2V <sub>CC</sub> , CL = 50 pF, See figure 3.	9, 10, 11	All	t <sub>DC</sub> + 10 <u>5/</u>		ns
One zero overlap	t <sub>D3</sub>		9, 10, 11	All		t <sub>DC</sub> - 10 <u>5/</u>	ns
Sync delay (ON)	t <sub>D6</sub>		9, 10, 11	All	-20	110	ns
Take data delay (ON)	t <sub>D7</sub>		9, 10, 11	All	0	110	ns
Serial data out delay	t <sub>D8</sub>		9, 10, 11	All		80	ns
Sync delay (OFF)	t <sub>D9</sub>		9, 10, 11	All	0	110	ns
Take data delay (OFF)	t <sub>D10</sub>		9, 10, 11	All	0	110	ns
Valid word delay	t <sub>D11</sub>		9, 10, 11	All	0	110	ns
Sync clock to shift clock delay	t <sub>D12</sub>		9, 10, 11	All		75	ns
Sync data setup	t <sub>D13</sub>		9, 10, 11	All	75		ns

1/ All tests to be performed using worst-case test conditions, unless otherwise specified.

2/ Interchanging of force and sense conditions is permitted.

3/ Guaranteed if not tested to the table I requirements.

4/ Functional tests performed to verify functionality of device as a Manchester encoder/decoder as defined by MIL-STD-1553.

5/ t<sub>DC</sub> = Decoder clock period = 1/f<sub>DC</sub>.

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Device types: 01 and 02			
Case outline: Q			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V <sub>CC</sub>	21	GND
2	VALID WORD	22	MASTER RESET
3	TAKE DATA'	23	COUNT C <sub>2</sub>
4	TAKE DATA	24	DIVIDE BY 6 OUT
5	SERIAL DATA OUT	25	<u>BIPOLAR ZERO OUT</u>
6	SYNCHR DATA	26	<u>OUTPUT INHIBIT</u>
7	SYNCHR DATA SEL	27	<u>BIPOLAR ONE OUT</u>
8	SYNCHR CLK	28	SERIAL DATA IN
9	DECODER CLK	29	ENCODER ENABLE
10	SYNCHR CLK SEL	30	SYNC SEL
11	BIPOLAR ZERO IN	31	ENCODER PARITY SEL
12	BIPOLAR ONE IN	32	SEND DATA
13	UNIPOLAR DATA IN	33	SEND CLK IN
14	DECODER SHIFT CLK	34	ENCODER SHIFT CLK
15	TRANSITION SEL	35	NC
16	NC	36	COUNT C <sub>3</sub>
17	COMMAND SYNC	37	ENCODER CLK
18	DECODER PARITY SEL	38	DATA SYNC
19	DECODER RESET	39	COUNT C <sub>4</sub>
20	COUNT C <sub>0</sub>	40	COUNT C <sub>1</sub>

NC = No connection

FIGURE 1. Terminal connections.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-90549</b>
		REVISION LEVEL <b>C</b>	SHEET <b>8</b>

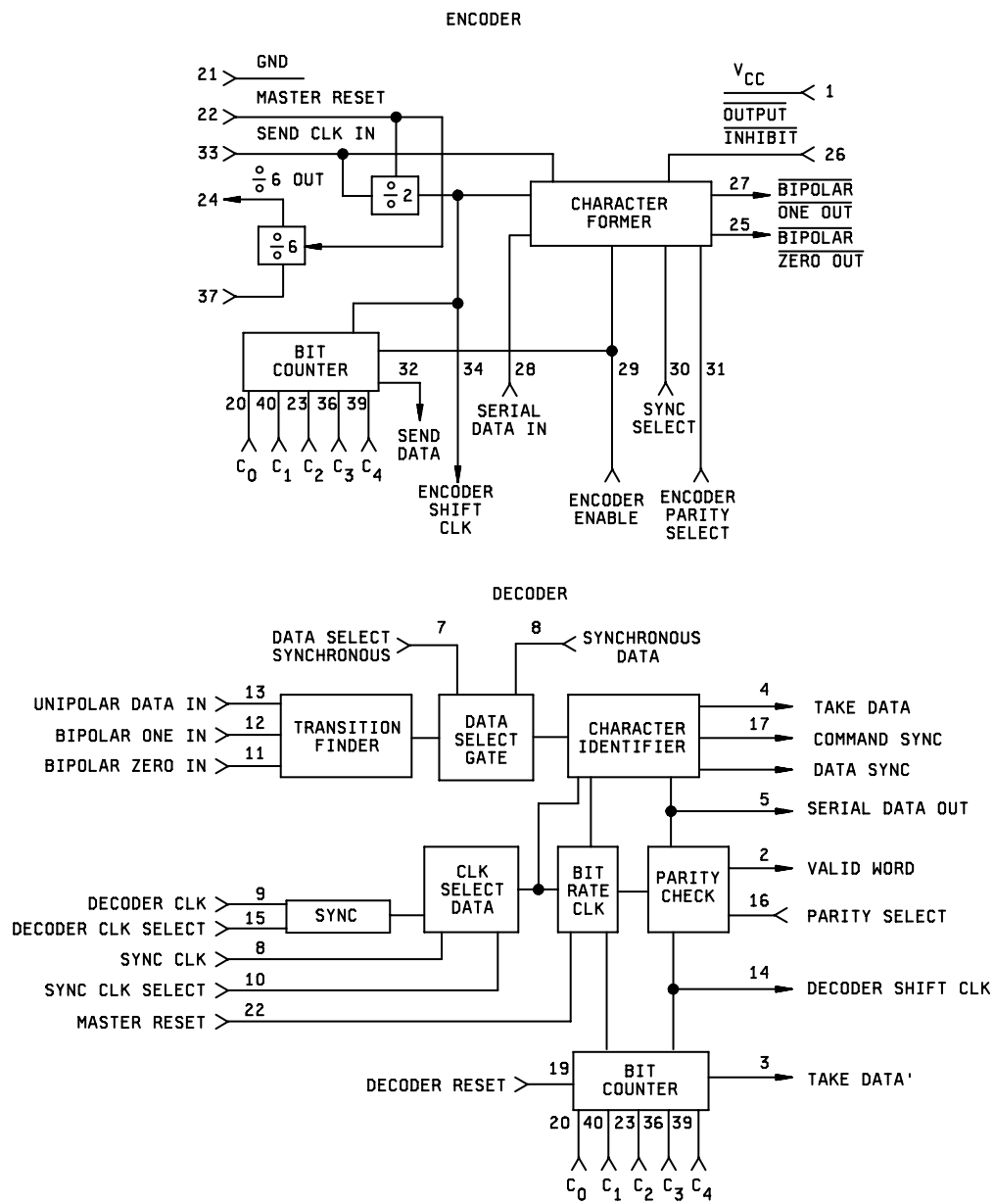


FIGURE 2. Block diagram.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-90549</b>
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ENCODER TIMING

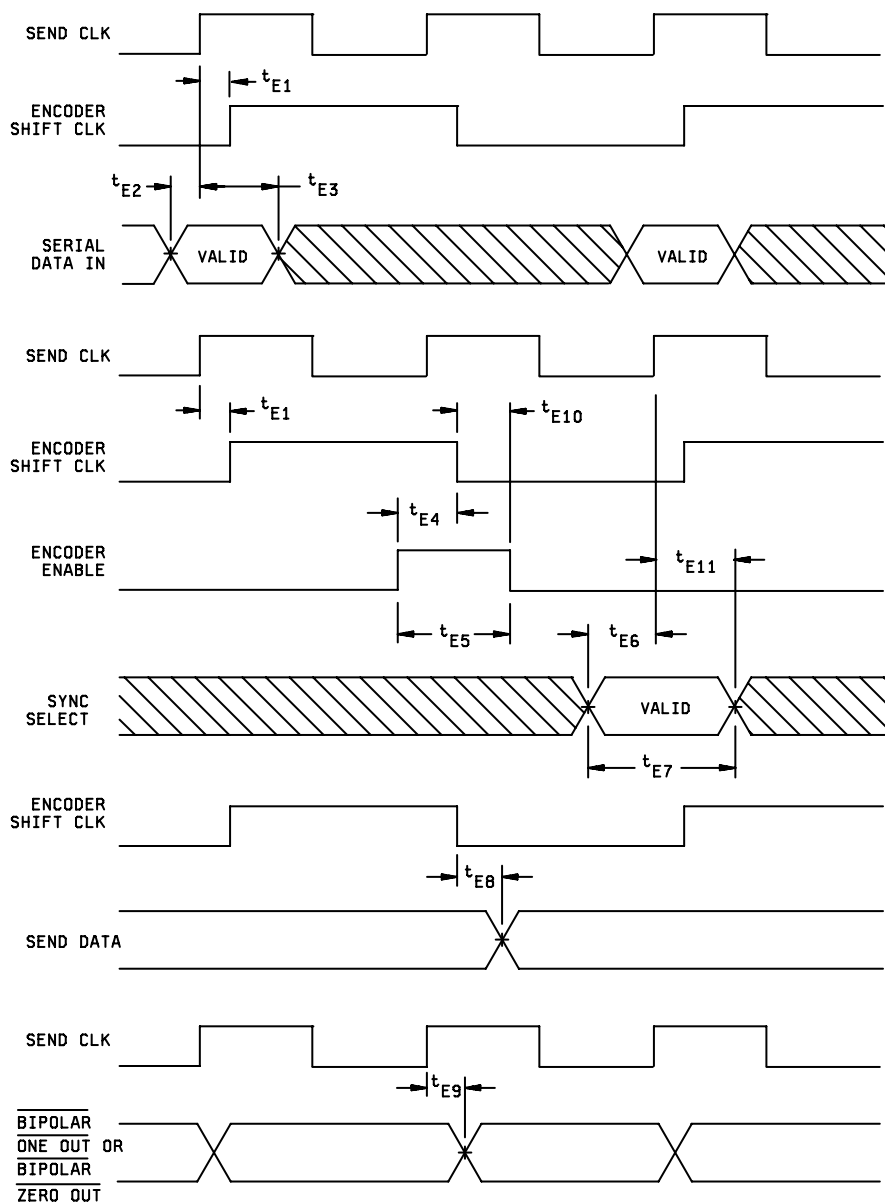
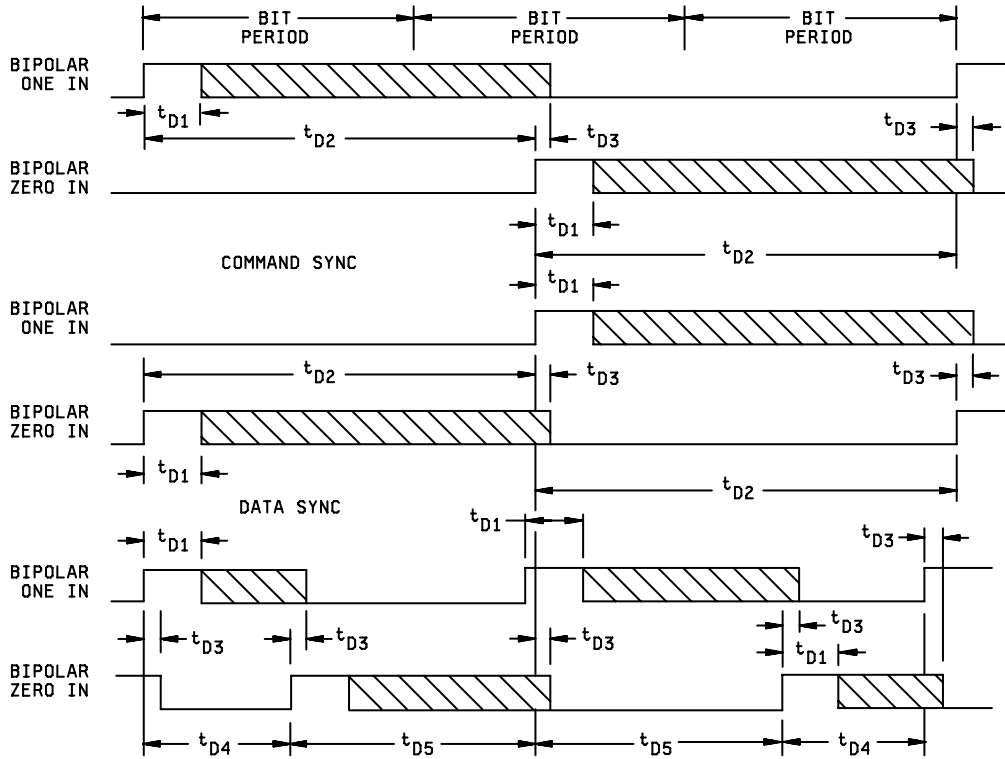


FIGURE 3. Timing waveforms and test circuit.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-90549</b>
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DECODER TIMING

NOTE: UNIPOLAR IN = 0, FOR NEXT DIAGRAM



NOTE: BIPOLAR ONE IN = 0, BIPOLAR ZERO IN = 1, FOR NEXT DIAGRAM

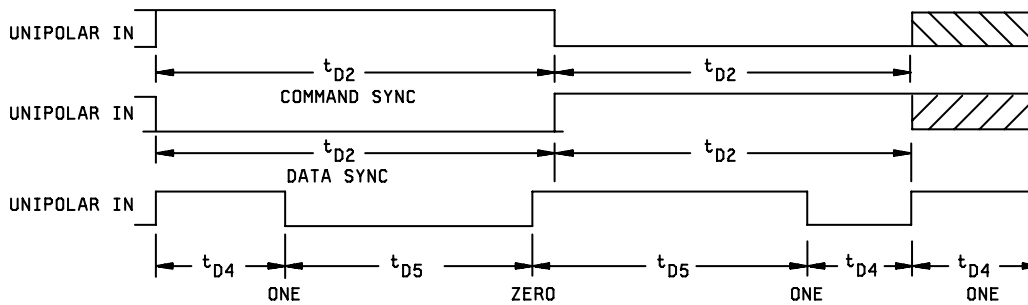


FIGURE 3. Timing waveforms and test circuit - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-90549</b>
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DECODER TIMING CONTINUED

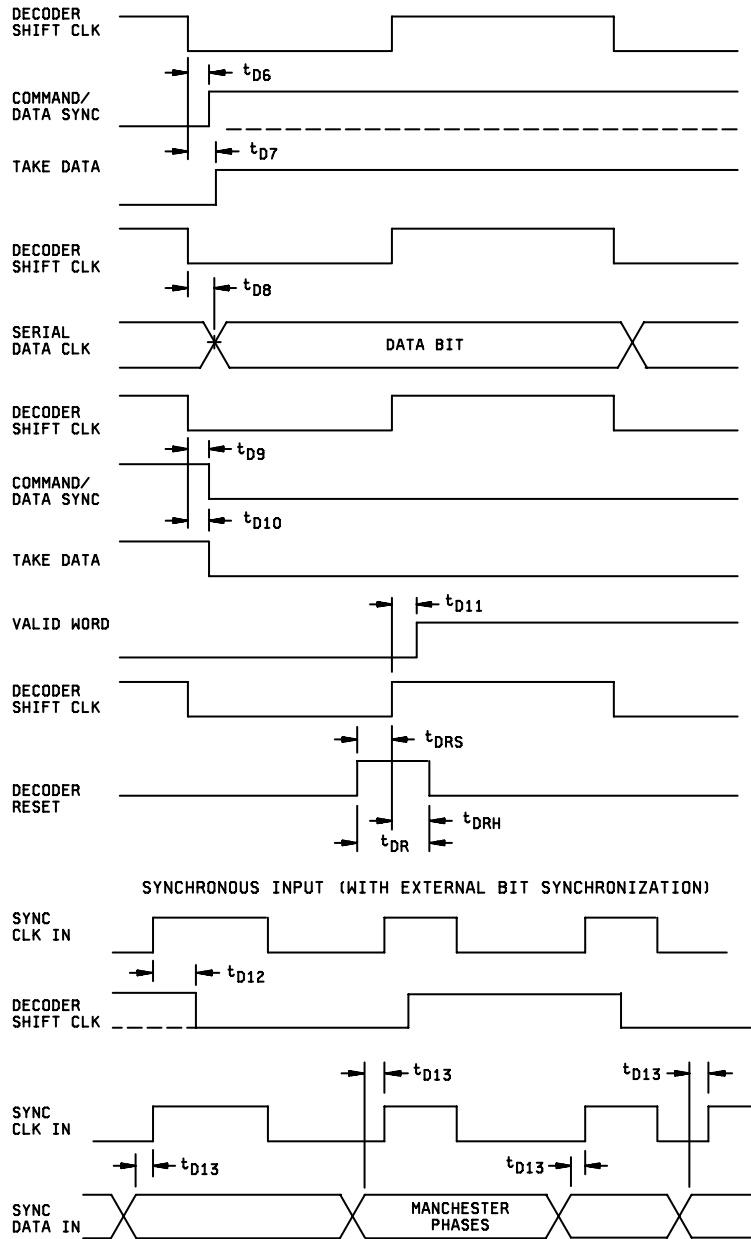
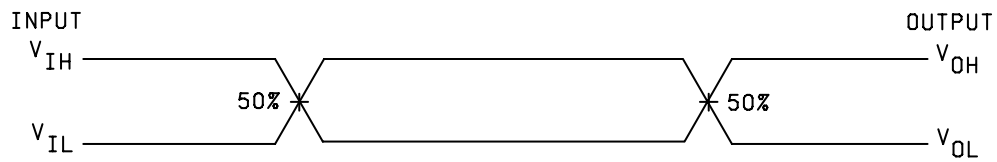
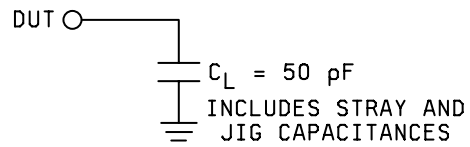


FIGURE 3. Timing waveforms and test circuit - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-90549</b>
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Note: AC testing: All input signals must switch between  $V_{IL}$  and  $V_{IH}$ .  
Input rise and fall times are driven at 1 ns per volt.

FIGURE 3. Timing waveforms and test circuit - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-90549</b>
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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device. These tests form a part of the manufacturer's test tape and shall be maintained and available from the approved source of supply.
- c. Subgroup 4 ( $C_I$  and  $C_{I/O}$  measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero failures shall be required.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 <u>1/</u>	1, 2, 3, 7, 8, 10, 11 <u>1/</u>	1, 2, 3, 7, 8, 10, 11 <u>2/</u>
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11 <u>1/</u>	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b.  $T_A = +125^\circ\text{C}$ , minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

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4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ , after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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6.7 Pin descriptions.

Pin number	Type <u>1/</u>	Name	Section	Description
1		V <sub>CC</sub>	Both	Positive supply pin. A 0.1 μF decoupling capacitor from V <sub>CC</sub> (Pin 1) to GROUND (Pin 21) is recommended.
2	O	VALID WORD	Decoder	Output high indicates receipt of a valid word (valid parity and no Manchester errors).
3	O	TAKE DATA'	Decoder	A continuous, free running signal provided for host timing or data handling. When data is present on the bus, this signal will be synchronized to the incoming data and will be identical to TAKE DATA.
4	O	TAKE DATA	Decoder	Output is high during receipt of data after identification of a valid sync pulse and two valid Manchester bits.
5	O	SERIAL DATA OUT	Decoder	Delivers received data in correct NRZ format.
6	I	SYNCHRONOUS DATA	Decoder	Input presents Manchester data directly to character identification logic. SYNCHRONOUS DATA SELECT must be held high to use this input. If not used, this pin must be held high.
7	I	SYNCHRONOUS DATA SELECT	Decoder	In high state allows the synchronous data to enter the character identification logic. Tie this input low for asynchronous data.
8	I	SYNCHRONOUS CLOCK	Decoder	Input provides externally synchronized clock to the decoder, for use when receiving synchronous data. This input must be tied high when not in use.
9	I	DECODER CLOCK	Decoder	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder. Input a frequency equal to 12X the data rate.
10	I	SYNCHRONOUS CLOCK SELECT	Decoder	In high state directs the SYNCHRONOUS CLOCK to control the decoder character identification logic. A low state selects the DECODER CLOCK.
11	I	BIPOLAR ZERO IN	Decoder	A high input should be applied when the bus is in its negative state. This pin must be held high when the unipolar input is used.
12	I	BIPOLAR ONE IN	Decoder	A high input should be applied when the bus is in its positive state. This pin must be held low when the unipolar input is used.
13	I	UNIPOLAR DATA IN	Decoder	With Pin 11 high and Pin 12 low, this pin enters unipolar data into the transition finder circuit. If not used, this input must be held low.
14	O	DECODER SHIFT CLOCK	Decoder	Output which delivers a frequency (DECOCER CLOCK divided by 12), synchronous by the recovered serial data stream.
15	I	TRANSITION SELECT	Decoder	A high input to this pin causes the transition finder to synchronize on every transition of in-out data. A low input causes the transition finder to synchronize only on mid-bit transitions.
16		NC		Not connected.
17	O	COMMAND SYNC	Decoder	Output of a high from this pin occurs during output of decoder data which was preceded by a Command (or Status) synchronizing character.

See footnotes at end of table.

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Pin number	Type <sup>1/</sup>	Name	Section	Description
18	I	DECODER PARITY SELECT	Decoder	An input for parity sense, calling for even parity with input high and odd parity with input low.
19	I	DECODER RESET	Decoder	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
20	I	COUNT C <sub>0</sub>	Both	One of five binary inputs which establish the total bit count to be encoded or decoded.
21		GROUND	Both	Supply pin.
22	I	MASTER RESET	Both	A high on this pin clears 2:1 counters in both encoder and decoder, and resets the divide by 6 circuit.
23	I	COUNT C <sub>2</sub>	Both	See pin 20
24	O	DIVIDE BY 6 OUT	Encoder	Output from 6:1 divider which is driven by the ENCODER CLOCK.
25	O	<u>BIPOLAR ZERO OUT</u>	Encoder	An active low output designed to drive the zero or negative sense of a bipolar line driver.
26	I	<u>OUTPUT INHIBIT</u>	Encoder	A low on this pin forces pin 25 and pin 27 high, the inactive states.
27	O	<u>BIPOLAR ONE OUT</u>	Encoder	An active low output designed to drive the one or positive sense of a bipolar line driver.
28	I	SERIAL DATA IN	Encoder	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
29	I	ENCODER ENABLE	Encoder	A high on this pin initiates the encode cycle. (Subject to the preceding cycle being complete.)
30	I	SYNC SELECT	Encoder	Actuates a Command Sync for an input high and Data Sync for an input low.
31	I	ENCODER PARITY SELECT	Encoder	Sets transmit parity odd for a high input, sets transmit parity even for a low input.
32	O	SEND DATA	Encoder	Is an active high output which enables the external source of serial data.
33	I	SEND CLOCK IN	Encoder	Clock input at a frequency equal to the data rate X2.
34	O	ENCODER SHIFT CLOCK	Encoder	Output for shifting data into the Encoder. The Encoder samples SDI (pin 28) on the low-to-high transition of ESC.
35		NC		Not connected.
36	I	COUNT C <sub>3</sub>	Both	See pin 20.
37	I	ENCODER CLOCK	Encoder	Input to the 6:1 divider, a frequency equal to 12 times the data rate is usually input here.
38	O	DATA SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a data synchronizing character.
39	I	COUNT C <sub>4</sub>	Both	See pin 20.
40	I	COUNT C <sub>1</sub>	Both	See pin 20.

<sup>1/</sup> I = Input, O = Output.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 08-07-17

Approved sources of supply for SMD 5962-90549 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9054901MQA	34371	HD1-15531
5962-9054902MQA	<u>3/</u>	HD1-15531B/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE  
number

34371

Vendor name  
and address

Intersil Corporation  
1001 Murphy Ranch Road  
Milpitas, CA 95035-6803  
Point of contact: 1650 Robert J. Conlan Blvd.  
Palm Bay, FL 32905

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