

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added Intersil as source of supply CAGE 34371. Updated boilerplate and editorial changes throughout. – LTG	00-09-12	Monica L. Poelking
B	Update boilerplate to MIL-PRF-38535 requirements. – LTG	01-04-20	Thomas M. Hess

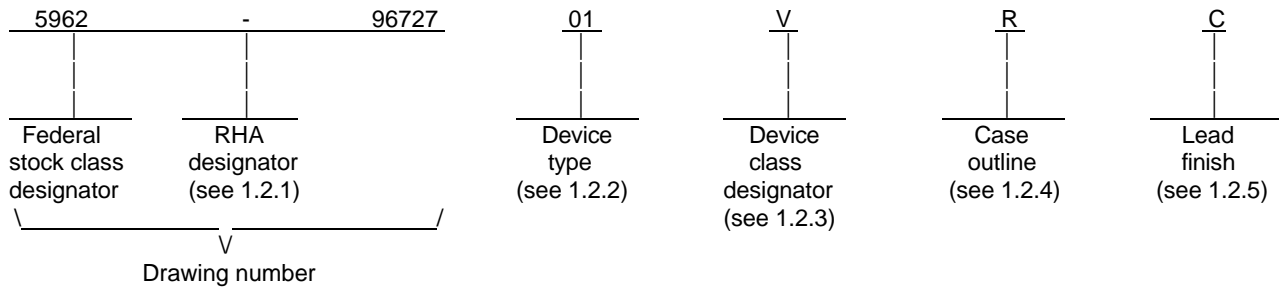
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OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14					

PMIC N/A	PREPARED BY Thomas M. Hess	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 http://www.dsccl.dla.mil													
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thomas M. Hess														
	APPROVED BY Monica L. Poelking	MICROCIRCUIT, DIGITAL, CMOS, BUS CONTROLLER, MONOLITHIC SILICON													
	DRAWING APPROVAL DATE 96-02-23														
	REVISION LEVEL B		SIZE A	CAGE CODE 67268	5962-96727										
		SHEET 1 OF 14													

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	82C88/7	Latchup resistant, CMOS, bus controller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
R	CDIP2-T20	20	Dual-in-line package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96727
		REVISION LEVEL A	SHEET 2

1.3 Absolute maximum ratings. 1/

Supply voltage (V _{CC}).....	+8.0 V dc
Input or I/O voltage range.....	GND -0.5 V dc to V _{CC} +0.5 V dc
Storage temperature range (T _{STG})	-65°C to +150°C
Junction temperature (T _J).....	+175°C
Lead temperature (soldering 10 seconds)	+265°C
Thermal resistance, Junction-to-case (θ _{JC}).....	12°C/W
Thermal resistance, Junction to ambient (θ _{JA}).....	68°C/W
Maximum package power dissipation T _A = +125°C (P _D) 2/	0.74 W

1.4 Recommended operating conditions.

Operating supply voltage range (V _{CC})	4.5 V dc to +5.5 V dc
Operating temperature range (T _A).....	-55°C to +125°C
Input low voltage range (V _{IL}).....	0.0 V dc to +0.7 V dc
Input high voltage range, except clock pin (V _{IH}).....	2.2 V dc to V _{DD}
Input high voltage range, clock pin (V _{IHC})	V _{DD} -0.8 V to V _{DD}

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012).....	90 percent
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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
 2/ If device power exceeds package dissipation capability provide heat sinking or derate linearly (the derating is based on θ_{JA}) at the rate of 14.7mW/°C

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96727
		REVISION LEVEL B	SHEET 3

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96727
		REVISION LEVEL B	SHEET 4

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logical "1" input voltage	V _{IH}	V _{CC} = 5.5 V 2/ Pins 1, 3, 6, 15, 18, 19	1, 2, 3	All	2.2		V
Logical "0" input voltage	V _{IL}	V _{CC} = 4.5 V 2/ Pins 1, 3, 6, 15, 18, 19	1, 2, 3	All		0.7	V
Logical "1" input voltage clock	V _{IHC}	V _{CC} = 5.5 V, Pin 2 2/	1, 2, 3	All	4.7		V
Logical "0" input voltage clock	V _{ILC}	V _{CC} = 4.5 V, Pin 2 2/	1, 2, 3	All		0.8	V
Output high voltage	V _{OH1A}	V _{CC} = 4.5 V I _{OH} = -8.0 mA Pins 4, 7, 8, 9, 11-14	1, 2, 3	All	3.0		V
	V _{OH1B}	V _{CC} = 4.5 V I _{OH} = -2.5 mA Pins 4, 7, 8, 9, 11-14			V _{CC} -0.4		
Output high voltage	V _{OH2A}	V _{CC} = 4.5 V I _{OH} = -4.0 mA Pins 4, 5, 16, 17	1, 2, 3	All	3.0		V
	V _{OH2B}	V _{CC} = 4.5 V I _{OH} = -2.5 mA Pins 4, 5, 16, 17			V _{CC} -0.4		
Output low voltage	V _{OL1}	V _{CC} = 4.5 V I _{OL} = +12.0 mA Pins 4, 7, 8, 9, 11-14	1, 2, 3	All		0.5	V
Output low voltage	V _{OL2}	V _{CC} = 4.5 V I _{OL} = +8.0 mA Pins 4, 5, 16, 17	1, 2, 3	All		0.4	V
Input leakage current	I _{IH} I _{IL}	V _{CC} = 5.5 V, V _{IN} = GND or V _{CC} , Pins 1, 2, 6, 15	1, 2, 3	All	-1.0	1.0	μA
Output leakage current	I _{OZL} I _{OZH}	V _{CC} = 5.5 V V _{OUT} = GND or V _{CC} Pins 7, 8, 9, 11-14	1, 2, 3	All	-10.0	10.0	μA
Standby power supply current	I _{CCSB}	V _{CC} = 5.5 V, V _{IN} = GND or V _{DD} , Outputs open	1, 2, 3	All		10.0	μA
Operating power supply current	I _{CCOP}	V _{CC} = 5.5 V, V _{IN} = GND or V _{DD} , Outputs open, f = 10 MHz	1, 2, 3	All		10.0	mA
Input leakage current status bus	I _{BHH}	V _{CC} = 5.5 V 3/ Outputs open, Pins 3, 18, 19	1, 2, 3	All	-300	-50.0	μA
Input capacitance	C _{IN}	V _{CC} = Open, f = 1 MHz All measurements referenced to GND See 4.4.1c	4	All		13.0	pF
Output capacitance	C _{OUT}		4	All		20.0	pF
Functional tests		V _{CC} = 4.5 V and 5.5 V See 4.4.1b	7, 8	All			

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96727
		REVISION LEVEL A	SHEET 5

TABLE I. Electrical performance characteristics Continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TIMING REQUIREMENTS							
CLK cycle period	t _{CLCL}	V _{CC} = 4.5 V and 5.5 V See figure 3 ^{2/}	9, 10, 11	All	125.0		ns
CLK low time	t _{CLCH}				55.0		ns
CLK high time	t _{CHCL}				45.0		ns
Status active setup time	t _{SVCH}				35.0		ns
Status inactive setup time	t _{CHSV}				10.0		ns
Status active hold time	t _{SHCL}				35.0		ns
Status inactive hold time	t _{CLSH}				10.0		ns
Control active delay	t _{CVNV}	V _{CC} = 4.5 V and 5.5 V See figure 3 Condition 1	9, 10, 11	All	5.0	45.0	ns
Control inactive delay	t _{CVNX}				10.0	45.0	ns
ALE active delay from CLK	t _{CLLH}	V _{CC} = 4.5 V and 5.5 V See figure 3 ^{2/} Condition 1	9, 10, 11	All		20.0	ns
MCE active delay from CLK	t _{CLMCH}					25.0	ns
ALE active delay from status	t _{SVLH}					20.0	ns
MCE active delay from status	t _{SVMCH}					30.0	ns
ALE inactive delay	t _{CHLL}					4.0	22.0
Command active delay	t _{CLML}	V _{CC} = 4.5 V and 5.5 V See figure 3 ^{2/} Condition 2	9, 10, 11	All	5.0	35.0	ns
Command inactive delay	t _{CLMH}				5.0	35.0	ns
Direction control active delay	t _{CHDTL}	V _{CC} = 4.5 V and 5.5 V See figure 3 ^{2/} Condition 1	9, 10, 11	All		50.0	ns
Direction control inactive delay	t _{CHDTH}				9, 10, 11	All	
Command enable time	t _{AELCH}	V _{CC} = 4.5 V and 5.5 V See figure 3 ^{2/} ^{4/} Condition 3	9, 10, 11	All		40.0	ns
Command disable time	t _{AEHCZ}	V _{CC} = 4.5 V and 5.5 V See figure 3 ^{5/} Condition 4	9, 10, 11	All		40.0	ns
Enable delay time	t _{AELCV}	V _{CC} = 4.5 V and 5.5 V See figure 3 ^{2/} Condition 2	9, 10, 11	All	110.0	250.0	ns
<u> </u> AEN to DEN	t _{AEVNV}	V _{CC} = 4.5 V and 5.5 V See figure 3 ^{2/} Condition 1	9, 10, 11	All		25.0	ns
CEN to DEN, PDEN DEN to command	t _{CEVNV}				9, 10, 11	All	
	t _{CELRH}	V _{CC} = 4.5 V and 5.5 V See figure 3 ^{2/} Condition 2	9, 10, 11	All		t _{CLML} +10	ns
ALE high time	t _{LHLL}	V _{CC} = 4.5 V and 5.5 V See figure 3 ^{2/} Condition 1	9, 10, 11	All		t _{CLML} -10	ns

^{1/} All testing to be performed using worst-case test conditions unless otherwise specified.

^{2/} These test are verified functionally as Go/no Go test.

^{3/} I_{BHH} should be measured after raising the V_{IN} on S0, S1, S2 to V_{CC} and then lowering to 2.0 V.

^{4/} t_{AELCH} measurement is between 1.5 V and 2.5 V.

^{5/} t_{AEHCZ} is not tested, but guaranteed to the limits specified.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96727
		REVISION LEVEL A	SHEET 6

Device type	01		
Case outlines	R		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	IOB	11	$\overline{\text{IOWC}}$
2	CLK	12	$\overline{\text{AIOWC}}$
3	$\overline{\text{S}}_1$	13	$\overline{\text{IORC}}$
4	$\overline{\text{DT/R}}$	14	$\overline{\text{INTA}}$
5	ALE	15	CEN
6	$\overline{\text{AEN}}$	16	$\overline{\text{DEN}}$
7	$\overline{\text{MRDC}}$	17	$\overline{\text{MCE/PDEN}}$
8	$\overline{\text{AMWC}}$	18	$\overline{\text{S}}_2$
9	$\overline{\text{MWTC}}$	19	$\overline{\text{S}}_0$
10	GND	20	V _{CC}

FIGURE 1. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96727
		REVISION LEVEL A	SHEET 7

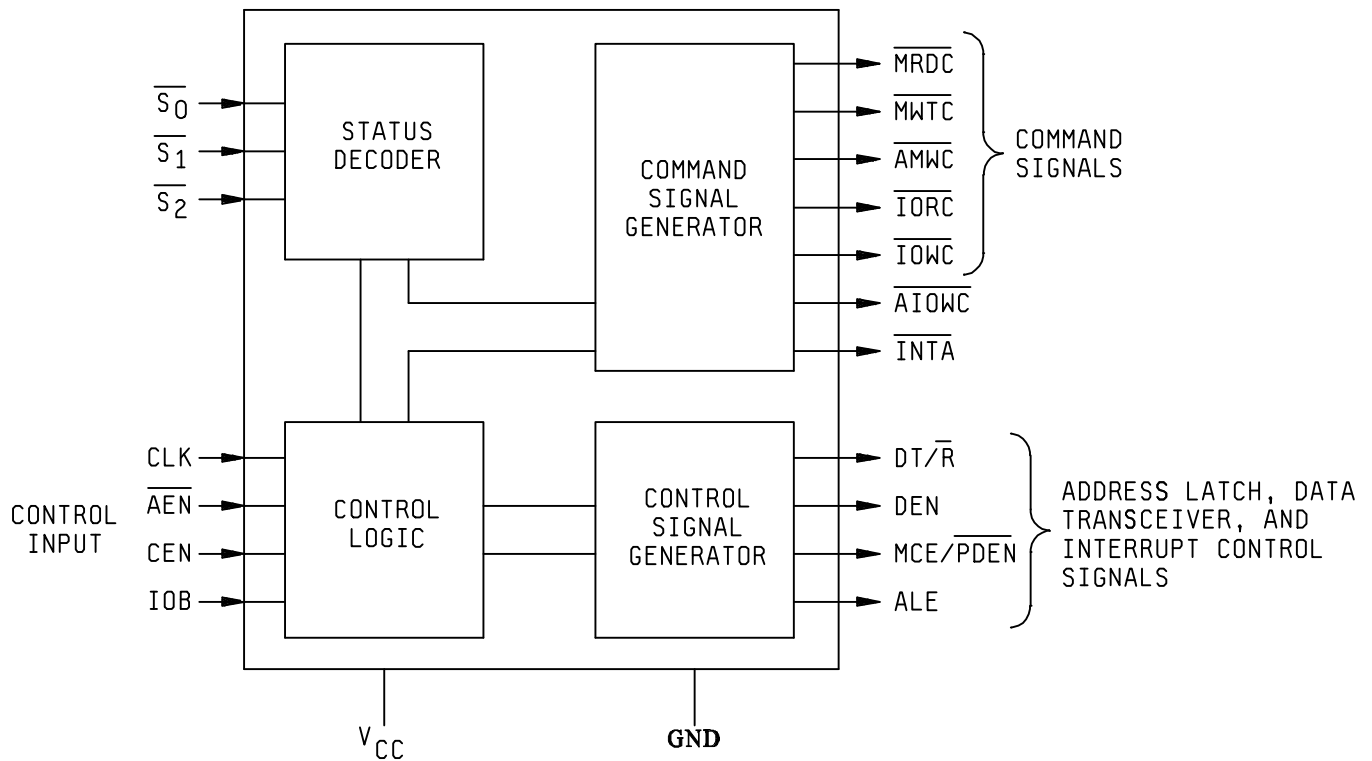
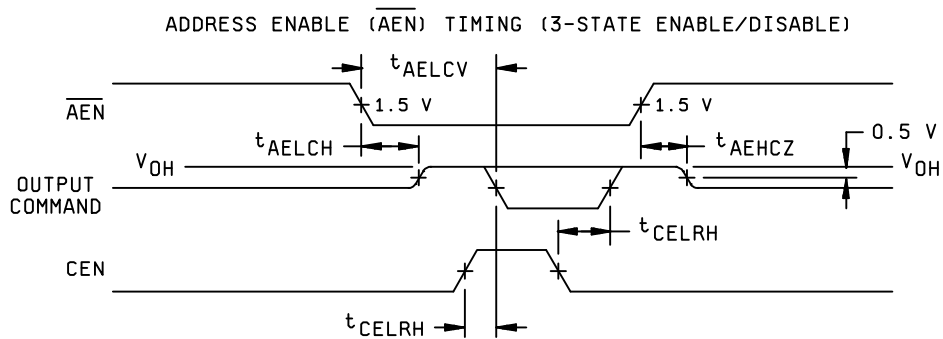
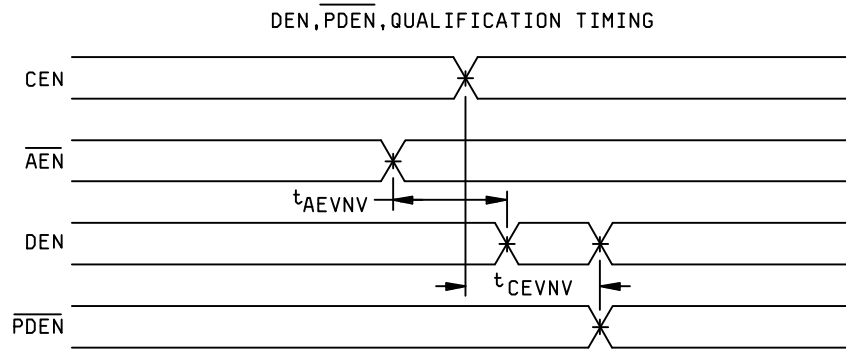
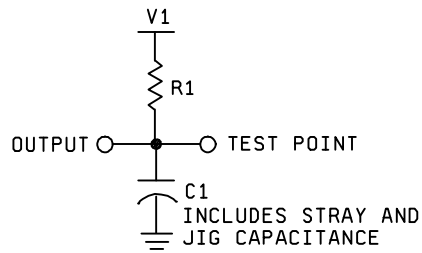


FIGURE 2. Block diagram.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96727
		REVISION LEVEL A	SHEET 8

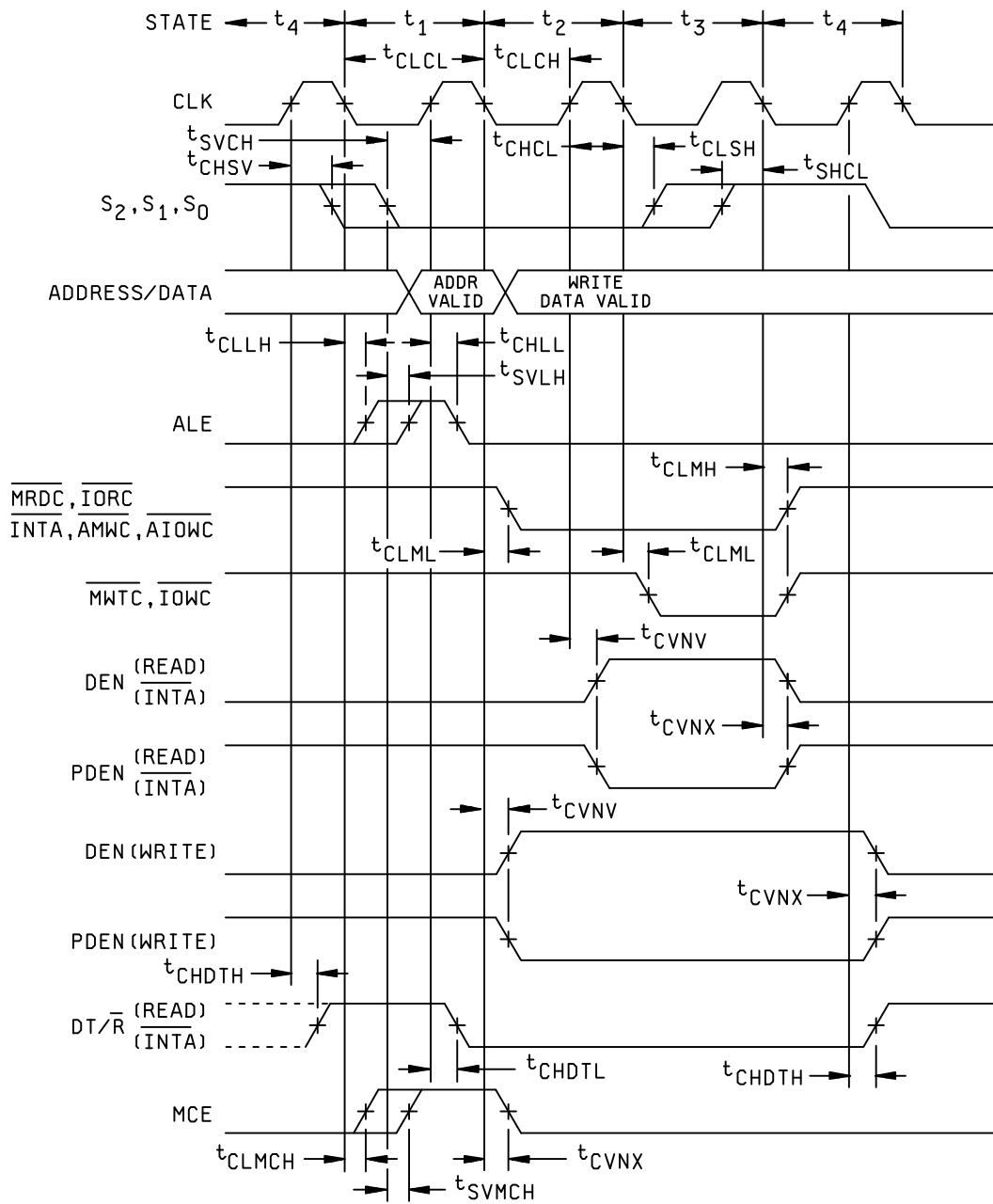


Test Condition	V1	R1	C1
1	2.13 V	220 Ω	80 pF
2	2.29 V	91 Ω	300 pF
3	1.5 V	187 Ω	300 pF
4	1.5 V	187 Ω	50 pF

Note:
CEN must be low or valid prior to t_2 to prevent the command from being generated.

FIGURE 3. Test circuit and timing waveforms.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96727
		REVISION LEVEL A	SHEET 9



Notes:

1. Addresses/data bus is shown only for reference purposes.
2. Leading edge of ALE and MCE is determined by the falling edge of CLK or status going active. Whichever occurs last.
3. All timing measurements are made at 1.5 V unless specified otherwise.

FIGURE 3. Test circuit and timing waveforms – Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96727
		REVISION LEVEL A	SHEET 10

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96727
		REVISION LEVEL B	SHEET 11

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).
- c. Subgroup 4 (C_{IN} , C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	<u>1</u> / 1, 2, 3, 7, 8, 9, 10, 11	<u>1</u> / 1, 2, 3, 7, 8, 9, 10, 11	<u>2</u> / 1, 2, 3, 7, 8, <u>3</u> / 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)			

1/ PDA applies to subgroups 1 and 7.

2/ PDA applies to subgroups 1, 7 and delta's.

3/ Delta limits as specified in Table IIB herein shall be required where specified and the delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Delta limits.

Parameter	Symbol	Delta limits
Standby power supply current	I_{CCSB}	$\pm 3.0 \mu A$
Output leakage current	I_{OZL}, I_{OZH}	$\pm 2.0 \mu A$
Input leakage current	I_{IH}, I_{IL}	$\pm 200 nA$

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96727
		REVISION LEVEL A	SHEET 12

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- b. $T_A = +125^{\circ}\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96727
		REVISION LEVEL A	SHEET 13

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96727
		REVISION LEVEL B	SHEET 14

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-04-20

Approved sources of supply for SMD 5962-96727 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9672701VRC	34371	MD82C88/7

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

34371

Vendor name
and address

Intersil Corporation
2401 Palm Bay Blvd.
P. O. Box 883
Melbourne, FL 32902-883

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.