REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
D	Update boilerplate. Add device types 17 through 24. Add vendor CAGE 61772 as source of supply for device types 17 through 24. Add case outline T. Editorial changes throughout.	94-09-06	M. A. Frye

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	D	D	D	D	D	D	D	D	D	D	D	D	D							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27							

REV STATUS OF SHEETS															
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
James E. Jamison

CHECKED BY
Charles Reusing

APPROVED BY
Michael Frye

DRAWING APPROVAL DATE
93-05-04

REVISION LEVEL
D

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, MEMORY, 2K X 8 CMOS, STATIC RAM (DUAL PORT), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87002**

SHEET 1 OF 27

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-87002	01	X	X
Drawing number	Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish per (See 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	7132SA	2K X 8 dual port static RAM, MASTER	45 ns
02	7132SA	2K X 8 dual port static RAM, MASTER	90 ns
03	7132SA	2K X 8 dual port static RAM, MASTER	70 ns
04	7132SA	2K X 8 dual port static RAM, MASTER	55 ns
05	7132LA	2K X 8 dual port static RAM, MASTER	45 ns
06	7132LA	2K X 8 dual port static RAM, MASTER	90 ns
07	7132LA	2K X 8 dual port static RAM, MASTER	70 ns
08	7132LA	2K X 8 dual port static RAM, MASTER	55 ns
09	7142SA	2K X 8 dual port static RAM, SLAVE	45 ns
10	7142SA	2K X 8 dual port static RAM, SLAVE	90 ns
11	7142SA	2K X 8 dual port static RAM, SLAVE	70 ns
12	7142SA	2K X 8 dual port static RAM, SLAVE	55 ns
13	7142LA	2K X 8 dual port static RAM, SLAVE	45 ns
14	7142LA	2K X 8 dual port static RAM, SLAVE	90 ns
15	7142LA	2K X 8 dual port static RAM, SLAVE	70 ns
16	7142LA	2K X 8 dual port static RAM, SLAVE	55 ns
17	7132SA	2K X 8 dual port static RAM, MASTER	35 ns
18	7132LA	2K X 8 dual port static RAM, MASTER	35 ns
19	7132SA	2K X 8 dual port static RAM, MASTER	25 ns
20	7132LA	2K X 8 dual port static RAM, MASTER	25 ns
21	7142SA	2K X 8 dual port static RAM, SLAVE	35 ns
22	7142LA	2K X 8 dual port static RAM, SLAVE	35 ns
23	7142SA	2K X 8 dual port static RAM, SLAVE	25 ns
24	7142LA	2K X 8 dual port static RAM, SLAVE	25 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CQCC1-N52	52	square leadless chip carrier
Y	See figure 1	48	dual-in-line
Z	GDIP1-T48 or CDIP2-T48	48	dual-in-line
U	See figure 1	48	square leadless chip carrier
T	See figure 1	48	flat pack

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Voltage on any pin with respect to ground 1/ - - - - - - - - - -0.5 V to +7.0 V
Storage temperature range -65°C to +150°C

1/ Unless otherwise specified, all voltages are referenced to V_{SS}.

Power dissipation (P_D)	1 W
Lead temperature (soldering, 5 seconds)	+270°C
Maximum junction temperature (T_J) 2/	+150°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X and Z	See MIL-STD-1835
Case Y	23°C/W 3/
Case U	24°C/W 3/
Case T	20°C/W 3/
Maximum dc output current	50 mA

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C
Input low voltage (V_{IL})	-0.5 to +0.8 V dc 4/
Input high voltage (V_{IH})	+2.2 V to V_{CC} +0.5 V dc 4/
Supply voltage (V_{CC})	+4.5 V to +5.5 V dc 4/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-STD-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
3/ When a thermal resistance value for this case outline is included in MIL-STD-1835, that value shall supersede the value specified herein.
4/ Unless otherwise specified, all voltages are referenced to ground.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ $V_{SS} = 0$ V, $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified		Group A subgroups	Device type	Limits Min	Limits Max	Unit
Output high voltage level	V_{OH}	$V_{CC} = 4.5$ V, $I_{OH} = -4.0$ mA $V_{IN} = V_{IH}$ or $V_{IN} = V_{IL}$		1,2,3	All	2.4		V
Output low voltage level	V_{OL}	$V_{CC} = 4.5$ V, $V_{IN} = V_{IH}$ or $V_{IN} = V_{IL}$	$I_{OL} = 6$ mA	1,2,3	All		0.4	V
			$I_{OL} = 8$ mA				0.5	
Open drain output low voltage (BUSY output)	V_{OL1}	$V_{CC} = 4.5$ V, $I_{OL} = 16$ mA		1,2,3	All		0.5	V
Input high voltage level	V_{IH}			1,2,3	All	2.2		V
Input low voltage level	V_{IL}			1,2,3	All		0.8	V
Input leakage current	I_{IH}	$V_{CC} = 5.5$ V	$V_{IN} = V_{CC}$	1,2,3	All		10	µA
			$V_{IN} = O$ V	1,2,3	All	-10		
Dynamic operating current, both ports active	I_{CC}	$\overline{CE} = V_{IL}$, outputs open		1,2,3	19,23		300	mA
					17,21		290	
					20,24		240	
					01,04,09, 12,18,22		230	
					03,11		225	
					02,10		200	
					05,08, 13,16		185	
					07,15		180	
					06,14		160	
Standby current, both ports inactive, TTL level inputs	I_{SB1}	$\overline{CE}_R$ and $\overline{CE}_L \ge V_{IH}$		1,2,3	17,19, 21,23		80	mA
					01-04 09-12		65	
					18,20, 22,24		60	
					05,07,08, 13,15,16		55	
					06,14		45	
Standby current, one port active, TTL level inputs	I_{SB2}	$\overline{CE}_R$ or $\overline{CE}_L \ge V_{IH}$ Active port outputs open		1,2,3	19,23		195	mA
					17,21		185	
					20,24		160	
					18,22		150	
					01,03,04, 09,11,12		135	
					02,10		125	
					05,07,08, 13,15,16		110	
					06,14		100	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ $V_{SS} = 0$ V, $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Full standby current, both ports inactive, CMOS level inputs	I_{SB3}	$\overline{CE}_R$ and $\overline{CE}_L \ge V_{CC}$ -0.2 V $V_{IN} \ge V_{CC}$ -0.2 V or $V_{IN} \le 0.2$ V	1,2,3	01-04, 09-12, 17,19, 21,23		30	mA
				05-08, 13-16, 18,20, 22,24		10	
Full standby current, one port active, CMOS level inputs	I_{SB4}	$\overline{CE}_R$ or $\overline{CE}_L \ge V_{CC}$ -0.2 V $V_{IN} \ge V_{CC}$ -0.2 V or $V_{IN} \le 0.2$ V Active port outputs open	1,2,3	19,23		185	mA
				17,21		175	
				20,24		150	
				18,22		140	
				01,03,04, 09,11,12		125	
				02,05,10, 13		110	
				06,07,08, 14,15,16		90	
Output leakage current	I_{OZ}	$\overline{CE} \le V_{IH}$ $V_{OUT} = 0$ V or $V_{OUT} = V_{CC}$	1,2,3	All	-10	10	µA
V_{CC} for data retention	V_{DR}	$V_{CC} = 2.0$ V, $\overline{CE} \ge V_{CC}$ - 0.2 V, $V_{IN} \ge V_{CC}$ - 0.2 V or $V_{IN} \le 0.2$ V	1,2,3	05-08, 13-16, 18,20, 22,24	2.0		V
Data retention current	I_{CCDR}	$V_{CC} = 2.0$ V, $\overline{CE} \ge V_{CC}$ -0.2 V $V_{IN} \ge V_{CC}$ -0.2 V or $V_{IN} \le 0.2$ V	1,2,3	05-08, 13-16, 18,20, 22,24		4000	µA
Chip deselect to data retention time 1/	t_{CDR}	$V_{CC} = 2.0$ V, $\overline{CE} \ge V_{CC}$ -0.2 V $V_{IN} \ge V_{CC}$ -0.2 V or $V_{IN} \le 0.2$ V	9,10,11	05-08, 13-16, 18,20, 22,24	0		ns
Operation recovery time	t_R	$V_{CC} = 2.0$ V, $\overline{CE} \ge V_{CC}$ -0.2 V $V_{IN} \ge V_{CC}$ -0.2 V or $V_{IN} \le 0.2$ V 1/	9,10,11	05-08, 13-16, 18,20, 22,24	t_{AVAV} 2/		ns
Functional tests		See 4.3.1d	7,8A,8B	All			
Input capacitance	C_{IN}	$T_A = 25^\circ C$, $V_{IN} = 0$ V, f= 1 MHz, see 4.3.1c	4	All		11	pF
Output capacitance	C_{OUT}	$T_A = 25^\circ C$, $V_{OUT} = 0$ V, f = 1 MHz, see 4.3.1c	4	All		11	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ $V_{SS} = 0$ V, 4.5 V $\le V_{CC} \le$ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Read/write cycle time	t_{AVAV}	See figure 5	9,10,11	01,05,09, 13	45		ns
				02,06,10, 14	90		
				03,07,11, 15	70		
				04,08,12, 16	55		
				17,18,21, 22	35		
				19,20,23, 24	25		
Address access time	t_{AVQV}		9,10,11	01,05,09, 13		45	ns
				02,06,10, 14		90	
				03,07,11, 15		70	
				04,08,12, 16		55	
				17,18,21, 22		35	
				19,20,23, 24		25	
Chip enable access time	t_{ELQV}		9,10,11	01,05,09, 13		45	ns
				02,06,10, 14		90	
				03,07,11, 15		70	
				04,08,12, 16		55	
				17,18,21, 22		35	
				19,20,23, 24		25	
Output enable access time	t_{OLQV}		9,10,11	02,03,06, 07,10,11, 14,15		40	ns
				04,08,12, 16		35	
				01,05,09, 13		30	
				17,18,21, 22		25	
				19,20,23, 24		12	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ $V_{SS} = 0$ V, 4.5 V $\le V_{CC} \le$ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Output hold from address change	t_{AVQX}	See figure 5	9,10,11	02,06,10, 14	10		ns
				01,03-05, 07-09, 11-13, 15-24	0		
Output low Z time 1/ 3/	t_{OLQZ}		9,10,11	01-16,17, 18,21,22	5		ns
				19,20,23, 24	0		
Output high Z time 1/ 3/	t_{OHQZ}		9,10,11	02,06,10, 14		40	ns
				03,07,11, 15		35	
				04,08,12, 16		30	
				01,05,09, 13		20	
				17,18,21, 22		15	
				19,20,23, 24		10	
Chip enable to power-up time 1/	t_{ELPU}		9,10,11	All	0		ns
Chip disable to power-down time 1/	t_{EHPD}		9,10,11	All		50	ns
Write cycle time 4/	t_{AVAV}		9,10,11	01,05,09, 13	45		ns
				02,06,10, 14	90		
				03,07,11, 15	70		
				04,08,12, 16	55		
				17,18,21, 22	35		
				19,20,23, 24	25		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ $V_{SS} = 0$ V, $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Chip enable to end of write	t_{ELWH}	See figure 5	9,10,11	01,05,09, 13	35		ns
				02,06,10, 14	85		
				03,07,11, 15	50		
				04,08,12, 16	40		
				17,18,21, 22	30		
				19,20,23, 24	20		
Address valid to end of write	t_{AVWH}		9,10,11	01,05,09, 13	35		ns
				02,06,10, 14	85		
				03,07,11, 15	50		
				04,08,12, 16	40		
				17,18,21, 22	30		
				19,20,23, 24	20		
Address setup time	t_{AVWL}		9,10,11	All	0		ns
Write pulse width 5/	t_{WLWH}		9,10,11	01,05,09, 13	35		ns
				02,06,10, 14	55		
				03,07,11, 15	50		
				04,08,12, 16	40		
				17,18,21, 22	30		
				19,20,23, 24	20		
Write recovery time	t_{EHOL}		9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ $V_{SS} = 0$ V, $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Data valid to end of write	t_{DVWH}		9,10,11	02,06,10, 14	40		ns
				03,07,11, 15	30		
				01,04,05, 08,09,12, 13,16-18, 21,22	20		
				19,20,23, 24	12		
Output high Z time 1/ 3/	t_{OHQZ}		9,10,11	02,06,10, 14		40	ns
				03,07,11, 15		35	
				04,08,12, 16		30	
				01,05,09, 13		20	
				17,18,21, 22		15	
				19,20,23, 24		10	
Data hold time	t_{WHDX}		9,10,11	All	0		ns
Write enabled to output in high Z 1/ 3/	t_{WLQZ}		9,10,11	02,06,10, 14		40	ns
				03,07,11, 15		35	
				04,08,12, 16		30	
				01,05,09, 13		20	
				17,18,21, 22		15	
				19,20,23, 24		10	
Output active from end of write 1/ 3/	t_{WHQX}		9,10,11	All	0		ns
Write to $\overline{BUSY}$ 6/	t_{WB}		9,10,11	09-16, 21-24	0		ns
Write to hold after $\overline{BUSY}$ 7/	t_{WH}		9,10,11	09-16,21, 22	20		ns
				23,24	15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ $V_{SS} = 0$ V, $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
$\overline{BUSY}$ access time to address	t_{BAA}	See figure 5	9,10,11	01,05, 17,18		35	ns
				02,03,04, 06,07,08		45	
				19,20		25	
$\overline{BUSY}$ disable time to address	t_{BDA}		9,10,11	01,05		35	ns
				02,06		45	
				03,04, 07,08		40	
				17,18		30	
				19,20		20	
$\overline{BUSY}$ access time to chip enable	t_{BAC}		9,10,11	01,05, 17,18		30	ns
				02,06		45	
				03,04, 07,08		35	
				19,20		20	
$\overline{BUSY}$ disable time to chip enable	t_{BDC}		9,10,11	01,05, 17,18		25	ns
				02,06		45	
				03,04, 07,08		30	
				19,20		20	
Write pulse to data delay 8/	t_{WDD}		9,10,11	01,05, 09,13		70	ns
				02,06, 10,14		100	
				03,07, 11,15		90	
				04,08, 12,16		80	
				17,18		60	
				19,20		50	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ $V_{SS} = 0$ V, $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Write data valid to read data delay 8/	t_{DDD}	See figure 5	9,10,11	01,05, 09,13		45	ns
				02,06, 10,14		90	
				03,07, 11,15		70	
				04,08, 12,16		55	
				17-20		35	
$\overline{BUSY}$ disable to valid data 9/	t_{BDD}		9,10,11	01-08, 17-20		6/	ns
Arbitration priority setup time 10/	t_{APS}		9,10,11	01-08, 17-20	5		ns

1/ This parameter not required to be tested but shall be guaranteed to the limits specified in table I.
2/ t_{RC} = Read Cycle Time = t_{AVAV}.
3/ Transition is measured ±500 mV from low or high impedance voltage with load. R_1 = 1250 ohms, C_L = 5 picofarads.
4/ For master/slave combination, $t_{AVAV} = t_{BAA} + t_{WLWH}$.
5/ Specified for OE at high.
6/ For slave device only. To ensure that the write cycle is completed after contention.
7/ To ensure that a write cycle is completed after contention.
8/ Port-to-port delay through RAM cells from writing port to reading port.
9/ t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WLWH}$ (actual) or $t_{DDD} - t_{DVWH}$ (actual).
10/ To ensure that the earlier of the two ports wins.

Case outline Y

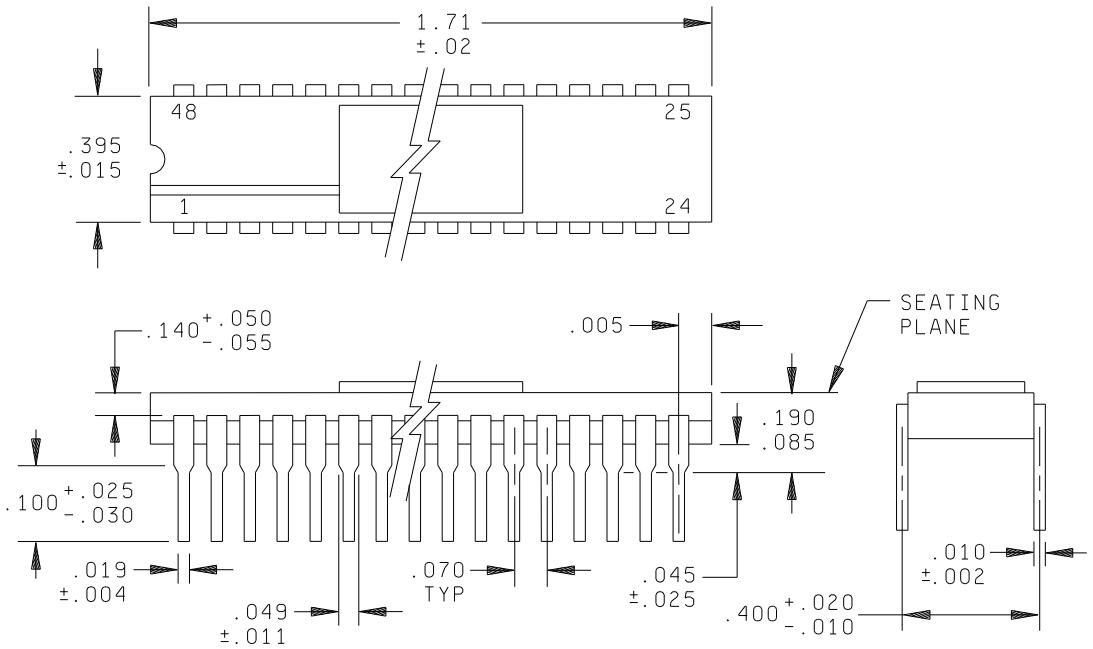
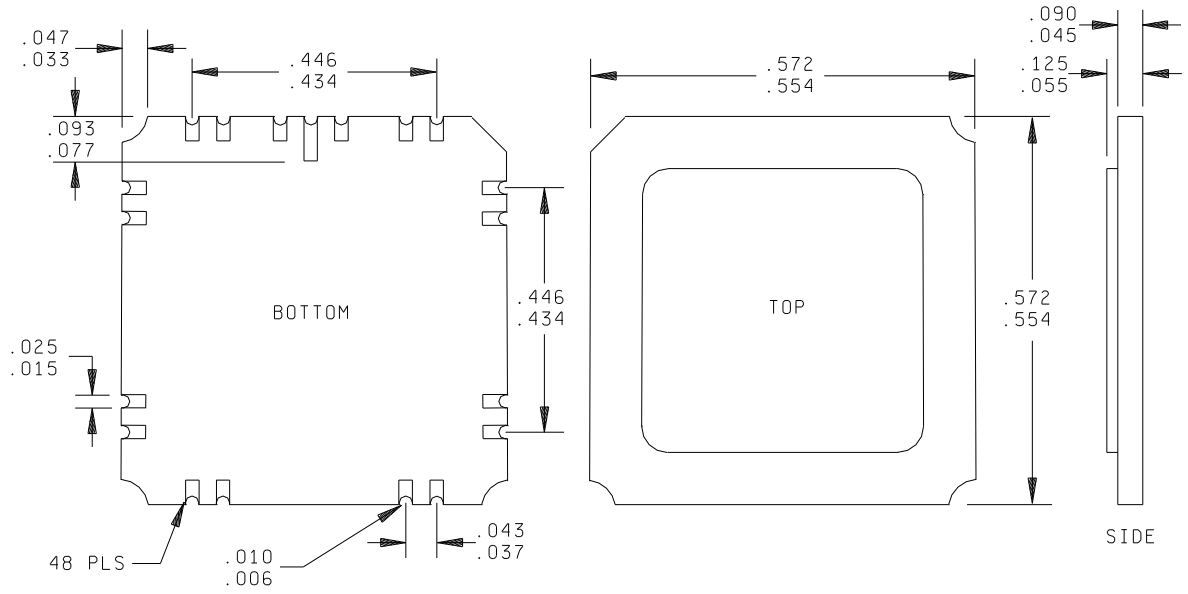


FIGURE 1. Package dimensions.

Case outline U

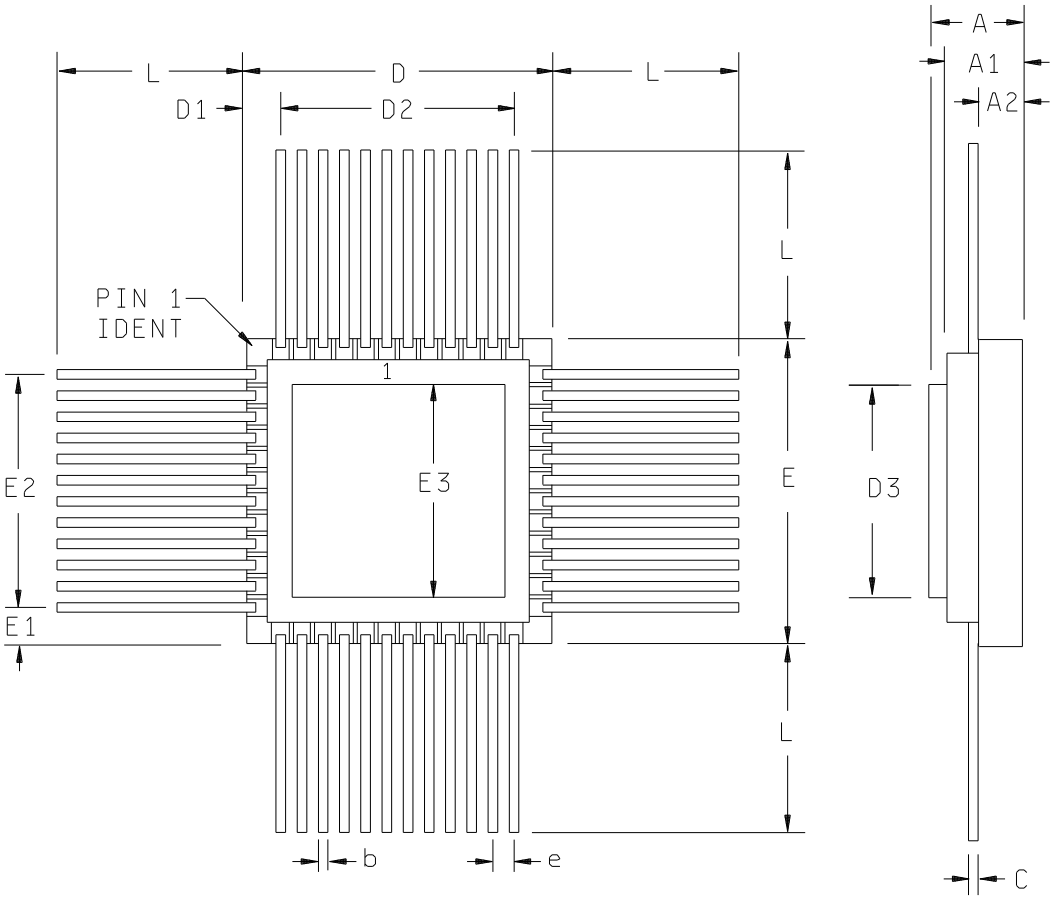


Inches	mm	Inches	mm
.006	0.15	.055	1.40
.010	0.25	.077	1.96
.015	0.38	.090	2.29
.025	0.64	.093	2.36
.033	0.84	.125	3.18
.037	0.94	.434	11.02
.043	1.09	.446	11.33
.045	1.14	.554	14.07
.047	1.19	.572	15.53

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm).

FIGURE 1. Package dimensions - Continued.

Case outline T



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.089	.108	2.26	2.74
A1	.079	.096	2.01	2.44
A2	.058	.073	1.47	1.85
B	.018	.022	0.46	0.56
C	.008	.010	0.20	0.25
D		.750		19.05
D1	.100 REF		2.54	
D2	.550 BSC		13.97	
D3		.630		16.00
e	.050 BSC		1.27	
E		.750		19.05
E1	.100 REF		2.54	
E2	.550 BSC		13.97	
E3		.630		16.00
L	.350	.450	8.89	11.43
ND	12			
NE	12			

FIGURE 1. Case outline - Continued.

Device types	All		Device types	All	
Case outlines	Y, Z, U, and T	X	Case outlines	Y, Z, U, and T	X
Terminal number	Terminal symbol		Terminal number	Terminal symbol	
1	$\overline{CE}_L$	$\overline{CE}_L$	27	I/O_{2R}	I/O_{0R}
2	$R/\overline{W}_L$	$R/\overline{W}_L$	28	I/O_{3R}	I/O_{1R}
3	$\overline{BUSY}_L$	$\overline{BUSY}_L$	29	I/O_{4R}	I/O_{2R}
4	A_{10L}	NC	30	I/O_{5R}	I/O_{3R}
5	OE_L	A_{10L}	31	I/O_{6R}	I/O_{4R}
6	A_{0L}	$\overline{OE}_L$	32	I/O_{7R}	I/O_{5R}
7	A_{1L}	A_{0L}	33	A_{9R}	I/O_{6R}
8	A_{2L}	A_{1L}	34	A_{8R}	I/O_{7R}
9	A_{3L}	A_{2L}	35	A_{7R}	NC
10	A_{4L}	A_{3L}	36	A_{6R}	A_{9R}
11	A_{5L}	A_{4L}	37	A_{5R}	A_{8R}
12	A_{6L}	A_{5L}	38	A_{4R}	A_{7R}
13	A_{7L}	A_{6L}	39	A_{3R}	A_{6R}
14	A_{8L}	A_{7L}	40	A_{2R}	A_{5R}
15	A_{9L}	A_{8L}	41	A_{1R}	A_{4R}
16	I/O_{0L}	A_{9L}	42	A_{0R}	A_{3R}
17	I/O_{1L}	I/O_{0L}	43	$\overline{OE}_R$	A_{2R}
18	I/O_{2L}	I/O_{1L}	44	A_{10R}	A_{1R}
19	I/O_{3L}	I/O_{2L}	45	$\overline{BUSY}_R$	A_{0R}
20	I/O_{4L}	I/O_{3L}	46	$R/\overline{W}_R$	$\overline{OE}_R$
21	I/O_{5L}	I/O_{4L}	47	CE_R	A_{10R}
22	I/O_{6L}	I/O_{5L}	48	V_{CC}	NC
23	I/O_{7L}	I/O_{6L}	49	---	$\overline{BUSY}_R$
24	GND	I/O_{7L}	50	---	$R/\overline{W}_R$
25	I/O_{0R}	NC	51	---	$\overline{CE}_R$
26	I/O_{1R}	GND	52	---	V_{CC}

FIGURE 2. Terminal connections.

Noncontention read/write control

Left or right port (see note 1)				Function
$R/\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port disabled and in power-down mode I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, power-down mode I_{SB1} or I_{SB3}
L	L	X	Data in	Data on port written into memory 2/
H	L	L	Data out	Data in memory output on port 3/
H	L	H	Z	High impedance outputs

H = High, L = Low, X = Don't care, Z = High impedance.

NOTES:
1. $A_{OL} - A_{10L} \neq A_{OR} - A_{10R}$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid. See t_{WDD} and t_{DDD} timing.

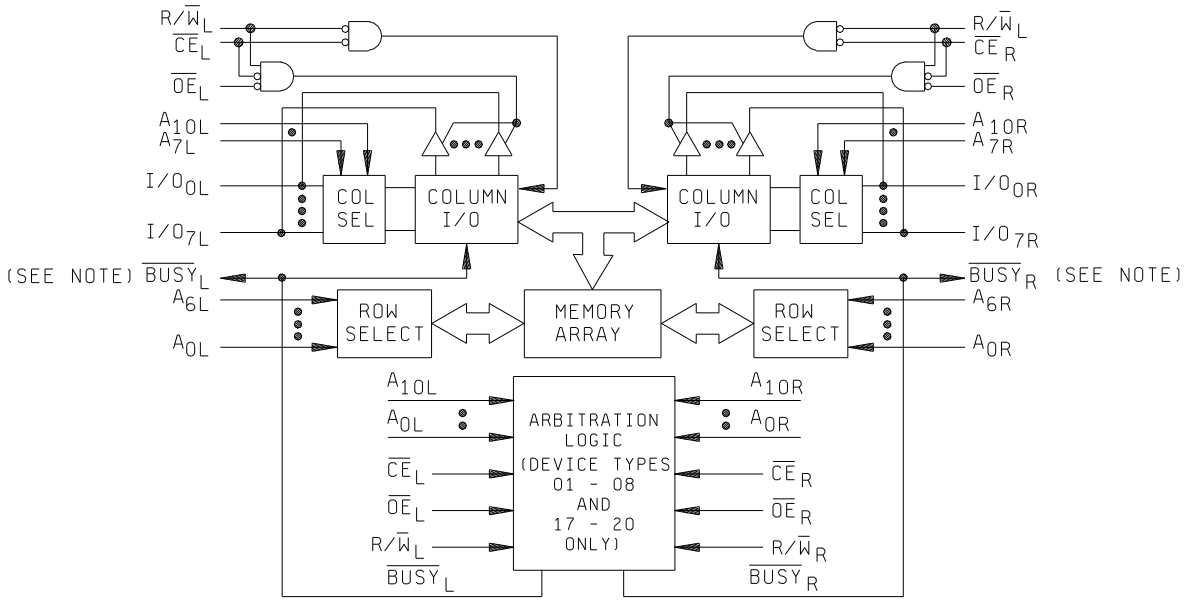
FIGURE 3. Truth tables.

Bus arbitration (see notes)

Left port		Right port		Flags		
$\overline{CE}_L$	$\neq A_{OL} - A_{10L}$	$\overline{CE}_R$	$\neq A_{OR} - A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
H	X	H	X	H	H	No contention
L	Any	H	X	H	H	No contention
H	X	L	Any	H	H	No contention
L	$\neq A_{OR} - A_{10R}$	L	$\neq A_{OL} - A_{10L}$	H	H	No contention
Address arbitration with $\overline{CE}$ low before address match						
L	LV5R	L	LV5R	H	L	Left-port wins
L	RV5L	L	RV5L	L	H	Right-port wins
L	Same	L	Same	H	L	Arbitration resolved
L	Same	L	Same	L	H	Arbitration resolved
$\overline{CE}$ arbitration with address match before $\overline{CE}$						
LL5R	$= A_{OR} - A_{10R}$	LL5R	$= A_{OL} - A_{10L}$	H	L	Left-port wins
RL5L	$= A_{OR} - A_{10R}$	RL5L	$= A_{OL} - A_{10L}$	L	H	Right-port wins
LW5R	$= A_{OR} - A_{10R}$	LW5R	$= A_{OL} - A_{10L}$	H	L	Arbitration resolved
LW5R	$= A_{OR} - A_{10R}$	LW5R	$= A_{OL} - A_{10L}$	L	H	Arbitration resolved

NOTES:
1. X = Don't care, L = Low, H = High.
2. LV5R = Left address valid $\geq$ 5 ns before right address.
3. RV5L = Right address valid $\geq$ 5 ns before left address.
4. Same = Left and right addresses match within 5 ns of each other.
5. LL5R = Left $\overline{CE}$ = Low $\geq$ 5 ns before right $\overline{CE}$.
6. RL5L = Right $\overline{CE}$ = Low $\geq$ 5 ns before left $\overline{CE}$.
7. LW5R = Left and right $\overline{CE}$ = Low within 5 ns of each other.

FIGURE 3. Truth tables - Continued.



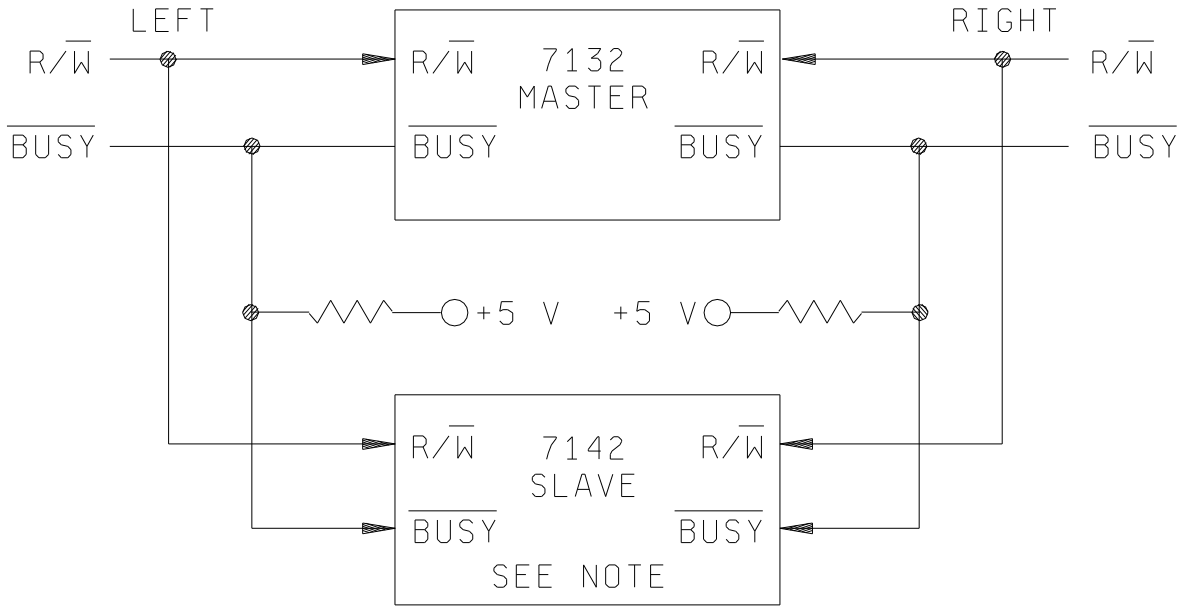
NOTE: For device types 01-08, 17-20: BUSY is open drain and requires pull-up resistor. For device types 09-16, 21-24: BUSY is input.

Pin names

Left port	Right port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/write enable
$\overline{OE}_L$	$\overline{OE}_R$	Output enable
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy flag
A_{0L} - A_{10L}	A_{0R} - A_{10R}	Address
I/O_{0L}-I/O_{7L}	I/O_{0R}-I/O_{7R}	Data input/output
V_{CC}		Power
GND		Ground

FIGURE 4. Functional block diagram.

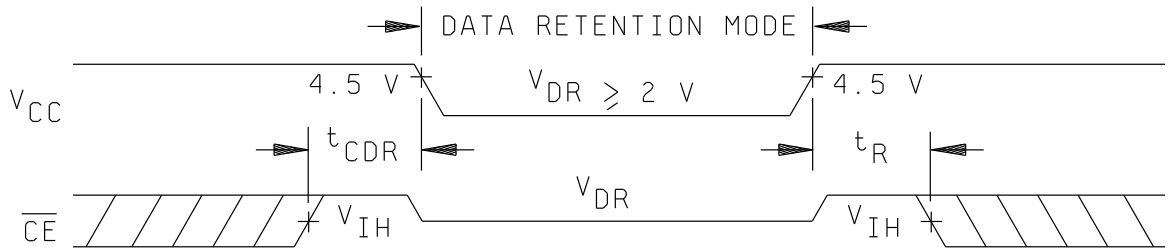
16-bit master/slave dual-port memory system



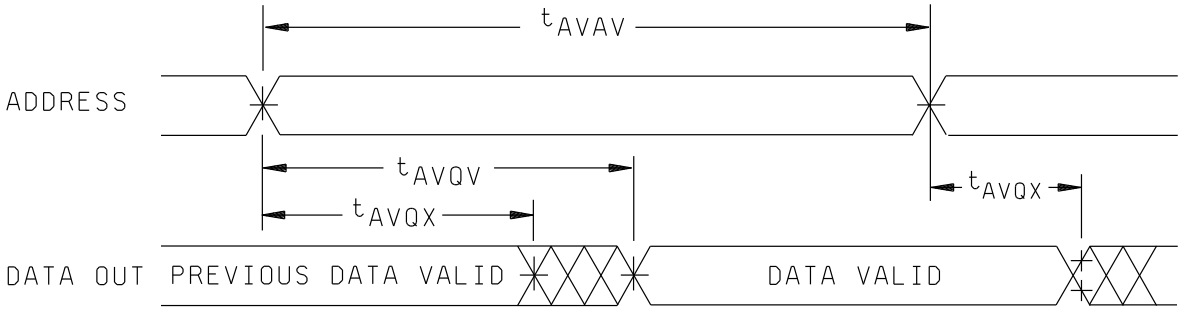
NOTE: No arbitration in 7142 (slave). $\overline{\text{BUSY}}$-in inhibits write in 7142 (slave).

FIGURE 4. Functional block diagram - Continued.

LOW V_{CC} DATA RETENTION WAVEFORM (FOR LA DEVICES ONLY)



READ CYCLE 1: SEE NOTES 1, 2, AND 6



READ CYCLE 2: SEE NOTES 1 AND 3

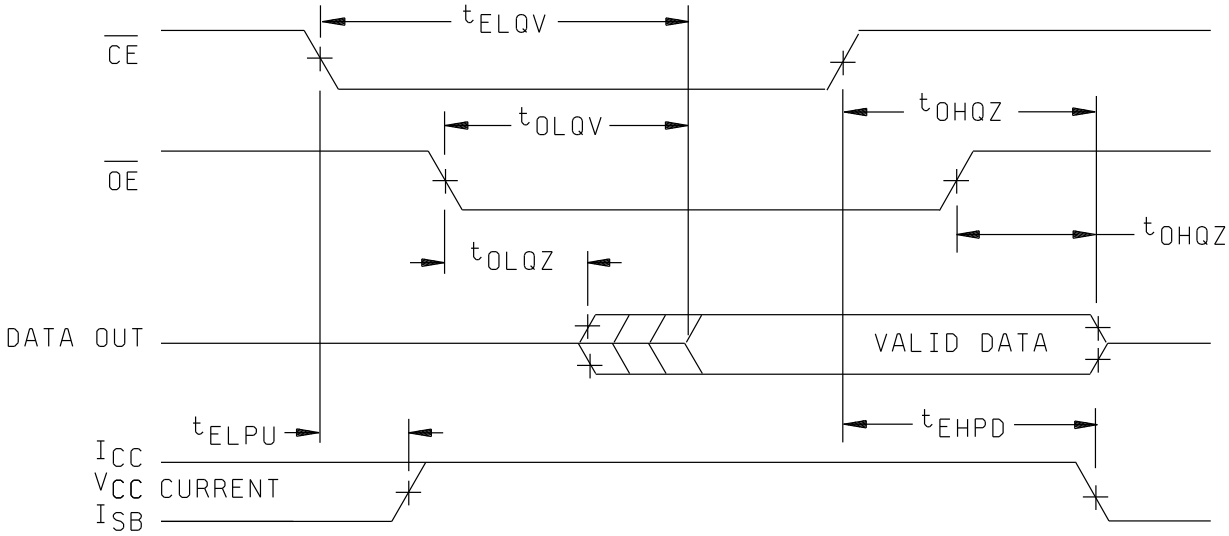
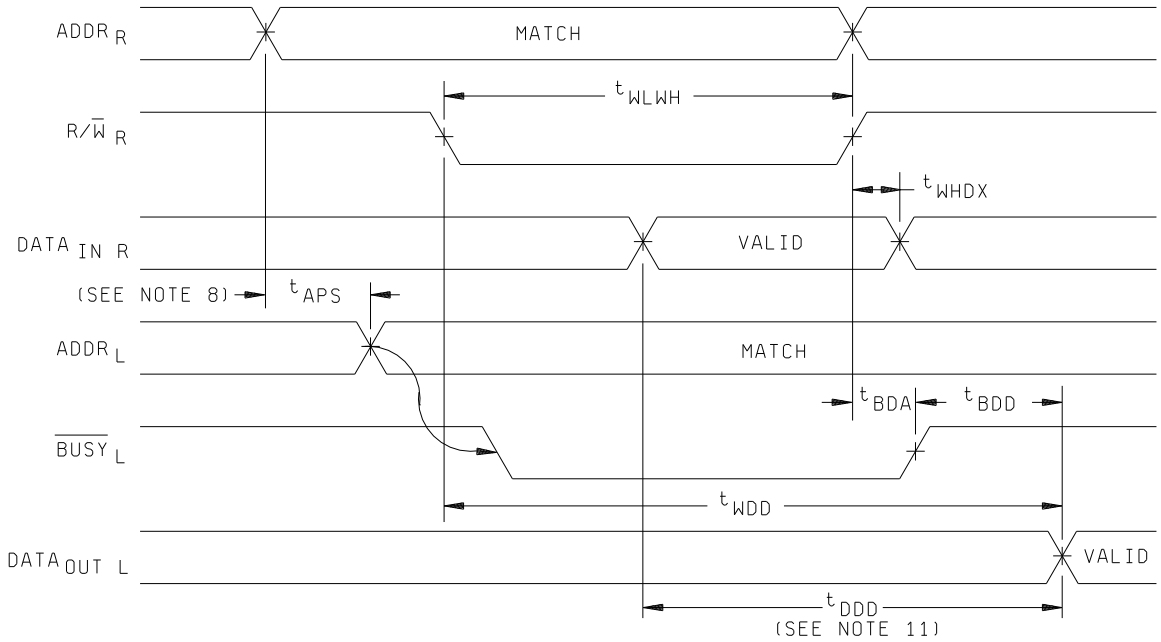


FIGURE 5. Timing diagrams and test conditions.

TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (SEE NOTES 8,9 AND 10)
FOR DEVICE TYPES 01-08 AND 17-20 ONLY



TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ FOR DEVICE TYPES
09-16 AND 21-24 ONLY

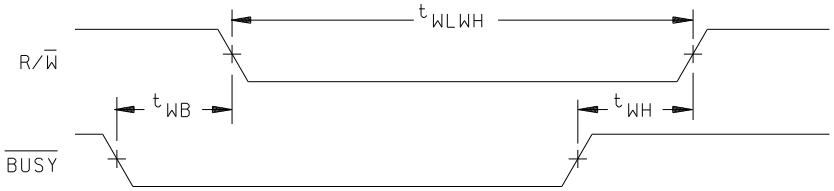
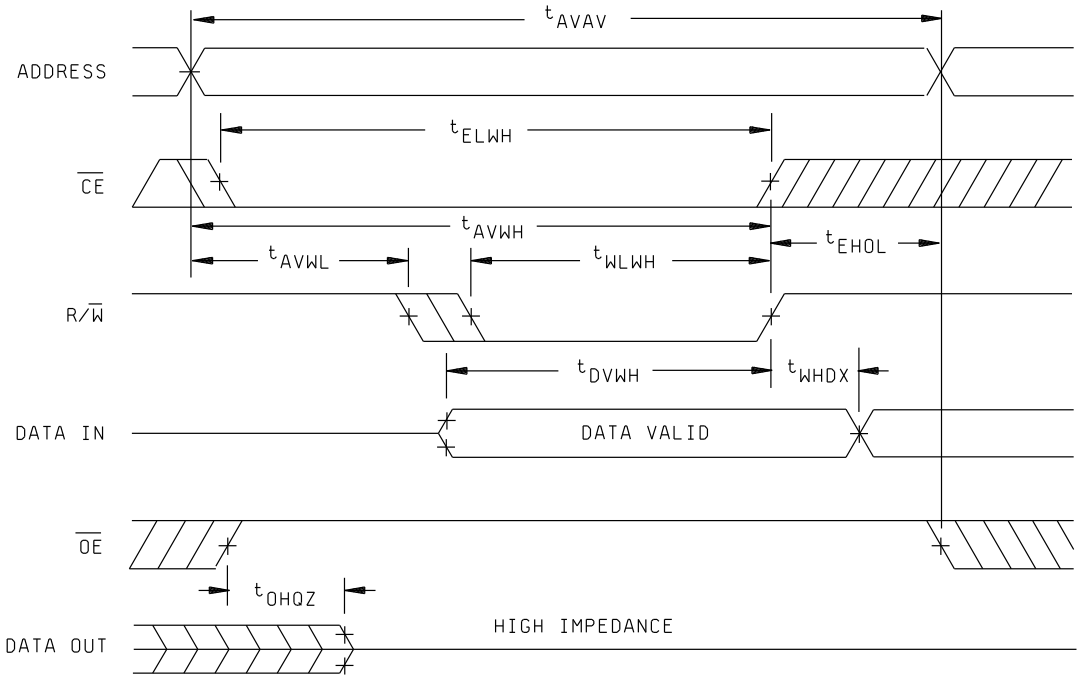


FIGURE 5. Timing diagrams and test conditions - Continued.

WRITE CYCLE 2: SEE NOTES 4,7,12 AND 13
(EITHER SIDE)



WRITE CYCLE 1: SEE NOTES 4,7,12,13 AND 14
(EITHER SIDE)

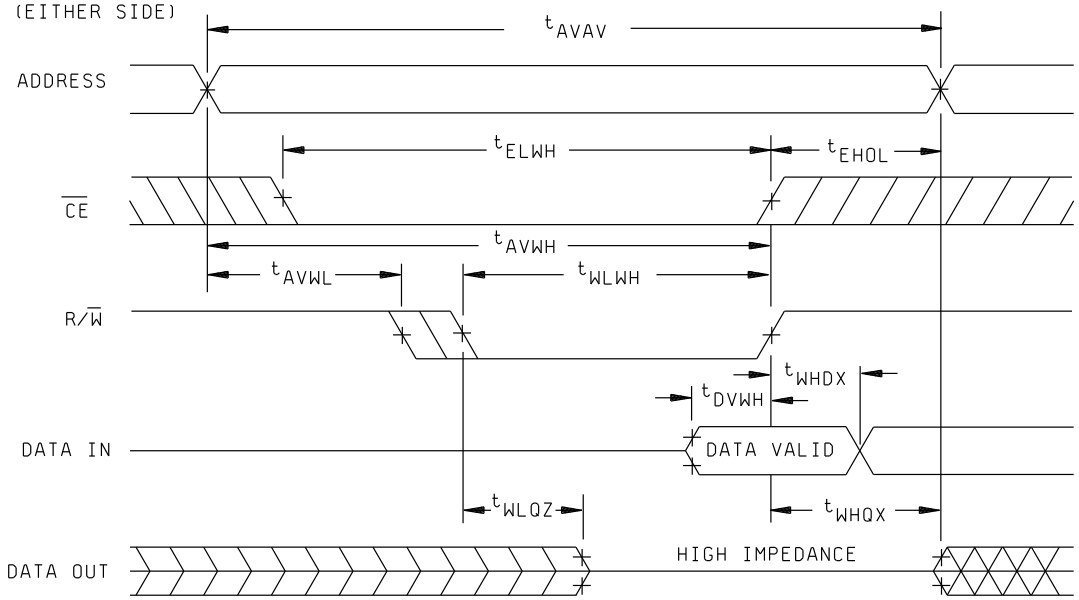
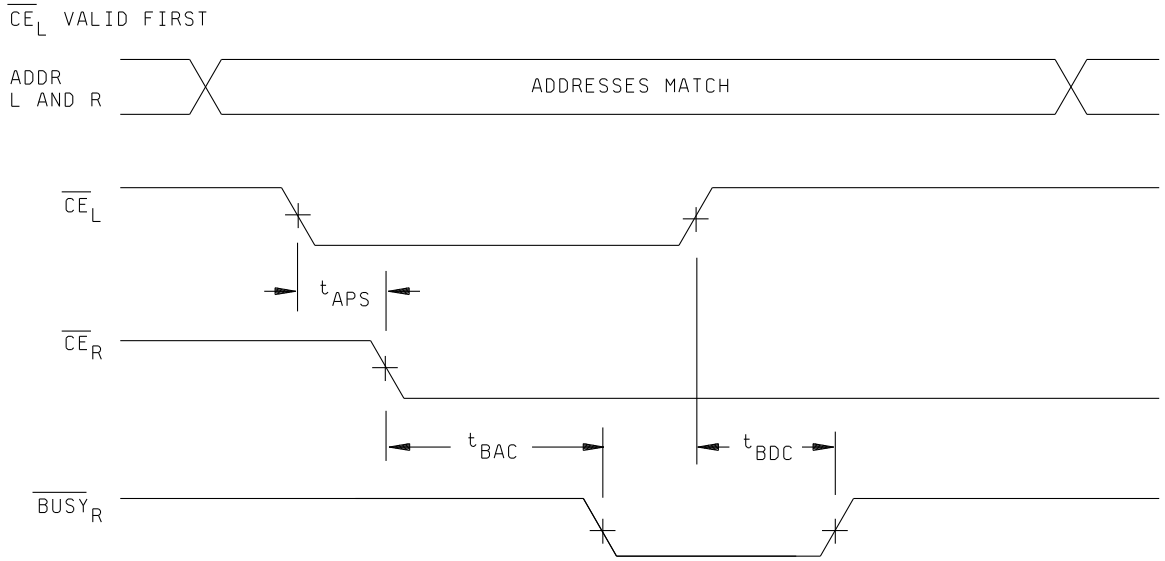


FIGURE 5. Timing diagrams and test conditions - Continued.

CONTENTION CYCLE 1: $\overline{CE}$ ARBITRATION FOR DEVICE TYPES 01-08, 17-20 ONLY



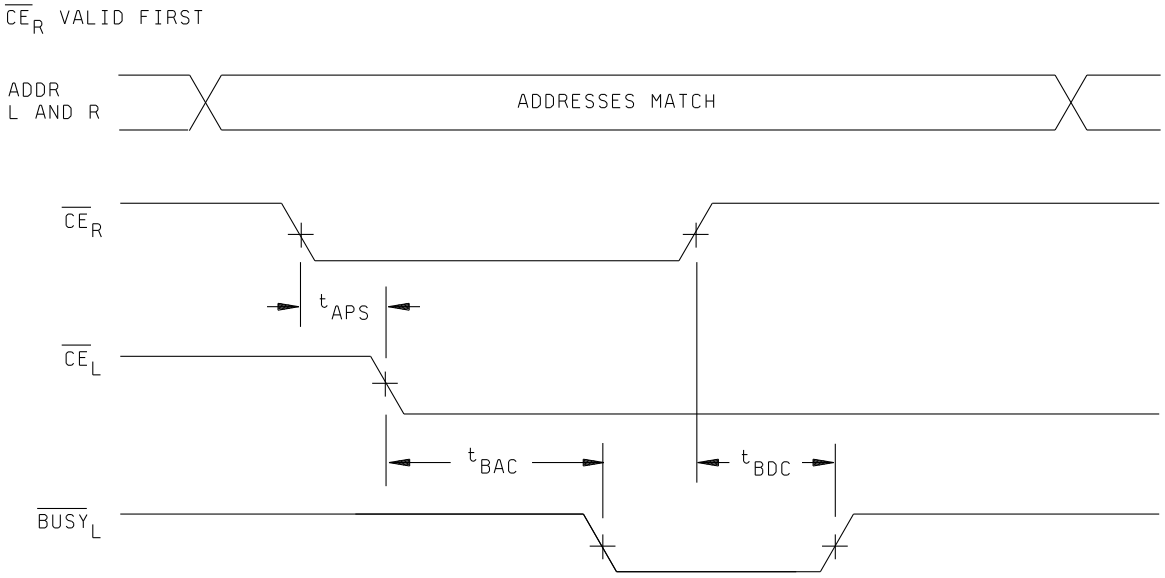
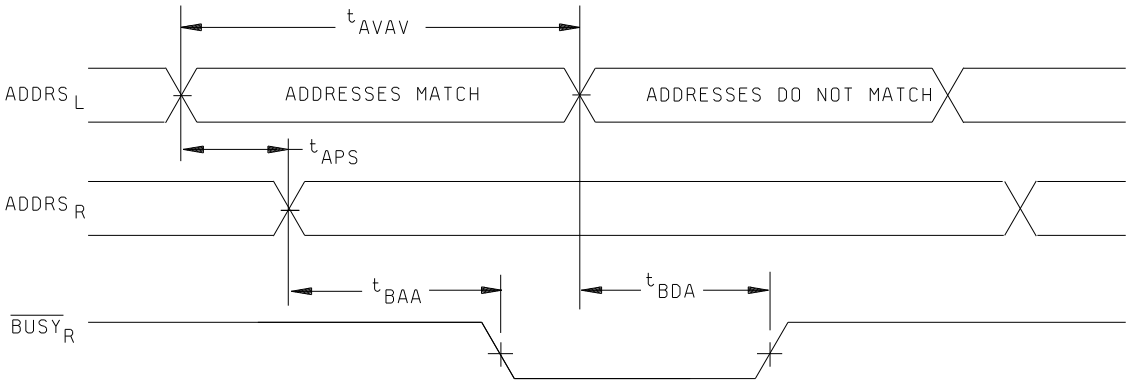


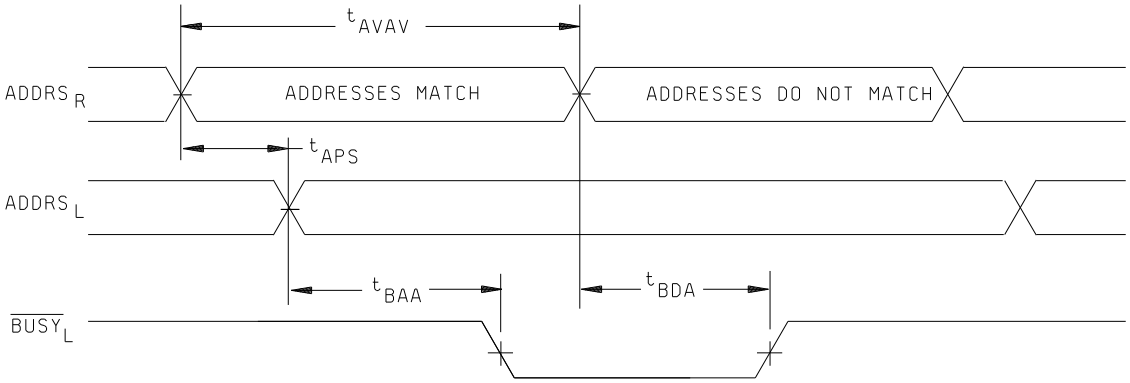
FIGURE 5. Timing diagrams and test conditions - Continued.

CONTENTION CYCLE 2: ADDRESS VALID ARBITRATION FOR
DEVICE TYPES 01-8 AND 17-20
SEE NOTE 5

LEFT ADDRESS VALID FIRST:



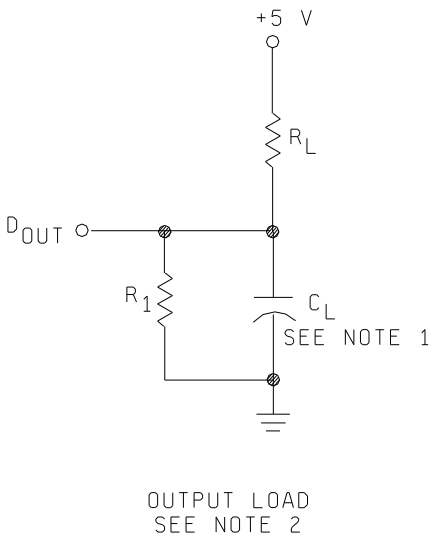
RIGHT ADDRESS VALID FIRST:



NOTES:
1. R/$\overline{W}$ is high for read cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/W low transition, the outputs remain in the high impedance state.
5. $\overline{CE}_L = \overline{CE}_R = V_{IL}$.
6. $\overline{OE} = V_{IL}$.
7. R/$\overline{W} = V_{IH}$ during address transition.
8. To ensure that the earlier of the two ports wins.
9. Write cycle parameters should be adhered to in order to ensure proper writing.
10. Device is continuously enabled for both ports.
11. $\overline{OE}$ at low for the reading port.
12. A write occurs during the overlap (t_{ELWH} or t_{WLWH}) of a low $\overline{CE}$ and a low R/$\overline{W}$.
13. t_{EHOL} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
14. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WLWH} or (t_{WLQZ} + t_{DVWH}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DVWH}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WLWH}.
15. During this period, the I/O pins are in the output state and input signals must not be applied.

FIGURE 5. Timing diagrams and test conditions - Continued.

NOTES:
1. Includes jig and probe capacitance.
2. See output load legend.



Output load legend

Row	Devices/conditions	C_L	R_L	R_1
1	02-04, 06-08, 10-12, and 14-16; for all ac parameters except as indicated in row 3	100 pF	1250Ω	775Ω
2	01, 05, 09, 13, and 17-24; for all ac parameters except as indicated in row 3	30 pF	1250Ω	775Ω
3	All devices; for ac parameters (t_{OHQZ}, t_{OLQZ}, t_{WLQZ}, and t_{WHOX}) only	5 pF	1250Ω	775Ω
4	01-08; $\overline{BUSY}$	100 pF	270Ω	Not used
5	17-20; $\overline{BUSY}$	30 pF	270Ω	Not used

AC test conditions

Input pulse levels Input rise and fall times Input timing reference levels Output reference levels	GND to 3.0 V 5 ns 1.5 V 1.5 V
Output load	See above

FIGURE 5. Timing diagrams and test conditions - Continued.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*, 8A,8B,9
Group A test requirements (method 5005)	1,2,3,4**,7*, 8A,8B,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8A,8B

* PDA applies to subgroups 1 and 7.
** See 4.3.1d.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth tables. The truth tables shall be as specified on figure 3.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 4.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and figure 1.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal .

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 94-09-06

Approved sources of supply for SMD 5962-87002 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8700201XX	2/	
5962-8700201YX	2/	
5962-8700201ZX	61772	IDT7132SA45CB
5962-8700201UX	61772	IDT7132SA45L48B
5962-8700201TX	61772	IDT7132SA45FB
5962-8700202XX	2/	
5962-8700202YX	2/	
5962-8700202ZX	61772	IDT7132SA90CB
5962-8700202UX	61772	IDT7132SA90L48B
5962-8700202TX	61772	IDT7132SA90FB
5962-8700203XX	2/	
5962-8700203YX	2/	
5962-8700203ZX	61772	IDT7132SA70CB
5962-8700203UX	61772	IDT7132SA70L48B
5962-8700203TX	61772	IDT7132SA70FB
5962-8700204XX	2/	
5962-8700204YX	2/	
5962-8700204ZX	61772	IDT7132SA55CB
5962-8700204UX	61772	IDT7132SA55L48B
5962-8700204TX	61772	IDT7132SA55FB

See footnotes at end of table.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8700205XX	2/	
5962-8700205YX	2/	
5962-8700205ZX	61772	IDT7132LA45CB
5962-8700205UX	61772	IDT7132LA45L48B
5962-8700205TX	61772	IDT7132LA45FB
5962-8700206XX	2/	
5962-8700206YX	2/	
5962-8700206ZX	61772	IDT7132LA90CB
5962-8700206UX	61772	IDT7132LA90L48B
5962-8700206TX	61772	IDT7132LA90FB
5962-8700207XX	2/	
5962-8700207YX	2/	
5962-8700207ZX	61772	IDT7132LA70CB
5962-8700207UX	61772	IDT7132LA70L48B
5962-8700207TX	61772	IDT7132LA70FB
5962-8700208XX	2/	
5962-8700208YX	2/	
5962-8700208ZX	61772	IDT7132LA55CB
5962-8700208UX	61772	IDT7132LA55L48B
5962-8700208TX	61772	IDT7132LA55FB
5962-8700209XX	2/	
5962-8700209YX	2/	
5962-8700209ZX	61772	IDT7142SA45CB
5962-8700209UX	61772	IDT7142SA45L48B
5962-8700209TX	61772	IDT7142SA45FB

See footnotes at end of table.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8700210XX	2/	
5962-8700210YX	2/	
5962-8700210ZX	61772	IDT7142SA90CB
5962-8700210UX	61772	IDT7142SA90L48B
5962-8700210TX	61772	IDT7142SA90FB
5962-8700211XX	2/	
5962-8700211YX	2/	
5962-8700211ZX	61772	IDT7142SA70CB
5962-8700211UX	61772	IDT7142SA70L48B
5962-8700211TX	61772	IDT7142SA70FB
5962-8700212XX	2/	
5962-8700212YX	2/	
5962-8700212ZX	61772	IDT7142SA55CB
5962-8700212UX	61772	IDT7142SA55L48B
5962-8700212TX	61772	IDT7142SA55FB
5962-8700213XX	2/	
5962-8700213YX	2/	
5962-8700213ZX	61772	IDT7142LA45CB
5962-8700213UX	61772	IDT7142LA45L48B
5962-8700213TX	61772	IDT7142LA45FB
5962-8700214XX	2/	
5962-8700214YX	2/	
5962-8700214ZX	61772	IDT7142LA90CB
5962-8700214UX	61772	IDT7142LA90L48B

See footnotes at end of table.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8700214TX	61772	IDT7142LA90FB
5962-8700215XX	2/	
5962-8700215YX	2/	
5962-8700215ZX	61772	IDT7142LA70CB
5962-8700215UX	61772	IDT7142LA70L48B
5962-8700215TX	61772	IDT7142LA70FB
5962-8700216XX	2/	
5962-8700216YX	2/	
5962-8700216ZX	61772	IDT7142LA55CB
5962-8700216UX	61772	IDT7142LA55L48B
5962-8700216TX	61772	IDT7142LA55FB
5962-8700217ZX	61772	IDT7132SA35CB
5962-8700217UX	61772	IDT7132SA35L48B
5962-8700217TX	61772	IDT7132SA35FB
5962-8700218ZX	61772	IDT7132LA35CB
5962-8700218UX	61772	IDT7132LA35L48B
5962-8700218TX	61772	IDT7132LA35FB
5962-8700219ZX	61772	IDT7132SA25CB
5962-8700219UX	61772	IDT7132SA25L48B
5962-8700219TX	61772	IDT7132SA25FB
5962-8700220ZX	61772	IDT7132LA25CB
5962-8700220UX	61772	IDT7132LA25L48B
5962-8700220TX	61772	IDT7132LA25FB
5962-8700221ZX	61772	IDT7142SA35CB
5962-8700221UX	61772	IDT7142SA35L48B
5962-8700221TX	61772	IDT7142SA35FB

See footnotes at end of table.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8700222ZX	61772	IDT7142LA35CB
5962-8700222UX	61772	IDT7142LA35L48B
5962-8700222TX	61772	IDT7142LA35FB
5962-8700223ZX	61772	IDT7142SA25CB
5962-8700223UX	61772	IDT7142SA25L48B
5962-8700223TX	61772	IDT7142SA25FB
5962-8700224ZX	61772	IDT7142LA25CB
5962-8700224UX	61772	IDT7142LA25L48B
5962-8700224TX	61772	IDT7142LA25FB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
2/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology, Incorporated 2975 Stender Way Santa Clara, CA 95054-8015

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